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High-stability polymer gate insulators and interface effects in organic field-effect transistors

Cuvillier Verlag Göttingen

Internationaler wissenschaftlicher Fachverlag

High-stability polymer gate insulators and interface effects in organic field-effect transistors

Vom Promotionsausschuss der

Technischen Universität Hamburg-Harburg

zur Erlangung des akademischen Grades

Doktor Ingenieur (Dr.-Ing.)

genehmigte Dissertation

von

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aus

Ankara, Türkei

2009

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Tag der mündlichen Prüfung: 23.07.2009

Table of Contents

1 Introduction

1.1 Organic Electronics

Electronics play an indispensible role in our daily lives. Due to the continuous evolution in materials processing technologies it became possible to imagine taking advantage of electronics in different areas and to find innovative applications. The most impressive and practical developments are seen in computers and microelectronics. The invention of metal-oxide-semiconductor field-effect transistor (MOSFET) in 1960 opened a new era in electronics, rendering today's computer technology possible, which still has not come to an end following the pace giving "Moore's Law" [1, 2]. Computing and data saving ability of computers increased rapidly. Today, billions of MOSFETs are a part of our every day lives; in our computers, cellular phones, cars, aerospace, medical systems, home entertainment and many other microelectronic devices. These successful implementations are based on the continuous improvement in the handling of the famous semiconductor, silicon.

Besides the high-performance applications, the knowledge gained from semiconductor technology triggered the research on new large-area and low-cost applications. An important example is the development of thin-film transistor (TFT) made of hydrogenated amorphous silicon. Amorphous silicon does not reach the performance of single crystal silicon due to their lower charge carrier mobility. They found applications in low-performance devices, e.g. display applications, where single crystal silicon can not be utilized [3]. Today, TFTs are the basic structures of active-matrix liquid crystal displays, which are replacing the classical displays and televisions. Another celebrated application of silicon is the solar cell. Solar energy gained a large amount of attention in the recent energy crisis and mass production of solar panels launched in industrial countries. Solar cells require large areas to benefit from sun light. Low-cost, low-performance silicon devices are therefore crucial to produce large area devices.

While the evolution in electronics was the main focus of interest, a new field of electronics was silently being launched in 1970s: the discovery and development of electrically conducting polymers [4]. These materials exhibit much lower charge carrier mobility compared to silicon, which results in a large response time and low switching speed, e.g. in a logic circuit. Organic semiconductors offer different, interesting properties that made

them attractive for researchers. These materials are light, mechanically flexible, they can be synthesized at much lower temperatures, and they can be dissolved in organic solvents so that thin-films can be deposited by spin-coating or printing techniques.

Although conductivity was readily observed in various organic materials, it took about 10 years for the researchers to understand the properties of these materials and their appropriate preparation. First field-effect device based on electrochemically grown polythiophene film was presented in 1986 [5, 6]. Since then, a wide variety of new organic materials, both small molecules (oligomers) and polymers have been synthesized and investigated for their electrical properties [7-11]. Field-effect devices with mobility values higher than those of amorphous silicon were presented already in 1997 [12]. With their overall properties conducting polymers impressed the researchers. A new vision of producing low-cost electronic devices on flexible, inexpensive plastic substrates with fast and simple processing techniques was born. Within the last two decades, applications like RF-ID devices [13], electronic paper [14], active-matrix displays with organic light-emitting diodes (OLED) [14, 15], integrated circuits [16], chemical vapor sensors [17], electrochromic windows [18] and organic solar cells [19] are demonstrated. Most of these applications would not be realized with inorganic semiconductors. Moreover, simple applications that use printed organic devices, like electronic card games, are already in the market [20].

"Organic electronics" has become one of the most popular research fields today, being explored by interdisciplinary research groups and institutions [21]. Applications like RF-ID tags, OLED displays and organic solar cells gained much attention since the potential applications have large markets that offer the potential of very high volume production. Therefore, the main driving force of this field is the manufacturing of low-cost products by using, e.g., large-area printing techniques. A forecast made by IDTechEx, a consulting company specialized on electronics, recently reported about a business size of around $250 billion by 2025 [22].

Printed RFID tags find different applications like product identification, brand protection, electronic tickets, etc. These applications belong to the group also named as "disposable electronics" or "one-way electronics", and require extremely low-cost processing techniques. Today the RFID technology is being used in pallet-level tagging in logistics where the costs of used silicon chips are over $0.20. The idea of replacing even the optical bar codes on every product with RFID tags seems to be possible provided that the chips cost less than $0.01, which can be realized by large-area printing techniques [23].

Similarly flexible displays have attractive applications like wearable lightweight information displays and wall-size displays like wallpapers. Several companies have already demonstrated prototypes of flexible organic displays [24-26]. Another very interesting application, organic solar cells, attracted serious attention after the recent improvements in conversion efficiency [19]. Although presented efficiency values are lower than that of silicon-based devices and the organic materials exhibit a limited lifetime, organic solar cells offer exciting capabilities. Since they are transparent and flexible, they can easily be applied over windows of high buildings enabling every building to produce its own electricity. Also the lower manufacturing costs offer the opportunity to cover very large areas with solar cells and produce remarkable amount of electricity. Considering the wide range of applications including flexible lightweight batteries, organic logic memories, corrosion protective coatings, etc., it can be concluded that organic electronics surely is one of today's most interesting research topics, and will be future's one of the most exciting technologies.

However, to achieve more complex applications like RF-ID tags, performance of devices needs to be further improved. Since large-area processing of multilayer structures brings significant limits to materials and configuration, performance of the devices does not reach the level of laboratory test devices. The challenges to overcome towards the commercialization of organic devices determine the direction of research in this field. They can be summarized together with their consequences as follows:

- Low charge carrier mobility → high operating voltages, low switching speed
- Sensitivity of organic materials to atmospheric conditions → short life time
- Difficulties in low-cost processing of functional films with fine structures → high operating voltages
- Reproducibility

Accordingly, research on OFETs can basically be classified into three groups, which have to be considered in close correlation. These groups with their respective research area can be listed as follows:

- Materials and interfaces → performance (mobility), reproducibility, chemical stability
- Device physics → determination of material requirements
- Processing technology → fine electrode structures, reproducibility

This thesis elaborates on organic field-effect transistors (OFET), which are the basic structural units in organic electronic devices (RFIDs, displays, memory devices, etc). Possibilities to improve device performance and to decrease the processing temperatures were investigated. Especially materials aspects are examined in details. New materials are introduced and organic devices with novel gate insulators are presented. The next section briefly introduces challenges and actual topics in OFET research to give a motivation about this study, whereas detailed information on the development of OFET research can be found in chapter 2.

1.2   Scope of thesis

Organic field-effect transistors are among the most intensively studied organic devices. Since their introduction in 1986, electrical performance of organic field-effect transistors increased continuously. Improving the performance of OFETs by optimizing organic semiconductor and dielectric materials is known to be an effective and useful route towards low-cost solution-processed devices. Electrical performance of discrete films of semiconductor and dielectric, as well as their cooperation at the interface is the key to improved properties, such as charge carrier mobility and threshold behavior. Downsizing the device dimensions, such as channel length L and width W; or introducing very high performance inorganic layers also improve the device performance and help discovering the limits of organic devices. But the applicability of downsizing in low-cost, large-area devices is questionable. Therefore solution-processed systems, using low temperature and simple processing techniques are selected for this study.

Semiconductors

It is known that small molecule semiconductors, like pentacene, exhibit higher performance compared to soluble polymers. Due to the small molecule size, crystal grain sizes in range of micrometers can be reached, which enhances the charge transport. However small molecules require vacuum evaporation methods for the film deposition, which are more complex, slow and expensive (see chapter 2). One very promising group of semiconducting polymers come from polythiophenes; poly(3-alkylthiophene) (P3AT). P3ATs offer high field-effect mobility due to their ordering properties and the possibility of wet chemical processing. This group of polymers has been applied in OFETs since 1996 and their properties were readily explored to

a certain extent when this study has started (see chapter 2). Therefore a member of this polymer family was chosen for this research, which is **poly(3-hexylthiophene) (P3HT)**. Organic transistors with inorganic and organic dielectric materials were investigated. Effects of material purity, interfaces, processing solvents, annealing conditions and interaction with the atmosphere on charge carrier mobility and device characteristics are the subjects covered in this study.

Gate insulators

Earlier studies on organic transistors focused almost exclusively on the performance of organic semiconductors. Results pushed the performance of organic devices into the range of amorphous silicon TFTs [12, 27]. Due to the advancement in the understanding of charge transport and charge injection, the research was extended to materials for source and drain contacts and substrate surfaces [28]. There were only several publications concentrating on polymeric gate insulators until the early 2000s. Most of these reports were limited to demonstration of novel devices. Comprehensive research and insight about the influence of dielectric materials were not addressed (see ch. 2). Additionally, from the wide variety of polymers, a limited number of materials were investigated as gate insulators. The studies generally did not focus on a detailed materials selection, but the reported materials were used because they were well established or reported before. However, perhaps the material with the greatest effect on device and semiconductor performance is the gate dielectric. Many years of intensive research was necessary until this became clear and many research groups concentrated on gate insulators [28-31]. Detailed information about recent developments and influence of dielectrics on device performance is discussed in chapter 2.

The extent of studies and reports on gate insulators were very limited when this research has started. This was the driving factor to focus on gate insulators and materials related aspects of OFETs. The method of systematic materials selection and design was followed to improve the electrical performance of devices and to understand solvent and interface related phenomena in OFETs [31, 32]. The innovative scientific achievement established within this study is the introduction of novel insulating materials including thermosetting thin-films as well as ferroelectric, high-k nanocomposites to OFET research. The work addresses the requirements for a gate insulator in a bottom-gate transistor and corresponding materials selection process. The application of selected insulators in OFETs by

optimizing film-processing conditions and investigation of interface issues conclude this work.

Another remarkable accomplishment achieved within this work is the participation of the Hamburg University of Technology (TUHH) in a large scale scientific industrial project, "MaDriX", under The Federal Ministry of Education and Research (BMBF – Bundesministerium für Bildung und Forschung). The research on new printable materials and devices leaded to results that were interesting for industrial institutions working on printed electronics. As a consequence, the Institute of Optical and Electronic Materials of TUHH now participates in a € 15 million project as a sub-contractor of Elantas Beck, together with other industrial companies and universities [33].

The main research topics this study aims to cover are:

- Understanding the device physics and improvement of the performance of hybrid transistors by the optimization of semiconductor processing and dielectric/semiconductor interface
- Systematic selection of new materials for simple solution-processed gate insulators
- Exploring the electrical insulation performance, size limits and surface properties of the selected insulators and their optimization for the selected OFET configuration
- Investigation and comparison of device performance based on material properties, surfaces, solvents and processing parameters
- Preparation and modification of new high-k nanocomposite materials for the reduction of operating voltages
- Demonstration of an all-polymer field-effect transistor by the selected materials
- Demonstration of memory retention and hysteresis behavior in solution-processed ferroelectric OFETs

1.3 Structure of thesis

This thesis is composed of six chapters. First chapter is an introduction on organic electronics and organic field-effect devices. Second chapter gives the theoretical background on conducting polymers and the technology of organic field-effect transistors. It also includes parameter extraction in organic field-effect devices. Chapters 3, 4 and 5 are about the main

experimental work realized in this research. In chapter 3 hybrid devices are discussed where the electrical properties of semiconductor P3HT were characterized. Influence of purity, annealing conditions and processing solvents are investigated. Chapter 4 deals with gate insulators, including materials selection and electrical characterization of both the insulation layers and OFETs with these insulators. Importance of semiconductor/dielectric interface is addressed. In chapter 5 solution-processed ferroelectric functionalized OFETs are presented. Ferroelectric poly(vinylidene fluoride) based copolymer was blended with barium titanate nanopowder to reach high dielectric permittivity values, which helps sinking the operating voltages without disturbing the ferroelectric functionality. The final chapter concludes the work and addresses further suggestions for the future work.

2 Theoretical Background

In this chapter a theoretical overview about the technology of organic field-effect transistors is presented. The essential understandings to design, conduct and evaluate the experimental studies that are conducted in this thesis are given. The first section describes polymers and their applications as electrical insulators, including coating applications. Conjugated polymers are introduced in the second section, where different materials and conduction processes are briefly discussed. The third section, "OFET Technology", begins with the introduction of different types and operation principles of OFETs. Theory of MOSFET is briefly discussed in order to elaborate on parameter extraction in OFETs. Furthermore, in a detailed literature review about solution-processed OFETs and polythiophenes, the recent developments in the field are addressed.

Gate insulators in organic field-effect transistors are the focus of the fourth part, which is also the main focus of this work. This section gives a detailed overview about various dielectric materials, solvents and interface issues. Different approaches to a wide variety of problems related to dielectrics will be presented and discussed. Focus is more on solution-processed systems, since they offer the possibility of simple reel-to-reel production. Interface engineering is the topic of the next section. The importance of interfaces is addressed and the efforts to improve interface related properties are presented. Finally, ferroelectric OFETs are introduced. In this part the research on organic non-volatile memory devices is summarized, where charge storing ferroelectric or electret layers are combined with semiconducting polymers.

2.1 Polymers

2.1.1 Polymer Structure

Polymers are organic, semi-organic or inorganic chemical substances composed of large polymer molecules (macromolecules). These molecules consist of usually a thousand or more atoms in the form of repeating units, thereby possessing very high molar masses. The units are typically connected by strong covalent bonds and therefore built very long and stable chains. One of the simple examples is polyethylene, which is composed of repeating ethylene units $[CH_2=CH_2]_n$. Number of repeating units "n" indicates the degree of polymerization (N) of the

molecule, which determines the molecular weight. Polymeric materials can possess different properties although they differ only in molecular weight. Therefore molecular weight is a basic material property for polymers.
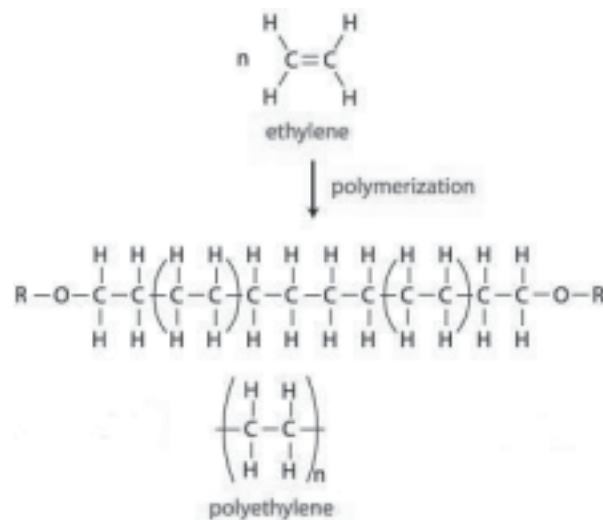
Figure 2.1 Molecular structure of ethylene and its polymerization to polyethylene.

Polymers are classified into two major groups based on their thermal behavior. The polymers that have the ability to melt or heat-soften are named as **thermoplastics.** Typical examples of thermoplastics are polyethylene, polystyrene, polypropylene, polyvinylchloride (PVC) and poly(methylmethacrylate) (PMMA). These polymers consist of chains that do not have permanent chemical bonds to their neighbors. Instead, molecules attract each other by the interaction of different side groups via physical forces, like ionic or hydrogen bonding, to the neighboring chain. Also weak van der Waals forces contribute to the intermolecular bonding. Upon heating a thermoplastic material, these bonds are weakened and the molecules start to slide over each other. This results in a polymer that can be processed like a viscous liquid. Upon cooling, the bonds are created again. This gives the opportunity to recycle thermoplastics. On the contrary, **thermosets** consist of individual chains that are chemically linked by covalent bonds. The bonds are formed either during the polymerization or by subsequent chemical or thermal treatment during fabrication. The structure can be described as an interconnected network of cross-linked molecule chains. Once the crosslinked network is formed, thermosets do not flow or melt, and resist chemical solvents. They can not be dissolved, but they can soften or swell. Such properties make thermosets feasible for applications like coatings, adhesives, and composites. Typical examples include epoxy resin, phenol-formaldehyde resins, polyimide, and unsaturated polyesters. **Elastomers** and

thermoplastic elastomers are the other two classes of polymers. Elastomers (rubber) consist of crosslinked molecules, similar to thermosets, whereas their crosslinking density is much lower than that of thermosets. The chains have a high degree of local molecular motion, which results in soft and elastic materials. The polymer flow is limited mainly by chemical crosslinks. Thermoplastic elastomers differ from classical elastomers in the sense that their crosslinks can be broken up thermally, which allows further processing [34-36].

(a)   (b)
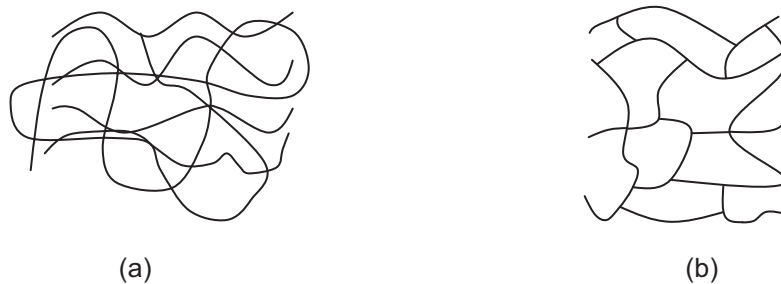
Figure 2.2 Symbolic chain structures of (a) a thermoplastic and (b) a thermosetting polymer.

Properties of all kinds of polymers are strongly affected by the details of chain structure, which can be listed as:

1. The chemical composition of the chain
2. The sequence of monomer units in the chain (copolymers)
3. The stereochemistry or tacticity of the chain (side groups)

Copolymers

New properties can be gained from polymers by using two different repeating units in the same chain. Such polymers are named as **copolymers**. The exact order of the monomer units on the chain can vary depending on the reaction rates of each monomer during the copolymerization process. Typical examples are derived from vinyl monomers, such as styrene, ethylene, vinyl chloride and vinyl fluoride. In Fig. 2.3, polyvinylidene fluoride homopolymer and polyvinylidene/trifluoroethylene copolymer are shown.
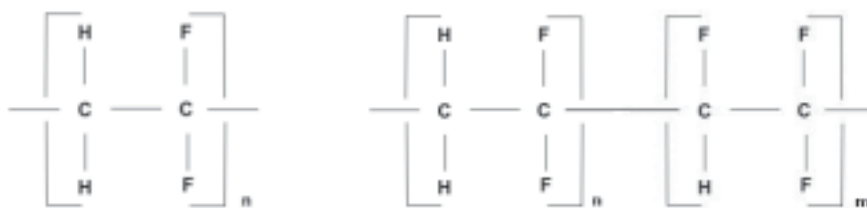
Figure 2.3 Molecular structures of poly(vinylidene fluoride) (PVDF) homopolymer and poly(vinylidene fluoride) – trifluoroethylene (PVDF-TrFE) copolymer.

Tacticity

Many polymers consist of side groups of different kinds and sizes. In this case, the **stereochemistry**, i.e. the direction and repetition of the side groups, play an important role in determining the properties. There are three different possible configurations in polymers. If the side chains lie on the same side of the plane formed by the extended polymer backbone the configuration is named as **isotactic**; if the substituent groups regularly alternate on both sides, **syndiotactic**; if the side chains are randomly placed, **atactic**. Generally, the polymers showing tacticity (isotactic or syndiotactic) are semicrystalline (see solid-state properties below), while atactic polymers possess an amorphous structure.

(a)   **(b)**

Figure 2.4 Schematic chain structures of (a) isotactic (upper), syndiotactic (middle), atactic (lower) molecules and (b) a crystalline polymer [37].

Solid-State Properties

Depending on the molecular structure, polymers can adopt **amorphous** or **semicrystalline** phases. In the amorphous phase the polymers do not exhibit any kind of order. The chains take spaghetti-like random conformation. Sometimes a certain long-range order is observed, whereas a crystalline ordering does not occur. Amorphous polymers show either a rubbery or a glass-like behavior, depending on the temperature. They can be transformed between these

two states reversibly by heating and cooling. Upon heating a classy amorphous polymer, **glass transition temperature** is the point where this transformation occurs and the chains begin to slide. They do not possess a certain melting point, similar to glass. Accordingly, glass transition temperature is a specific materials property for polymers. Polymers, which have the ability to crystallize, form microscopic-scale crystallites that are surrounded by amorphous chains. They do not crystallize completely like small molecules, due to the entanglements of extremely long chains. Therefore they are named as "semicrystalline polymers". The physical and chemical properties of polymers are therefore determined by both the properties of the crystalline phase, and those of the amorphous "tie chains" that connect crystal grains. Unlike their amorphous counterparts, crystalline polymers possess a certain melting/freezing temperature, due to the sudden dissolution of crystallites. Upon cooling a molten polymer, the chains tend to pack closely since it is thermodynamically favorable. Upon further cooling, crystalline polymers also possess a glass transition and become brittle [34-36].

Polymers are used in increasing number and type of applications, thanks to the development of polymer science and technology. General properties of polymers that make them attractive for many applications include low density, mechanical flexibility and toughness, very good electrical insulation, good resistance against inorganic chemicals, simplicity in processing into pure or composite materials, optical transparency and additionally the recently applied semiconducting properties. The intrinsic conductivity in organic materials is the topic of chapter 2.2, while electrical insulation aspects and applications can be found in the following chapter.

2.1.2 Electrical Properties of Polymers

Materials are subdivided according to their electrical conductivity σ into three classes: insulators ($\sigma < 10^{-14}$ S/cm), semiconductors ($\sigma = 10^{-9}$-10^{-2} S/cm) and conductors ($\sigma > 10^{3}$ S/cm). Most plastics are electrical insulators since their electrons are tightly bound to their atomic nuclei. This section gives an overview on electrical properties of polymers related to their chemical and structural properties, and therefore gives the background to understand the electrical insulation behavior of different polymers.

The basic parameters which define the insulating properties of a polymer are:

1. Volume resistivity (ρ)
2. Dielectric constant (ε_r) and dielectric loss
3. Dielectric strength (S) or breakdown voltage (E_B)
4. Surface resistivity
5. Arc resistance

Volume Resistivity

According to their electrical properties plastics can be divided into two classes as excellent and moderate insulators. Polymers that consist of non-polar groups like carbon-carbon or carbon-hydrogen bonds are excellent insulators. Typical examples are polyethylene, polypropylene and polystyrene. Polymers made from polar groups exhibit moderate insulation, due to the interaction of their dipoles with electric fields. Small electric fields cause a change in orientation of the dipoles of a dielectric material, while high fields remove electrons from some atoms, which result in the formation of ions. These ions are mainly responsible from electrical conduction in polymers, not the electrons themselves[34, 38]. PVC, PMMA and poly(vinyl acetate) are some examples to polymers with polar groups.

Dielectric Constant

Dielectric constant is a specific materials property, which is inversely related to resistivity for polymers. It depends strongly on the polarizability of molecules within the polymer. In non-polar (nonionic) polymers, the molecules are covalently bonded to each other with shared electrons. Under an applied electric field, there will be a displacement of the electron cloud in one direction and a smaller displacement of the positively charged nucleus in the other direction, resulting in an induced dipole. The polarization caused by the displacement of electron cloud is named as **electronic polarization**. In certain polymers, the electrons of a covalent bond are not equally shared, but rather closer to one of the bonded atoms. The resulting permanent dipole takes an orientation under an electric field, which leads to polarization of the polymer. This is known as **orientation polarization** and observed prevailingly in polymers with polar groups or atoms. In polar polymers the electric field dependent orientation can be seen in whole molecule, depending on the place of the polar group. If the dipoles are on the polymer backbone, their alignment is hindered, due to the stiff backbone. The dipoles would first start to orient at higher temperatures, which results in an

increase in the dielectric constant. If the polar groups are on the side chains, the situation becomes more complex, so the dielectric constant will be depending on various factors.

Dielectric loss

In case of an alternating electric field, dipoles try to follow the direction of the field by aligning themselves. If the alternation frequency is low, the dipoles have time for the alignment and the polymer exhibits a high dielectric constant. As the frequency increases, the orientation lags behind the change in field polarity and the dipoles become less susceptible to the electric field. At even higher frequencies the electric field alternates so fast that the dipole alignments lose all correlation with the field and the dielectric constant decreases to a minimum. Therefore the electrical energy input to polarize the polymer is lost in the form of thermal energy. The ratio of energy lost to the stored energy in the polarized polymer is called as the **dissipation factor**. In literature, the **dielectric loss** is quoted as the numerical product of dissipation factor and the dielectric constant.
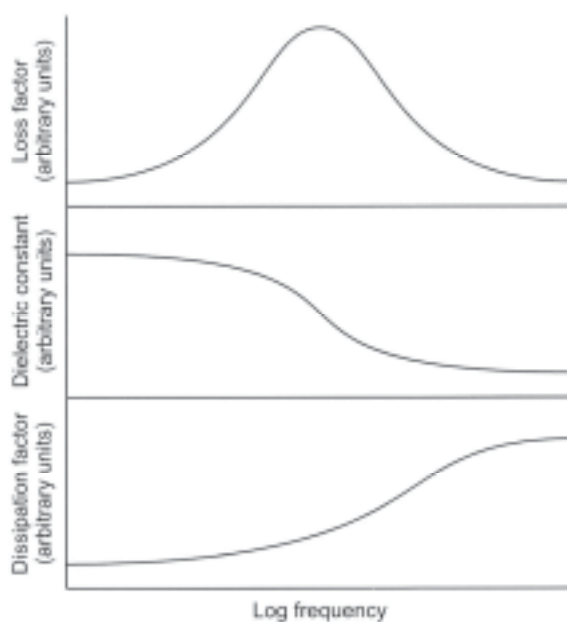
Figure 2.5 Typical behavior of dielectric constant with frequency and its relationship to the loss and the dissipation factors.

There is an important distinction between electronic and orientation polarization mechanisms, when the frequency dependence is considered. Electronic polarization involves only the movement of electrons, while orientation polarization requires the movement of a part or the whole of the molecule. Therefore in the latter, the polarization is much slower, which leads to a much stronger frequency dependence at moderate frequencies. At very high frequencies, as

explained in the previous paragraph, the orientation part of the polarization misses completely. As a result, the dielectric constant is dependent only on the electronic polarization. Accordingly, the temperature dependence of dielectric constant can be explained by in view of both types of polarization mechanisms. Since the alignment of molecules is temperature activated, the dielectric constant of a polar polymer is strongly dependent on temperature. On the contrary, dielectric behaviors of nonionic polymers that exhibit electronic polarization are not affected from temperature [34-36].

Under these circumstances, the basic dielectric properties of polymers can be summarized in two points:

1. In non-polar polymers, the dielectric constant is mainly due to electronic polarization and will have a value up to 3. Since the polarization is instantaneous the dielectric constant is independent of frequency and temperature. Thus, the dielectric loss is negligible

2. In case of polymers with polar groups or bonds, the contribution of orientation polarization to the dielectric constant is temperature and frequency dependent. Such polymers typically possess dielectric constant values between 3.0 and 8.0. Temperature behavior of dielectric constant also depends on whether the polar groups are attached to the main chain. When they are, the orientation polarization will depend on segmental mobility, which is lower below the glass transition temperature. This not only influences the dielectric constant, but also such polymers are better insulators below their glass transition temperatures.

Applications of Polymers in Electronics

Except the field of organic electronics, the applications of polymers in electronics industry include encapsulation of semiconductors, photoresists, printed circuit board components, solder masks, laminates, masking tapes, adhesives, vibration dampers, etc. Wide variety of applications of polymers as active electrical insulation can be found in celebrated references, together with their coating conditions and electrical properties [38-40]. These references present the research on a wide variety of polymeric materials for thin-film applications, which surely are very interesting and inspiring for the organic electronics research community.

2.2 *Conducting polymers*

Early foundations on conducting polymers date back to mid 1800s, whereas first scientific studies reporting electrical resistivity values of doped polypyrrole polymers were presented in 1960s [41]. The discovery of Ziegler-Natta polymerization in 1958 made the production of highly crystalline polyacetylene possible. Starting from early 1970's Shirakawa and coworkers elaborated on these polymeric materials intensively, where they optimized the polymerization methods. Finally in 1977, A.J. Heeger, A.G. Diarmid and H. Shirakawa reported their discovery of metallic conductivity in polyacetylene by oxidizing the polymer with iodine vapor; which was named as "doping" analogous to inorganic semiconductors. After series of systematic studies on various conjugated polymers based on their foundations conducting polymers were developed to a state that they can be used in real applications. Number of discovered conducting polymers increased continuously so that a new interdisciplinary field of research, called "plastic electronics", was born. In year 2000, these three scientists were awarded the Nobel-prize in chemistry for their work in 1977 [42]. Today different kinds of such polymers find applications in corrosion resistant coatings, electromagnetic shielding, antistatic coatings, electrochromic windows, as well as in more complex devices like field-effect transistors, sensors, solar cells, etc. Although even today the details of physical conduction mechanisms are still under investigation, it is already known that conducting molecules have one thing in common; alternating single and double bonds – the conjugation. The following section gives an introduction on conjugated polymer systems.

2.2.1 Conjugated systems

Conjugated molecule systems are those having covalently bonded atoms with delocalized charges [43]. Molecules with alternating single and multiple bonds form conjugated systems, where electrons do not belong to a single bond or atom, but rather a region. One very effective example demonstrating orbital behavior in conjugated systems is the benzene molecule.

Benzene consists of six sp^2-hybridized carbon atoms in shape of a hexagon. There are alternating double and single bonds between the C atoms. In a sp^2-hybridization, three of the total four valence electrons are shared in σ-bonds and one of them takes part in the p-bonding, which is in the double bond. In the double bond structure, σ-bond is much stronger than the p-bond, so the six electrons in three p-bonds are delocalized over the entire ring, which are shown inside the hexagon. Therefore conjugated polymers have a quasi-infinite π-system extending over a large number of recurring monomer units, which is the basis of electrical

conduction in molecules. As a result of the continuous π-electron system conjugated materials exhibit directional conductivity along the chain axis.
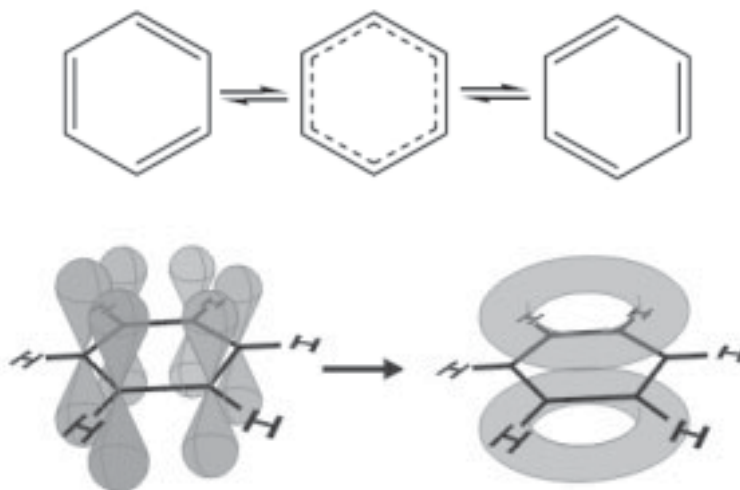
Figure 2.6 (a) Molecular structure of benzene, (b) π-orbitals and their structure showing delocalized states [44].

Conjugated polymers, in their pure state, are either insulators or semiconductors, so conjugation is not enough to make the molecule reach a metallic conductivity. In addition, charge carriers in the form of extra electrons or holes have to be present in the material. These extra charge carriers can be created artificially by oxidation/reduction (doping) of the molecules by treating the molecules by, e.g. halogens [42]. Additionally, the defects in conjugation also contribute to charge transport, since they disturb the charge balance. High electrical conductivity is not the only important property of organic conductors. On the contrary in organic semiconductors a controlled process of charge transport is required. Therefore other conduction processes and different types of charge carriers in organic materials are also discussed in the following part.

In addition to the charge transport along the molecule, the understanding of charge transport between molecules of a polymer is of great importance for organic electronics. Bulk conductivity in the polymer material is limited by the need for the electrons to jump from one chain to the next, which is the intermolecular charge transfer reaction [45]. It is also limited by macroscopic factors such as grain boundaries in the material.

2.2.2 Charge transport in conjugated polymers

There are several concepts describing charge transport in organic semiconductors. In different studies detailed physical mechanisms of charge transport have been discussed and existing models are improved by considering new aspects. However, relatively complex and overlapping conduction mechanisms make it difficult to extract certain conclusions. This part of the thesis gives a brief qualitative overview about currently used models. Detailed discussions about recent developments in this field can be found in recent publications [37, 46, 47].
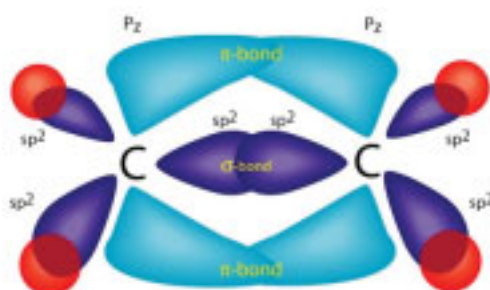
Figure 2.7 Molecular structure of ethylene presenting σ- and π-bonding together with the hybridization states of orbitals [48].

To understand the charge conduction in conjugated materials, the type and origin of charge carriers, as well as the mechanisms of charge transport should be taken into account. In Fig. 2.8, charge carrier (polaron) formation is shown on the simplest conjugated polymer, polyacetylene. Polyacetylene is formed by the polymerization of ethylene (Fig. 2.7). Polyacetylene consists of a one-dimensional chain with alternating single and double bonds. When a halogen, like iodine (I_2), is introduced to polyacetylene it removes an electron from the polymer under formation of an I_3^- ion. Therefore the polymer is oxidized, or in terms of molecular electronics, "doped". A hole is created on the chain. Upon increased doping, bipolarons may form as well as new polarons. Solitary wave defects, solitons are structural defects like polarons, which also play an active role in charge transport in conducting polymers. In polyacetylene, solitons can be formed during thermal isomerization or doping [42]. As a result, the order of single and double bond alternation is disturbed where an extra charge is formed, as shown in Fig. 2.8.

Polyacetylene

Polaron

Soliton
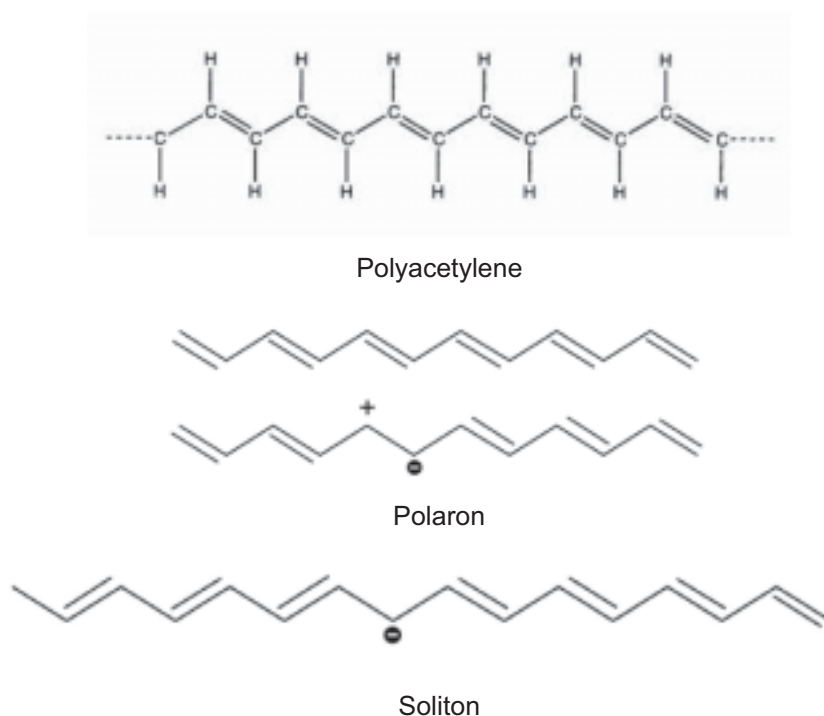
Figure 2.8 Molecular structure of polyacetylene and the structural defects that are responsible from charge transport along the molecular backbone.

One of the basic concepts describing the charge transport in solids is the electronic band structure. Just like in the demonstration of ethylene molecule, electrons are delocalized over the entire molecule, forming an "electron cloud". In conducting polymers showing high level of crystallinity molecular orbitals correspond to individual energy levels. Electrons fill the energy levels starting from the lowest to the highest, where in case of conjugated molecules the highest energy level is the p-orbital. Therefore p-orbital is where conduction processes occur in conjugated polymers. The highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) in conjugated systems are similar to the valence and conduction bands in inorganic semiconductors, from the electronic point of view. So the extended-overlap p-bands become the valence band and p*-bands the conduction band. Considering this analogy, the energy difference between HOMO and LUMO levels is regarded as the band gap of organic semiconductors. Therefore the electronic band theory for semiconductors can be considered for conjugated systems as well [49-52]. With increasing doping, i.e. polarons, solitons, new energy states are introduced into the band gap, which increases the conductivity. Band model is developed for perfect crystals by phonon-scattering and does not take the impurities into account. Additionally, partly crystalline materials, like ordered semiconducting polymers, are not described in this model.
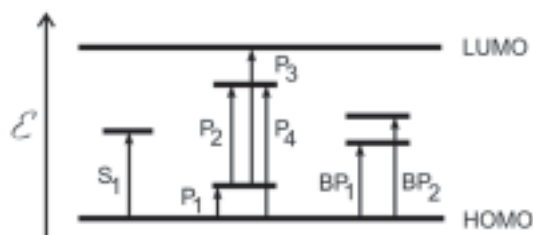
Figure 2.9 Energy level of solitons, polarons and bipolarons in the energy band gap [37].

As mentioned before charge transport in conducting polymers can be considered in two parts; microscopic and macroscopic. Due to the continuous metallic-like "electron cloud" the conduction along the chain occurs without any energy loss, provided that the conjugated structure is ideal and isolated. However, in real systems this transport is disturbed by both the defects on the chain and electrostatic interaction with the environment. In the cases where the charge transport is disturbed, the charges jump over the defect states by **"hopping"**. In the hopping model, the charge carriers remain at localized positions for a certain time so that the molecule around the charge returns to the relaxed state. One of these carriers are polarons, which are extra electrons accompanied by the surrounding polarization field [53]. The electrons are therefore neutralized by the relaxation of the surrounding lattice and all together the polaron gets to an energetically stable state. As a result, it needs activation energy to jump to other sites. The activation energy depends on the pi-orbital overlap between molecules. At high temperatures, these jumps are assisted by phonons, whereas at low temperatures **"tunneling"** mechanism dominates due to the absence of phonons. This explains the increase in mobility with increasing temperatures. Hopping mechanism is also active in macroscopic transport, where the charges jump from one chain to another. Therefore in well-ordered, close-packed polymers hopping occurs much easier, which also contributes to charge carrier mobility. Tunneling model assumes the jump of a charge carrier without following the activation energy route. The charges "tunnel" through the energy barrier. Therefore the possibility of tunneling depends on the width of the energy barrier, as well as the mass and the energy of the tunneling particle [54]. Tunneling and hopping are both thermally activated processes and generally treated under hopping model.

Another macroscopic conduction model used in partly crystalline molecules is the **"grain boundary model"**. It assumes that the charges are strongly localized at certain lattice positions and fully stabilized again relaxing the surrounding molecules [55]. Grain boundaries are such high energy positions where the possibility of **"charge trapping"** is the highest.

Since the molecules have a random amorphous structure, the orbital overlap is weak. Therefore, charges which travel easily through the well-ordered crystal grains full of delocalized charges meet large energy barriers and slowed down. As a result, the overall conduction is limited to the grain boundary conduction, since it is the slowest-step.

Similar to the grain-boundary trapping, additional trap states also play an important role in charge conduction. Chemical impurities, interface irregularities or lattice defects act as "trap states" in conjugated polymers. The **"multiple trapping and thermal release"** model explains charge transport from the point of view of traps and their nature. It assumes an equal distribution of traps over the whole lattice [56]. The defects introduce new energy states into the band gap between HOMO and LUMO states. Charge carriers are first excited to these states, where a further jump requires additional activation energy. Therefore they become trapped in these states. The equilibrium between trap and release is used to model the charge conduction kinetics. Vissenberg and Matters presented an improved version of this model considering different types of traps, where also gate voltage dependent mobility is discussed [57].

2.2.3 Organic semiconductors

Due to the early discovery of its electrical conductivity, polyacetylene was initially the most studied conducting polymer. However, its high chemical instability and related aspects made the research on polyacetylene to be confined to scientific experiments. Poly(aniline), poly(pyrrole), poly(phenylene vinylene) and polythiophenes remain the most extensively investigated conjugated polymers to date, from scientific, practical and commercial points of view. These polymers find applications both as semiconductors (pure, not doped) and as conducting electrode materials (in doped state) in field-effect devices. The most widely used specific examples are P3HT, poly[9,9-dioctylfluorene-co-bithiophene] (F8T2), polyquarterthiophenes (PQT) and polytriarylamines (PTAA) [58]. In addition to polymers, conjugated small molecules have also received attention for their semiconducting properties. Although the very initial experiments on molecular semiconductors were on anthracene and tetracene, pentacene has become one of the most extensively studied materials in field-effect devices. As already mentioned before, these materials are deposited by vacuum evaporation and from very large crystal grains. As a result of this, very high charge carrier mobilities (3 cm^2/Vs) can be reached. Oligothiophenes, copper phthalocyanine and rubrene are additional molecular semiconductors, which exhibited remarkable electrical properties in OFETs.

Further information on different types of organic semiconductors can be found in recently published review papers and books [58, 59].

In this study, regioregular poly(3-hexylthiophene) (P3HT) and pentacene (only for comparison purpose) were used for the experiments. In section 2.3, a more detailed literature review on P3HT devices can be found. In chapters three and four the electrical characteristics of P3HT are investigated extensively. Self-ordering (crystallization) tendency of P3HT upon solution-deposition and its influence on mobility are discussed in the following chapters as well.

2.3 OFET Technology

2.3.1 Organic field-effect transistors

Organic field-effect transistors are multilayer thin-film devices which are structurally analogous to their inorganic counterparts, metal oxide semiconductor field-effect transistors (MOSFET). They are also named as organic thin-film transistors. OFETs consist of three functional materials – a semiconductor layer, an insulating layer and three electrodes. OFETs have several structural variants, according to their manufacturing methods. Bottom-gate (BG) and top-gate (TG) configurations indicate the order of deposition of semiconductor and dielectric layers. In BG configuration, gate insulator is deposited on the gate electrode and acts as a substrate for the deposition of semiconductor. In the top gated variant, the insulator layer is deposited onto the semiconductor. In the bottom gate configuration there are two further alternatives, which are called the top contact (TC) and bottom contact (BC). The configuration of an OFET is determined not only by its operating principles, but also by processability of the successive layers on top of each other. Each of these different configurations has its advantages and disadvantages, again from both processing and electronic points of view. Bottom gate devices, where the semiconductor is processed on the dielectric, are generally preferred because most of the organic semiconductors are very sensitive to solvents and heat. It is therefore more difficult to process dielectric on semiconductor layers. Bottom contact structures are preferred to enable the use of photolithographic techniques on the dielectric layer.
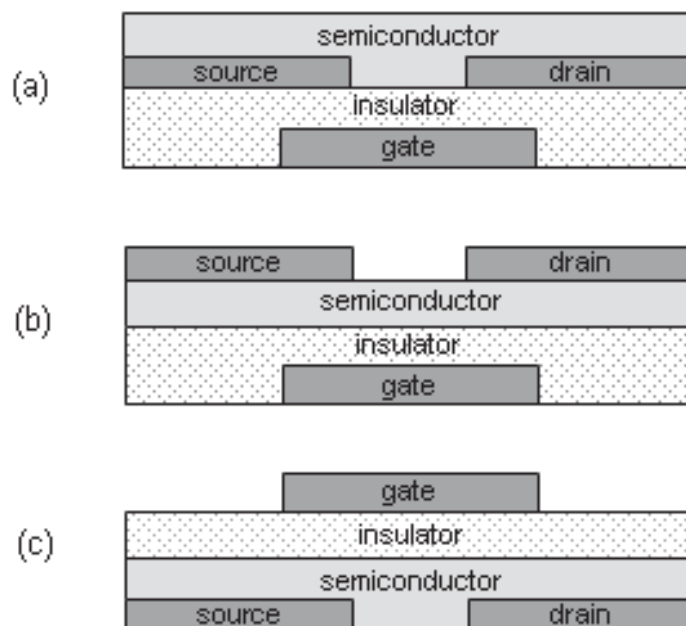
Figure 2.10 Schematic view of different OFET structures (a) BG-BC, (b) BG-TC, (c) TG-BC.

Depending on the processability of used materials and their properties, different methods are used in manufacturing OFETs. For example, polymers that are soluble in organic solvents are preferred, since they offer the possibility of using large-area processing techniques like ink-jet printing, spin-coating, doctor-blading, etc. Also dispersions of organic or inorganic materials can be solution-processed. However, it is crucial to avoid dissolution or swelling effects during the successive deposition of organic layers, to prevent interfacial mixing. This significantly restricts the choice of materials and solvents, which is one of the main challenges in front of organic electronics towards realization of reproducible products. This phenomenon and other material- and interface-related aspects are further discussed in section 2.3.3, and in the experimental chapters 3 and 4. Direct electrochemical polymerization of semiconductors between the S/D electrodes has also been used to process organic devices.

Additionally, vacuum deposition techniques are used for organic film deposition. Physical vapor deposition (PVD), sputtering, electron-beam evaporation methods are generally used to deposit metallic electrodes for organic devices. Also small semiconductor molecules, like pentacene and sexithiophene, can be thermally evaporated. Although vacuum deposition methods are time-consuming and more complex with respect to processing from solutions, vacuum deposited devices exhibit a much higher performance [58], due to solvent-free high-purity materials and precisely controlled deposition conditions.

In addition to the deposition of functional thin-films, structuring of S/D electrodes and hence the transistor channel, is the other important challenge in OFET processing. Patterning methods like lithography [15, 60, 61], laser ablation [62-64], selective surface activation [23], MIMIC [65] and printing [23] are utilized, whereas only a small fraction of these satisfy the large throughput speeds necessary for efficient fabrication of devices. Transistor channel length (L) and width (W) determine the operating voltages, so fine and precise structuring of S/D electrodes is essential for high-performance devices.

2.3.2 Operating Principles and Parameter Extraction

OFETs basically operate like their inorganic counterparts, MOSFETs. The gate insulator acts as a capacitor. When a voltage is applied to the gate electrode a capacitance is formed between gate and semiconductor. The induced charge in the capacitor creates a conducting channel on the semiconductor side of capacitor, provided that the charge carriers can be injected into the semiconductor. The resistance of this channel is proportional to the amount of induced charge, which is controlled by the gate voltage. At low drain-voltages, current follows the voltage linearly. In the *linear regime* the transistor works like a resistor, where the current is controlled by both gate and drain voltages. When the drain voltage is further increased to the level of gate voltage, the channel starts to deplete at the drain-end. The channel goes into the pinch-off state where the drain current saturates and becomes independent of the drain bias. This is called as the *saturation regime*. This behavior can be observed from output characteristics of a field-effect transistor (Fig. 2.11).

Linear and saturation regimes can be defined quantitatively by the following equations:

$$I_{D,lin} = \frac{W}{L} \mu C_i \left(V_G - V_T - \frac{V_D}{2} \right) V_D \qquad (2.1)$$

$$I_{D,sat} = \frac{W}{2L} \mu C_i \left(V_G - V_T \right)^2 \qquad (2.2)$$

where W and L are the channel width and length; V_T is the threshold voltage, μ is the field effect mobility of the semiconductor film and C_i is the capacitance per unit area for the gate insulator.

These equations are also used to predict OFET characteristics considering the following assumptions [21]:

1. The electric field created by the gate, which is perpendicular to the channel, is much larger than the field along the channel (gradual channel approximation); which is generally the case in organic devices where channel length is greater than dielectric thickness,

2. The field-effect mobility μ is constant for a semiconductor layer.
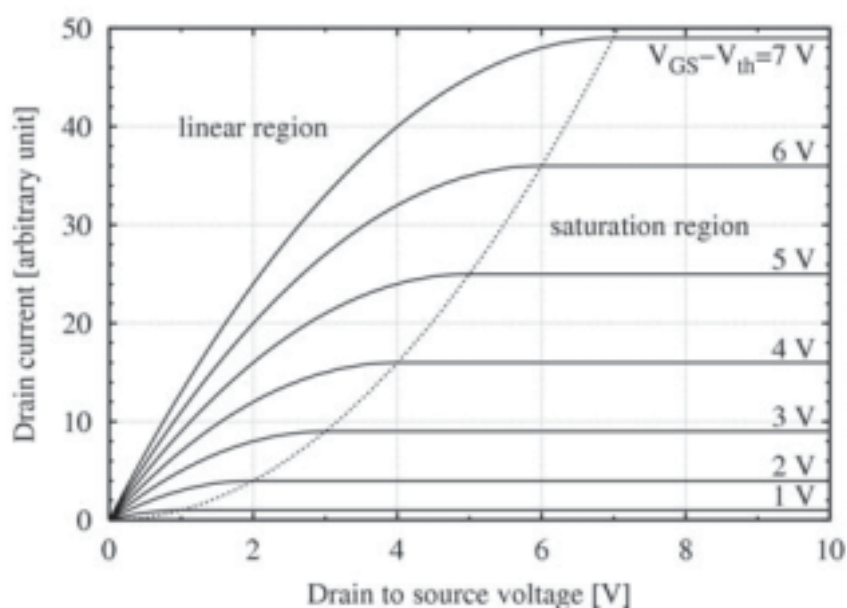
Figure 2.11 Typical output characteristics of a MOSFET.

Charge carrier mobility is the quantity relating the average drift velocity of charge carriers under an applied electric field. Mobility is an important property in organic field-effect transistors since it influences essential device properties like the device switching speed. There are different methods for the determination of mobility including optical [66] and electrical methods like time of flight measurements [67], or using the Hall Effect [68]. These methods mostly return significant differences in the determined mobility values for a semiconductor. Therefore in organic devices the mobility is generally derived from I – V characteristics, as discussed below, and regarded as "device mobility" rather than a semiconductor material property.

Transconductance g_m which is defined as the rate of change in the drain current with respect to a change in gate voltage at a constant drain voltage can be used to calculate the field effect mobility in linear regime. Drain current equation for the linear regime (Equation 2.1) can be derived with respect to gate voltage at a constant drain voltage to find g_m.

$$g_m = \frac{\partial I_d}{\partial V_g}\bigg|_{V_d = const} = \frac{W \mu_{lin} C_i}{L} V_d \tag{2.3}$$

Transconductance and related transistor characteristics are best observed from the transfer characteristics (I_D vs. V_G) of an OFET as seen in Fig. 2.12. The saturation charge carrier mobility can be calculated from the slope of the plot of $I_D^{1/2}$ vs V_G. Threshold voltage V_T can be read from the same plot where the extrapolation of the slope line intersects the x-axis.
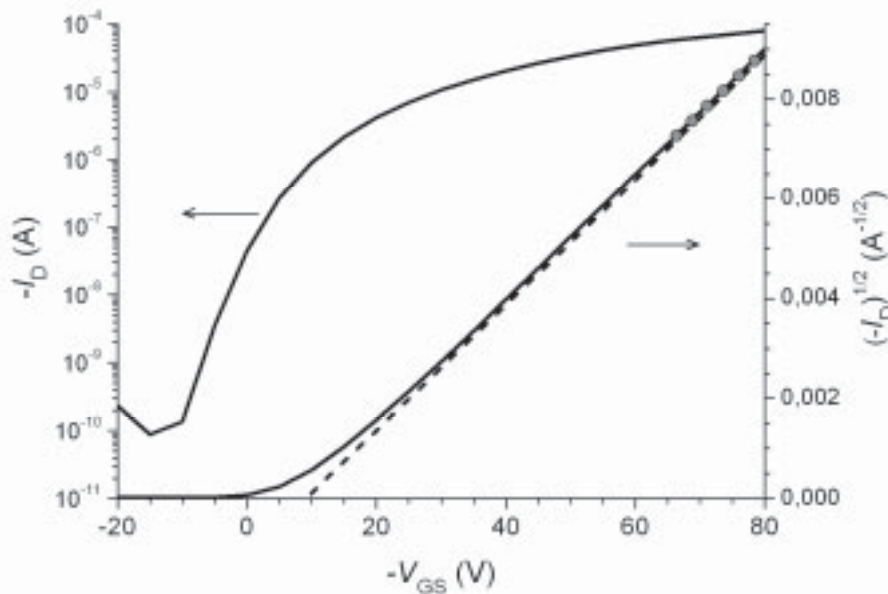
Figure 2.12 Transfer characteristics of an OFET demonstrating the evaluation of threshold voltage by extrapolating the tangent drawn on the $I_D^{1/2}$ vs. V_G plot.

There is an important difference between OFETs and their inorganic counterparts, especially when the MOSFETs operating in inversion mode are considered. Such a MOSFET consists of, e.g. a p-type channel and n-type charge injection zones, at zero gate bias a drain current can not flow between source and drain even if a voltage is applied. Two diodes are formed

between the source-drain and the semiconductor, which only allow a negligible amount of charges to be injected into the semiconductor through the diode. In organic devices, however, metallic electrodes are generally used as charge injection layers with the active semiconductor layer. The contacts formed here are most frequently not diodes like in MOSFETs. They are either ohmic or Schottky contacts, which are out of the scope of this study. The result is that, if a drain bias V_d is applied a drain-source current flows even at zero gate bias, $V_G = 0$. Therefore, OFETs are named as **normally on** devices, and operate in the accumulation mode. The current flowing without any gate effect corresponds to the conductivity σ of the film which can be calculated according to Equation (2.4),

$$\sigma \cong \left(\frac{L}{W \cdot t} \right) \frac{I_{ds}}{V_d} \Bigg|_{V_g \ = \ 0, \ V_d \ \to \ 0} \tag{2.4}$$

where W is the channel width, L is the channel length and t is the semiconductor film thickness. Off-current is an important parameter in organic devices, since it influences the ratio between on- and off-states of the device significantly. It depends mainly on the conductivity of the organic semiconductor and the energy barrier at the electrodes. Conductivity depends mainly on the unintentional doping in an organic semiconductor, which can have different natures. This phenomenon and its influence on device characteristics will be discussed in details in section 2.4.2 and in the following chapters of experimental work.

2.3.3   Solution-processed OFETs: P3HT

The most attractive feature of organic field-effect transistors is the possibility of fabrication by using simple processing techniques from polymer solutions. Therefore commercial printing techniques are considered for processing different materials into functional layers. These techniques allow large-area production under ambient atmospheric conditions with high throughput speeds.

Organic transistors and basic integrated-circuits have been demonstrated using some of the presented printing techniques. In most of these efforts, however, these techniques are combined with other conventional processing methods. One of the main drawbacks of printing is the limited precision of the printing technique. In order to achieve high resolution

structures various parameters including solution viscosity, surface energy, printing speed, have to be optimized. Innovative solutions like pre-treatment of the substrates creating a surface energy pattern increase the resolution [69]. However, in most of the previous studies on organic transistors device L and W sizes of 50-100 μm are used, which were obviously large and create problems like parasitic capacitance, high operating voltages and low switching speeds [23]. Another high-throughput structuring method is the laser ablation. In this case the layers to be patterned are solution-coated on the complete substrate and structured afterwards via laser ablation. Structure sizes lower than 10 μm have been successfully demonstrated with laser-patterning, by the optimization of the beam properties according to layer thickness and properties [64]. Meanwhile, there are several research groups who integrated several printing techniques for manufacturing organic devices [33]. Completely printed organic RF-ID tags and electronic tickets are already presented, whereas the performance, reproducibility and life-time are still the issues under research.

Considering these efforts for the low-cost, large-area production of organic devices, it can be concluded that solution-processed devices and integrated circuits are still the main focus of research in organic electronics. Accordingly, direct solution deposition of organic semiconductors and other functional layers are more desirable than vacuum evaporated or precursor systems, in terms of processing speed and quality [70].

Polythiophenes

Organic semiconductors, like almost all conducting polymers having a π-π backbone structure, are not soluble in common organic solvents. To increase the solubility, side groups are added to the polymers. Typical examples to these polymers are the alkyl-substituted polythiophenes (Fig 2.13). Alkyl side groups of different sizes are incorporated at the 3-position of each thiophene ring which lead to significant increase in the solubility [70]. The solubility increases with the length of a particular substituent group. In addition to increased solubility, if the side groups are produced in an isotactic configuration, they help the thiophene polymer backbone to form an ordered crystalline structure on the substrate (Fig. 2.14). Crystallization takes place during drying stage of the film after solution-deposition processes, such as spin-coating or printing, and improves the charge transport (mobility) significantly [23]. However, if the side chains are too long they degrade the π-π orbital overlap by increasing the distance between polythiophene chains (Fig. 2.15).
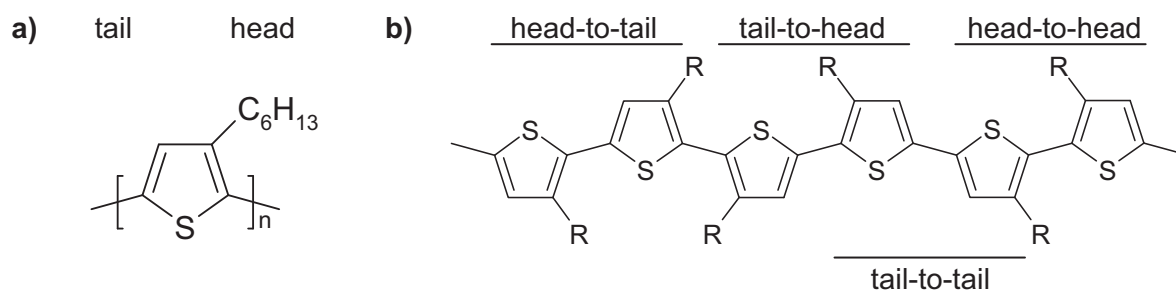
Figure 2.13 (a) Molecular structure of P3HT and (b) different regioregular configurations [37].

Poly(3-hexylthiophene) (P3HT) is one of the most intensively studied soluble organic semiconductors for transistor applications. P3HT offers good solubility in organic solvents, possibility to produce at high purity, good film-forming properties, and although highly surface and process dependent, good electrical properties. On the other hand, P3HT's sensitivity to oxygen, light and humidity makes a special encapsulation of the devices necessary. In the mean time a wide variety of other semiconductor materials have been synthesized which exhibit improved air stability. However the well established physical and electronic properties make P3HT still a very attractive material for research and even real application purposes. P3HT can be found in isotactic and atactic configuration. It is discovered that the amount of crystallinity increases with increasing percentage of isotactic part in the polymer, which improves electrical properties.
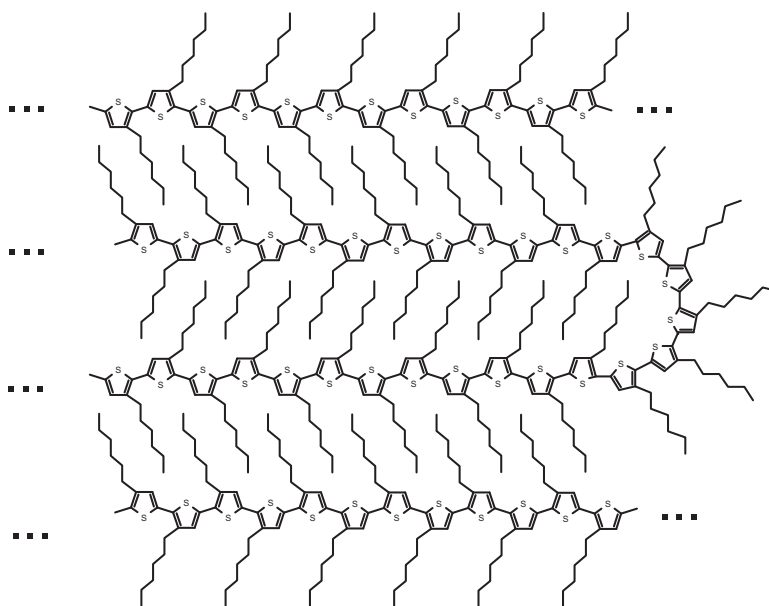
Figure 2.14 Ordered lamellar structure of poly(3-hexylthiophene) in a crystalline region.

The pioneering work on organic devices with soluble semiconductors was presented by Assadi and coworkers in 1988 [71]. A regiorandom P3HT was used in this study, exhibiting mobility values around 10^{-4} cm^2/Vs. In 1996 Bao and coworkers deposited a soluble regioregular P3HT by spin-coating from different solvents on SiO$_2$ gate insulators and showed higher performance devices with mobilities of up to 0.045 cm^2/Vs [72]. This value was comparable to those of vacuum evaporated thiophenes, which indicated an improved charge transport due to enhanced π – orbital overlap. By means of a transmission electron diffraction study they observed strong crystalline ordering in P3HT layers, which was caused by the chain interaction due to the regioregular side groups and responsible from the enhanced charge transport. This ordering phenomenon was demonstrated to be depending on used solvents and deposition parameters. The influence of solvent evaporation rate during film-drying phase was related to the ordering in the layers. Sirringhaus and coworkers took the research and understanding on P3HT-based devices one step further and presented improved electrical performance related to the ordering and conformation of the polymer chains [49]. The dependence of mobility on the regioregularity was also examined in this work. Additionally, the researchers achieved the highest performance where the chains took the edge-on conformation on the substrate surface. The way the chains were standing on the substrate has lead to improved charge transport by providing a closer packing of conjugated chains and therefore improving the π-π orbital overlap. With this study the importance of interfaces was become explicit, which attracted the attention of many researchers on interfaces and dielectrics. These phenomena are the topic of section 2.4.

The highest mobility presented for P3HT so far is 0.2 cm^2/Vs, which was measured in very thin, highly ordered layers [73]. Since the early achievements, there has been an intensive research on solution-processed polymeric semiconductors, towards air-stable, high-performance devices. Organic field-effect devices prepared with a wide variety of p- and n-type semiconducting polymers are presented in recent review articles [58]. Solution-processing of transistors has been a particular research topic after all these achievements. Unintentional doping of semiconductor, reproducibility, complex interfaces, threshold behavior, low mobility devices, dielectric layers and high operating voltages are still the electronic aspects under investigation towards potential applications. Some of these topics are discussed and investigated in this thesis. In the following chapter a more detailed introduction about gate insulators, insulator/semiconductor interaction, surface effects, interface engineering and ferroelectric functionalized transistors will be given.
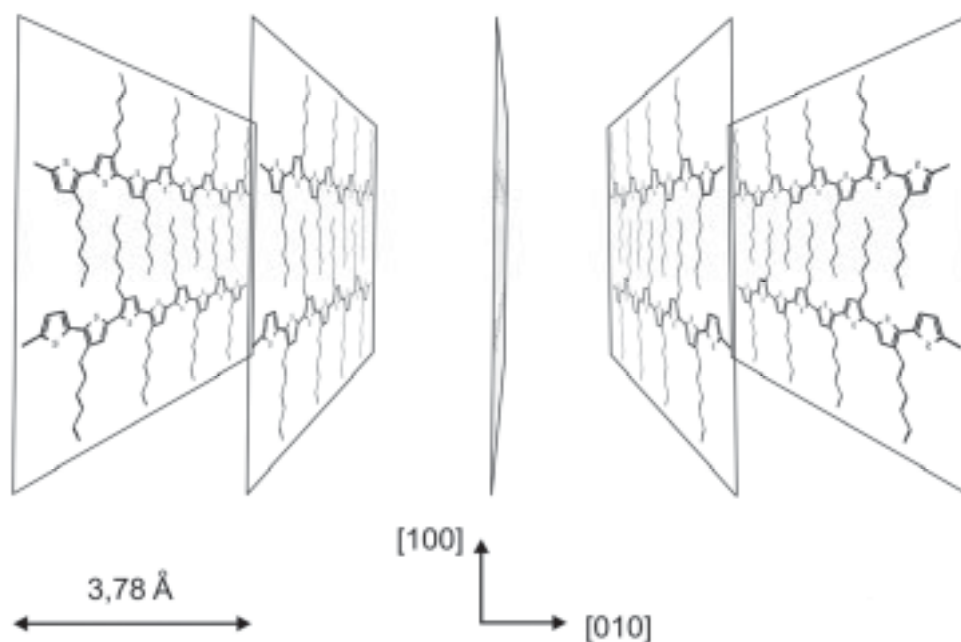
Figure 2.15 3D view of the crystalline structure of P3HT, displaying the π-π stacking.

2.4   Gate Insulators in Organic Field-Effect Transistors

In early 2000's, when the research on organic semiconductors and organic devices was mature enough to allow production of high-performance devices, it was observed that the performance is strongly affected by the dielectric material. From the basic electrical point of view the requirements from a gate insulator for high performance are obvious: The material should possess a high dielectric constant (ε_r) together with a high dielectric strength (E_B) to withstand higher electric fields, expressed by the equations for a parallel plate capacitor,

$$C = \varepsilon_0 \varepsilon_r \, \frac{A}{t} \tag{2.6}$$

$$D_{\max} = \varepsilon_0 \varepsilon_r E_B \tag{2.7}$$

where C is the capacitance (A: area of the capacitor, t: dielectric thickness) and $D_{\max}$ is the maximum charge displacement at the point of electrical breakdown. However, the conditions change when the production techniques, interface effects and the vast variety of organic semiconductors are considered. In multilayer OFET structures, the chemical stability, purity

and interface properties play important roles in device performance. In that sense, a deeper insight into the organic gate insulators is necessary.

The gate dielectric is responsible from the charge accumulation and the formation of a highly conductive channel. In early research on OFETs thermally grown SiO_2 was used as the dielectric. These devices were constructed in bottom-gate configuration where the dielectric also served as the substrate for the semiconductor. Therefore also prealigned, rubbed substrates or monomolecular surface treatments were used to enhance molecular orientation. Hence the tasks of gate insulator were electrical insulation and improvement of semiconductor growth and morphology. The extent that trapped space charges and even molecular dipoles influence the interface charge transport surprised many scientists. The unique charge transport mechanisms make the insulator choice as important as the semiconductor itself. Therefore the role of gate insulator in organic devices turned out to be more complicated than it was thought. Today research on organic dielectrics has become one of the main challenges towards the realization of high-performance applications. There are a wide variety of issues related to gate insulator: Processability, high capacitance, high dielectric strength at low thicknesses, high on/off ratio, hysteresis behavior in electrical characteristics, etc. The optimization of a material for all of the above named parameters is a great challenge for the OFET community.

In the first part of this section 2.4.1, important studies on gate dielectrics are summarized. These studies mostly aim at achieving higher performance devices. Only a part of the studies show simple and inexpensive processing conditions necessary for potential applications. The following section 2.4.2 is about interfaces and related issues in OFETs to present different advantages that are gained by modifying interfaces. Final section will be about spontaneously polarizable gate insulators, mainly ferroelectrics, where the efforts on low-voltage non-volatile OFET memory elements are presented.

2.4.1 Literature Survey: Organic gate insulators

In this part of the thesis various studies are presented to give an idea about the dimensions and diversity of research on gate insulators. Selected studies present only solution-processed gate insulators and therefore demonstrate the possibility of using simple production methods, like printing or casting, for low-cost applications. This will provide the essential perspective to understand the aspects about organic gate insulators.

The first detailed work elaborating on the effects of different polymeric insulators on device properties was reported by Peng et al. in 1990 [74]. Five different polymeric insulators were used in combination with vacuum evaporated alpha-sexithienyl, which were Poly(methyl methacrylate) (PMMA), cyanoethylpullulan (CYEPL), poly(vinyl alcohol) (PVA), polystyrene (PS) and poly(vinyl chloride) (PVC). The polymers were cast on Au-coated glass substrates from solutions of different concentrations. A field-enhanced current was not observed in case of PS and PMMA dielectrics, whereas a very slight enhancement was observed with PVC. Proper I-V characteristics were obtained with PVA and CYEPL dielectrics, with mobilities in the range of SiO_2-based devices. The authors reported a correlation between k values of dielectrics and charge carrier mobility, which improved from $2.1 \cdot 10^{-4}$ (k=3.9) to $3.4 \cdot 10^{-2}$ (k=18.5).

In 1997, Bao et al. employed a polyimide gate insulator and presented a printed high-performance plastic transistor. [75] The dielectric was directly printed on ITO coated polyester substrates, forming gate electrode and the insulator. Semiconductor P3HT and source-drain contacts (conductive ink) were also printed, resulting in devices with mobilities of 0.01-0.03 cm^2/Vs. This was an important study since it showed that completely printed high-performance organic devices are possible.

In 1998 [61] and 2000 [60], Philips group reported all-polymer integrated circuits prepared by using melamine cross-linked PVP gate insulator with a very low thickness value of 250 nm . However, in this work the dielectric did not have to resist solvents since the semiconductors used were vacuum evaporated in bottom-gate devices. Poly (thienylene vinylene) (PTV) and pentacene semiconductors used with polyaniline (PANI) as the electrode material. 15-bit code generators were successfully demonstrated employing several hundred OFETs and vias. The circuits operate even when the substrates are sharply bent.

Semiconductor F8T2 was spin-coated from xylene onto which the 400-500 nm thick PVP gate dielectric was deposited. Finally the top-gate electrode PEDOT:PSS was printed. This was the first completely organic, completely solution-processed organic transistor and exhibited mobility values around 0.01 cm^2/Vs. Via holes were created by dissolving the necessary parts of the dielectric by ink-jet printing of isopropanol in order to produce inverters, which finally operated at frequencies of few hundred Hz.

In 2002, Infineon group elaborated more on PVP dielectrics and optimized the cross-linked polymer, its processing conditions and solvents. Insulating capabilities and dielectric constants of a PVP copolymer and crosslinked PVP were elaborated in details [76]. Very

high-performance pentacene devices employing 280 nm PVP layers, with charge carrier mobility values of up to 3 cm^2/Vs were reported. This important work showed the upper limits of organic devices and set new goals for the OFET community. In the same year Bao et al. introduced a new group of insulating materials to organic electronics world, namely silsesquioxane resins [77]. These materials, in their final-form, present a class between polymers and ceramics, although their precursors are soluble in organic solvents. The low molecular weight precursors have the molecular formula $RSiO_{1.5}$, where R can be hydrogen or alkyl, alkenyl, alkoxy or aryl groups. Later, using the optimized silsesquioxane materials, Rogers et al. demonstrated organic active-matrix backplane circuits with 256 transistors.

Sirringhaus et al. presented another route to low-cost ICs using high-resolution ink-jet printing (IJP) in 2000 [78]. It is the most difficult step to form source-drain electrodes with the desired channel length without using lithographic techniques. This challenge was overcome by using patterned substrates for printing S-D electrodes. Hydrophobic areas were created to define the channel (5µm) where the electrode material PEDOT:PSS did not adhere. Semiconductor F8T2 was spin-coated from xylene onto which the 400-500 nm thick PVP gate dielectric was deposited. Finally the top-gate electrode PEDOT:PSS was printed. This was the first completely organic, completely solution-processed organic transistor and exhibited mobility values around 0.01 cm^2/Vs. Via holes were created by dissolving the necessary parts of the dielectric by ink-jet printing of isopropanol in order to produce inverters, which finally operated at frequencies of few hundred Hz.

Table 2.1 Overview of selected studies on organic dielectric materials for OFETs.

Reference Year	Dielectric Materials	Semiconductor	Remarks (μ values in cm^2/Vs)
Peng et al. 1990 [74]	Solution-processed PMMA, CYEPL, PVA, PS, PVC	Evaporation Sexithiophene (6T)	• Functional devices with PVA and CYEPL. • Permittivity (k) dependent mobility μ: $2.1 \cdot 10^{-4}$ (k=3.9), $3.4 \cdot 10^{-2}$ (k=18.5)
Bao et al. 1997 [75]	Printing Polyimide	Printing P3HT	• **Printed high-performance devices** • μ = 0.01 – 0.03
Philips 1998 & 2000 [60, 61]	Spin-coating Crosslinked PVP t = 250 nm	Evaporation Pentacene	• PANI electrodes • 15-bit code generators were presented
Sirringhaus et al. 2000 [78]	Spin-coating PVP t = 400-500 nm	Spin-coating F8T2	• PEDOT/PSS electrodes • **All-organic, completely solution-processed transistors**, μ = 0.01 • Inverter demonstrated
Infineon 2002 [76]	Spin-coating Crosslinked PVP t = 280 nm	Evaporation Pentacene	• Optimized dielectric processing • **μ = 3.0**
Bao et al. 2002 [77]	Spin-coating Silsesquioxanes	Six different p- and n-channel semiconductors	• Silsesquioxane dielectrics are compatible with different semiconductors • Organic active-matrix backplane circuits demonstrated with 256 transistors
Chua et al. 2004 [79]	Spin-coating BCB **t = 50 nm**	Spin-coating Polyarylamine	• **Low operating voltages (up to 8.5 V)** • High processing T required for BCB
Veres et al. 2004 [29]	Spin-coating PVP, PMMA, PVA, low-k TOPAS	PTAA and F8T2	• Higher device performance achieved with a low-k dielectric • **Discussion: Local polarization effects at the dielectric interface disturb charge transport in semiconductors and cause hysteresis.**
Chen et al. 2004 [80]	Spin-coating Crosslinked PVP with TiO$_2$ nanoparticles	Pentacene (evap.)	• Dielectric constant was increased from 3.5 to 5.4 without affecting mobility.

Table 2.1 Continued.

Reference Year	Dielectric Materials	Semiconductor	Remarks (μ values in cm²/Vs)
Park et al. 2004 [81]	Spin-coating PVP and PVP/PVAc double layer	Pentacene (evap.)	• Hysteresis behavior prevented by using double layer concept • **Discussion: Semiconductor - dipole interaction causing hysteresis results from the bulk of dielectric.**
Park et al. 2004 [82]	Spin-coating PHEMA	Spin-coating P3HT	• Optimization of solvents by examining the solubility parameter • Completely solution-processed high-performance devices, μ = 0.1 • Effect of interface roughness
Fachetti et al. 2005 [30]	Spin-coating Crosslinked polymer blends **t = 10 - 20 nm**	P3HT (spin-coating) Pentacene (evap.)	• Very low dielectric thickness, with very good insulating properties • **Very low operating voltages (1.0 V)**

In 2002, Infineon group elaborated more on PVP dielectrics and optimized the cross-linked polymer, its processing conditions and solvents. Insulating capabilities and dielectric constants of a PVP copolymer and crosslinked PVP were elaborated in details [76]. Very high-performance pentacene devices employing 280 nm PVP layers, with charge carrier mobility values of up to 3 cm²/Vs were reported. This important work showed the upper limits of organic devices and set new goals for the OFET community. In the same year Bao et al. introduced a new group of insulating materials to organic electronics world, namely silsesquioxane resins [77]. These materials, in their final-form, present a class between polymers and ceramics, although their precursors are soluble in organic solvents. The low molecular weight precursors have the molecular formula $RSiO_{1.5}$, where R can be hydrogen or alkyl, alkenyl, alkoxy or aryl groups. Later, using the optimized silsesquioxane materials, Rogers et al. demonstrated organic active-matrix backplane circuits with 256 transistors.

Chua et al. showed that a siloxane based material, benzocyclobutene (BCB), possesses most of the requisite gate insulator properties, in their work in 2004 [79]. BCB was originally developed for interlevel dielectric technologies and sold under the brand name Cyclotene by The DOW Chemical Company. BCB layers presented excellent insulating properties at a very low thickness of 50 nm, which offered the opportunity of manufacturing low-voltage devices. Since it is a crosslinked material, it possessed chemical stability so that further layers could be processed on it. BCB was cured at 290°C for 9 seconds under N_2 atmosphere. Operating

voltages of up to 8.5 volts were used and the devices exhibited mobility values of 10^{-3} to 10^{-2} cm^2/Vs. The most remarkable success of this work was the pin-hole free films at a record thickness of 50 nm. High processing temperatures and sensitivity to oxygen were the disadvantages of BCB precursor.

Veres et al. took another approach and brought a new insight to the researchers by investigating the electrical interaction between gate insulator and semiconductor, in 2004 [29]. It is reported that the local polarization effects can dominate the charge carrier transport by influencing the density of states at the semiconductor dielectric interface. The authors argued that the advantages of using a high permittivity insulator to decrease the operating voltages and increase the mobility are actually limited by these interface effects. Random dipole fields enhance the charge carrier localization at the interface and therefore compensate the advantages of the high-k insulator. These effects were also observed by many other groups as hysteresis effects in the transfer characteristics of devices. In this study poly(4-vinyl phenol) (PVP), PMMA, PVA and the low-k poly(perfluoroethylene-co-butenyl vinyl ether) was used in combination with PTAA and F8T2 semiconductors. Low-k insulator provided optimum results concerning carrier mobility.

The understanding of this interfacial phenomenon has lead to the idea of designing new high-k gate insulators, where local dipoles at the surface are somehow isolated or deactivated and therefore do not affect the semiconductor. Furthermore, it was necessary to investigate this phenomenon in further materials. In 2004, two further studies demonstrated how it can be possible, which are explained in the next paragraphs.

Chen et al. prepared nanocomposite gate-insulators consisting of melamine crosslinked PVP and high permittivity TiO_2 nanoparticles [80]. Oxide particles were dispersed in PVP solutions and 600-700 nm thick layers with oxide wt.-% from 0 to 7.0 were prepared. The measured dielectric constants were 3.5 and 5.4 respectively, whereas the composite layer showed an increased surface roughness value. Surface roughness is proven in another study to have a negative effect on charge transport, since they affect both the semiconductor grain growth and charge transport negatively [82]. Charge carrier mobility values of 0.25 cm^2/Vs and on/off ratios of 10^3 were reported for both kinds of devices. This work was successful in the sense that the nanocomposite layers did not affect mobility, although they consisted of highly polar oxide particles. On the other hand, the on/off ratio was also not improved through nanocomposite layers. This can be attributed to the increased leakage currents through the gate, which increased I_{off} values.

Second innovative work towards hindering the semiconductor-dipole interactions was reported by Park et al [81]. They introduced the concept of "double layer", using two different materials as a single dielectric layer. PVP was used as the dielectric which is in contact with the semiconductor pentacene also in this work. PVP dielectric was already shown to have proper surfaces for pentacene deposition and device operation. However this material combination exhibit hysteresis behavior, which indicates a threshold shift depending on the sweep direction of gate-source voltage. The authors suspect that the charge trapping was cased by oxygen, moisture and ionic impurities which are easily trapped in highly polar matrices. Therefore researchers employed a 1 μm thick layer of lower polarity poly(vinyl acetate) (PVAc) as the main dielectric, which was coated with a 20 nm thick PVP layer on top. Pentacene was deposited on PVP layer in this double-layer dielectric device. Electrical characteristics of this device were compared with those of pure PVP-dielectric and pure PVAc-dielectric devices. In case of pure PVP, an enhanced hysteresis behavior was observed as expected. PVAc devices exhibited no hysteresis, but a lower mobility. The devices with the cooperative double-layer dielectrics showed high mobility values up to 0.1 cm^2/Vs, without any hysteresis. Comparing single- and double-layer devices, the authors concluded that hysteresis behavior is mainly a bulk rather than an interface-related phenomenon. These results have slightly opposed the theory of Veres. et al., but more importantly, showed that there is still much more to understand from the interaction of semiconductors and dielectrics.

Park et al. presented a very interesting study on solution-processed OFETs, introducing poly(2-hydroxyethylmethacrylate) (PHEMA) as gate insulator in P3HT devices, again in 2004 [82]. This study showed that it is possible to produce high-performance devices with simple solution-processable materials, just by a clever materials and solvents selection. The devices exhibited mobility values of up to 0.1 cm^2/Vs and showed excellent threshold behavior, which are normally observed in vacuum evaporated semiconductor devices. P3HT was deposited from three different solvents onto 700 nm thick PHEMA dielectric layers and device properties were compared. Highest mobility values were reached when P3HT layers were drop-cast from toluene solutions and lowest with chloroform. The authors explained this behavior with the solubility parameter. A polymer dissolves in a solvent when its solubility parameter is similar to that of solvent. PHEMA has a solubility parameter of around 29.7 $(MPa)^{1/2}$. It was observed that when the difference between this value and the solubility parameter of P3HT solvent increased (Toluene-18.2, chloroform-19.0), mobility values also have increased. Authors showed that the roughness of semiconductor-dielectric interface

increases when the solubility parameters are closer. Since rough surfaces leads to more defects and voids, the charge transport quality degrades on rough interfaces.

On the search for solution-processable gate insulators a very innovative effort came from Facchetti et al. in 2005 [30]. New polymer blends based on siloxanes and polymers were designed and synthesized. The materials are named as crosslinked polymer blends CPBs and the results of this intensive study were very interesting. They are made up of three different chlorosilane crosslinking agents blended with two polymers (PVP and PS). Presented materials can be spin-coated into very thin films of 10-20 nm, and offer better insulating properties than pure polymer layers, which means that the dielectric strengths of these very thin layers are extremely high. The combination of high capacitance (comes with low thickness here) with high dielectric strength is the desired fundamental insulating property from a gate insulator. Devices were produced both with solution-processed P3HT and evaporated pentacene. P3HT devices were measured with very low voltages but they exhibited only acceptable device properties. Excellent transistor responses were observed from pentacene devices at operating voltages of up to 1.0 V and the hysteresis effects were almost negligible. Dynamic switching characteristics of an inverter were also demonstrated. The authors also investigated the mechanical flexibility of devices, where no significant degradation of transistor response could be observed. This study was very successful in the sense that the self-synthesized materials can be processed from solutions, into such defect-free, robust and very thin layers with excellent insulation properties. Such innovative solutions are very important towards the realization of low-cost all-organic devices.

As it can be observed from this brief literature review, the number of publications exploring gate insulators increased dramatically after 2002. This confirms the importance of research in gate insulators and interface issues.

2.4.2 Interface Engineering in OFETs

Recent technological advances in organic semiconductor devices have accelerated the research on molecular structures and morphologies of organic layers and interfaces that influence the charge transport. There are mainly two interfaces that determine the charge carrier transport in organic field-effect transistors: Dielectric-semiconductor interface, where charge transport and device operation takes place, and the electrode-semiconductor interface, where the charge injection occurs. Therefore these interfaces can be chemically modified by

the functionalization of surfaces and the device performance can be improved significantly. In this section a brief review is given on the recent developments on interface engineering in OFETs.

The major charge transport and transistor operation takes place at the dielectric-semiconductor interface, in the first several molecular layers of the semiconductor. Therefore the physical and morphological state of these interface layers are extremely important. There are two aspects related to this interface. First one is the growth of semiconductor films on the insulator. Charge carrier mobility depends on the molecular orientation of the semiconductor. Highly ordered organic semiconductors exhibit improved mobilities since the molecular orbital overlap is enhanced. Also grain size and the chain orientation play an important role in charge transport. Grain nucleation and grain growth can be influenced by modifying the surface energy of the dielectric. Similarly, the desired molecular orientation (the way that molecules are sitting on the surface) can be obtained by modifying the chemical state and surface energy.
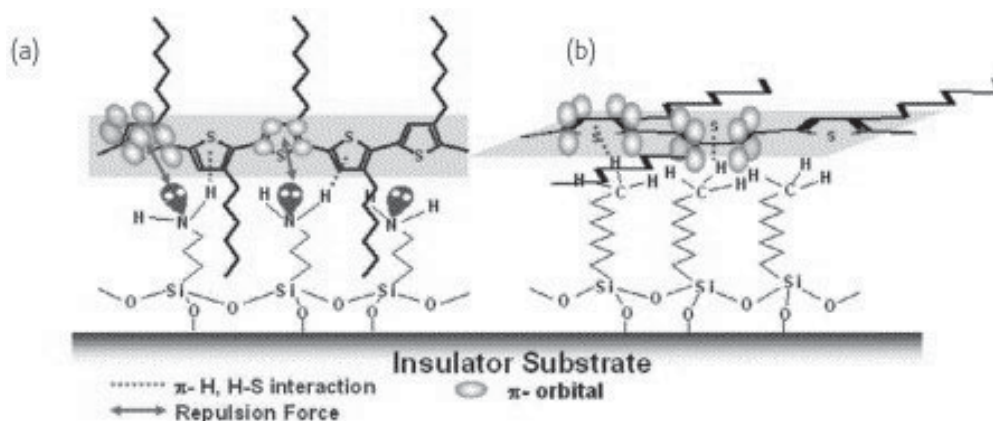
Figure 2.16 Semiconductor P3HT processed on different SAM surfaces take the desired chain orientation and exhibit improved electrical properties: (a) edge-on, (b) plain-on [83].

Second aspect is the initial defect density at the interface [84]. These defects disturb the charge transport either by creating traps or by increasing the conductivity (doping) of semiconductor film. Surface treatment of the dielectric prevents these by creating a suitable surface for film growth and device operation. Typical surface modifications used for OFETs with silicon oxide as the dielectric are orthodecyltrichlorosilane (OTS) or hexamethyldisilazane (HMDS). These materials build a self-assembled monolayer (SAM) on the surface of silicon dioxide and prepare a high-purity, hydrophobic surface.
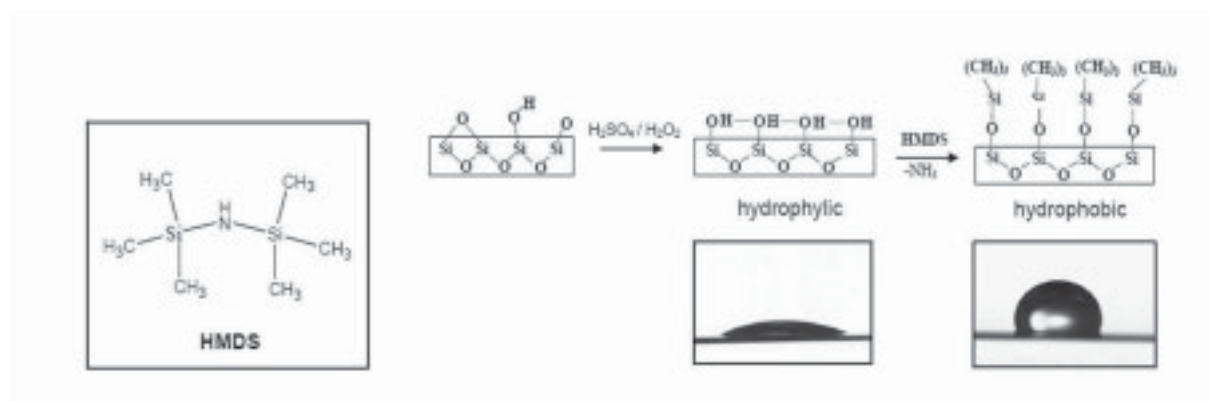
Figure 2.17 Chemical structure of HMDS and the process chemistry of the surface functionalization with HMDS. The surface becomes hydrophobic [85].

The electrode/semiconductor interface has the task of charge injection into the semiconductor. By functionalizing the surfaces, work function of the electrode can be adjusted. This leads to the reduction of contact resistances [86]. Additionally, the ordered growth of semiconductor at the electrode interface can be improved. Organic semiconductor shows better crystallinity with a suitable SAM modification. These materials generally contain thiol (-SH) groups, which form a covalent bond to gold surfaces.

2.4.3   Ferroelectric functionalized OFETs

Ferroelectric materials are electrical insulators which can be permanently polarized due to the presence of internal dipole moments that can change their direction up or down, depending on the sign of an applied field. Ferroelectricity was discovered in 1922 in Rochelle salt (KNa(C4H4O6)·4H2O) [87]. It was discovered that the "electrical properties of Rochelle salt crystal are analogous to the magnetic properties of iron. The dielectric polarization varies with the electric field in the same manner as magnetization varies with magnetic field for iron and showing an electrical hysteresis. The discovery of ferroelectricity in barium titanate (BaTiO$_3$) in 1944 and other ceramics in later years, most notably the lead zirconate titanate (Pb(Zr,Ti)O$_3$, PZT) family of materials, induced a surge in research efforts in this field. These modern ferroelectric materials are now used for a vast array of applications including transducers, acoustic sensors and memory. Additionally, ferroelectric materials are studied extensively for the ferroelectric-paraelectric phase transformation at the Curie Temperature, for the sake of understanding solid-solid phase transformations in materials science [88]. In

OFETs ferroelectrics are used to realize memory elements. In addition to their ferroelectric polarization, most of the ferroelectrics mostly offer high dielectric constant. This makes ferroelectrics and other electrets very attractive for decreasing the operating gate voltages in organic transistors.

There are increasing numbers of studies on memory elements with organic semiconductors; simply by using ferroelectric functionalized gate insulators or electrets [89-96]. Some of these studies demonstrated the possibility of producing low-cost non-volatile memory elements. In these devices memory function is obtained by the bistable polarization of the ferroelectric layer, which spontaneously attenuates the charge density in the semiconductor channel. If such a memory device could be realized by solution-processing techniques that would enable its use in ultra-low-cost applications. One of the major applications is integrated memories. An important example of this is the plastic RF-ID (radio-frequency identification) tag. These tags are small integrated circuits that communicate with a reader via radio communication, to send and receive information stored in its memory. The most important purpose of the plastic tags is to replace bar codes. In order to realize this it is estimated that the price of the plastic tags must come down to a few cents. This is unattainable with traditional silicon technology, whereas it may be possible to realize with low-cost solution-processing techniques employed for plastic devices.

As mentioned above several research groups have demonstrated ferroelectric OFETs successfully, where the gate insulator has high dielectric constant together with the ferroelectric hysteresis. These studies are overviewed in the following section of this thesis. It can be observed from these studies that there is still room for improvement of the devices, especially when the operating voltages are concerned. One possibility to improve device properties, which is presented in chapter 5, is to integrate composite high-*k* ferroelectric composite layers into OFETs.

2.4.4 Literature Survey: Non-volatile OFET memory elements with high-*k* gate insulators

In two pioneering attempts using high-*k* ferroelectric gate insulators with organic semiconductors, the research groups of Dimitrakopoulos et al. (1999) [97] and Velu et al. (2001) [91] presented low driving voltage bottom-gate transistors. They used vacuum deposited organic semiconductors (pentacene and sexithiophene) and inorganic ferroelectric

gate insulators (BaZrTiO$_3$ and PbZrTiO$_3$). In the latter study sexithiophene-PZT transistors were compared with sexithiophene-SiO$_2$ counterparts for lower voltage operation. Although a ferroelectric hysteresis behavior was demonstrated, memory retention test was not conducted. Since the materials were deposited with vacuum deposition techniques the devices were not applicable for low-cost manufacturing of memory devices.

In 2001, Katz and coworkers investigated the polarization effects in four different dielectric materials in combination with organic semiconductors [98]. Two of these materials were particularly hydrophobic electret polymers, which exhibit charge storage characteristics. The work focused on threshold voltage shift in different material combinations, which actually indicates hysteresis behavior. They were able to shift the threshold voltage in several material combinations successfully, whereas the devices were not optimized for further research. They discussed that the charging effect was due to the injected static charges in the dielectric and induced dipoles at the interface.

In 2003, Reece et al. presented a hybrid non-volatile ferroelectric memory element by using the ferroelectric polymer P(VDF-TrFE 70:30) [99]. They successfully employed Langmuir-Blogdett films of P(VDF-TrFE) on n-type silicon substrates, where the silicon was the active semiconductor. 100 monolayer thick P(VDF-TrFE) films showed excellent switching characteristics at ± 15 V applied gate voltage, whereas the memory retention test was not optimized and fully understood at that time. The hybrid devices presented here were also not suitable for simple, low-cost processing of non-volatile memories.

In 2004 three different groups demonstrated memory elements by using organic active layers. Singh et al. demonstrated a non-volatile OFET memory element by using a polymer gate electret poly(vinyl alcohol) (PVA) with a methanofullerene semiconductor (PCBM) [90]. They demonstrated the ferroelectric-like hysteresis behavior and memory retention properties, as well as write/read/erase/read cycles successfully. In this work the spontaneous polarization was obtained by space charge gate electrets with internally trapped charges, instead of ferroelectric gate insulators. Since both of the active semiconductor and insulator layers were processed by spin-coating, these devices offer the possibility of producing low-cost memory devices. Unni et al. demonstrated a ferroelectric memory device by using evaporated pentacene and solution-processed P(VDF-TrFE) layers [94]. Their ferroelectric devices showed a relatively poor hysteresis behavior whereas very good memory retention properties. The third study, by Schroeder et al., presented a non-volatile memory device by using MXD6 as gate insulator [95]. This polymer shows ferroelectric like polarization hysteresis in its

amorphous state, probably due to hydrogen bond alignment, whereas the typical thermodynamic ferroelectric phase and crystallinity can not be observed. The MXD6-pentacene devices exhibited very good hysteresis behavior and retention properties. The latter two studies presented devices that employed evaporated pentacene as the semiconductor. Therefore these devices were not suitable for simple solution-processing of memory devices.

Table 2.2 Overview of selected studies on organic memory elements.

Reference Year	Charge Storage Material	Semiconductor	Remarks
Reece et al. 2003 [99]	Langmuir-Blodgett films of ferroelectric **P(VDF-TrFE 70:30)**	n-silicon	• Very thin ferroelectric layers (100 monolayers) • Low operating voltage • Inorganic semiconductor
Singh et al. 2004 [90]	Spin-coated films of polymer electret **Poly(vinyl alcohol) (PVA)**	Spin-coating Methanofullerene (PCBM)	• **Printable materials were used** • **Very good hysteresis and memory retention properties**
Unni et al. 2004 [94]	Spin-coated films of ferroelectric **P(VDF-TrFE)**	PVD Pentacene	• Poor ferroelectric hysteresis • Very good memory retention properties
Schroeder et al. 2005 [95]	**MXD6 (nylon)**	PVD Pentacene	• Very good hysteresis and memory retention properties
Naber et al. 2005 [93]	Spin-coated films of ferroelectric **P(VDF-TrFE)**	Spin-coating P3HT	• **Printable materials were used** • **Excellent good ferroelectric hysteresis and memory retention properties**
Yildirim et al. 2007 [96] (this work)	Spin-coated nanocomposite films of ferroelectric **P(VDF-TrFE) and BaTiO$_3$**	Spin-coating P3HT	• **Very high permittivity values were reached (k>50) by using printable materials** • Good ferroelectric hysteresis and memory retention properties • **Operating voltages could be reduced by the use of nanocomposite layers.**

In 2005, Naber and coworkers presented low-voltage ferroelectric OFETs by using spin-coated active layers of P(VDF-TrFE) and semiconductor P3HT in a bottom-gate configuration [93]. In this study they optimized the solvents and solution-processing conditions for the P(VDF-TrFE) layer in order to improve its ferroelectric properties. They presented excellent memory retention properties and ferroelectric hysteresis behavior. This work, together with the efforts of Singh et al., showed that it is possible to process low-cost organic memory elements by simple solution-processing techniques.

The research on organic non-volatile memory elements reached such a state that research groups are presenting device properties like memory retention time and hysteresis behavior. Just like in case of OFETs the research on memory behavior is focusing more and more on devices using printable materials.

3 Hybrid Organic Field-Effect Transistors

Organic transistors are named as "hybrid" when they are made up of a combination of organic and inorganic materials. In this part of the work hybrid devices built on silicon wafers (Si-SiO$_2$) substrates are presented. Source, drain and gate electrodes are made of gold. Surface of silicon dioxide is modified with a self-assembled monolayer (SAM) for good interface with the semiconductor. Inorganic materials used in hybrid devices offer optimum surface properties, are chemically very stable and offer reliable electrical performance. Therefore hybrid OFETs are very suitable tools to characterize organic semiconductors electrically. The performance of the transistor is limited by the semiconductor since inorganic materials are known to exhibit reliable properties. Therefore any variations in transistor performance give important information on the chemical and physical states of the semiconductor.

The results and understanding gained from hybrid devices help both to improve the properties of semiconductor films and to understand the measurement and evaluation of organic transistors. Since organic devices exhibit quite different characteristics with changing configuration, materials and measurement conditions, hybrid transistors could be used as reference devices. By using these guidelines, it is easier to evaluate all-polymer transistors.
In the experiments with hybrid transistors, poly (3-hexylthiophene) (P3HT) was used as the semiconductor. Several series of experiments were conducted. In each series, one parameter was altered in order to examine the influence of different factors on transistor performance. The experimental work following the section "Materials and Methods" concentrate on these particular series of experiments:

1. Effect of HMDS-priming of dielectric surface
2. Annealing time of semiconductor
3. Different solvents for P3HT
4. Interaction of P3HT transistors with ambient atmosphere
5. Device configuration: channel length L, channel width W, dielectric thickness
6. Semiconductor purity

3.1 Materials and Methods

3.1.1 Silicon wafers and electrodes

Silicon wafers of 3 inches size (CEMAT Silicon S.A.), with a thermally grown oxide layer, were used as substrates for hybrid transistors. Thickness of the oxide layer was 300 ± 10 nm, which functions as the gate dielectric. N-doped silicon serves as the gate contact.
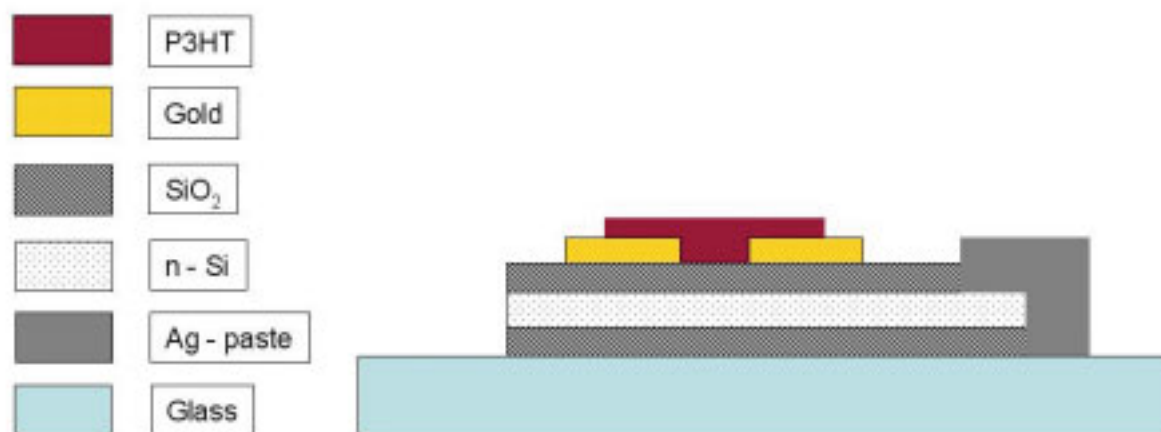
Figure 3.1 Schematic structure of a hybrid organic field-effect transistor.

Source and drain (S/D) electrodes were evaporated onto silicon wafers by electron-beam deposition (EBD). To define transistor channel, a simple shadow mask was used. Aluminum shadow mask had many holes of size 2 to 8 mm, in the middle of which a platinum wire of 26μm was placed. The Pt wire defines the channel length in the transistors. Therefore, the deposited S/D electrodes were rectangles with side lengths of 2 mm to 4 mm. They form a channel of length 26μm and width 2 mm. Electrodes on Si-wafers or glass substrates consist of two layers: a 5 nm thick adhesion layer (chromium) at the bottom and 30-50 nm thick gold layers on top. Leybold L560 was used for the electron beam deposition of chromium and gold layers.

3.1.2 HMDS priming of wafers and contact angle measurements

HMDS-treatment of the surface was conducted by a simple evaporation process. HMDS was condensed onto the wafer from vapor phase, after the preparation of SiO_2 surface (hydrogen termination). Evaporation took place in an air-tight chamber without vacuum. The contact angle of the SiO_2 surface with water was measured before, during and after the HMDS-processing. It was expected that SiO_2 surface first gets hydrophilic, due to hydrogen termination by ammonia, and then hydrophobic after final HMDS deposition. Measurements were conducted by using an EasyDrop® Contact Angle Measurement System in the Institute of Microsystem Technology at the Hamburg University of Technology. Measurement principle was as follows: A small water droplet is placed onto the surface of the sample and a picture is taken from the side. Then, the angle between the substrate-droplet surface and the tangent to the water-air boundary is measured through image processing. (Fig. 3.2) Here, the droplet should be as small as possible since big droplets will be flattened due to the force of gravity, changing the measured angle.
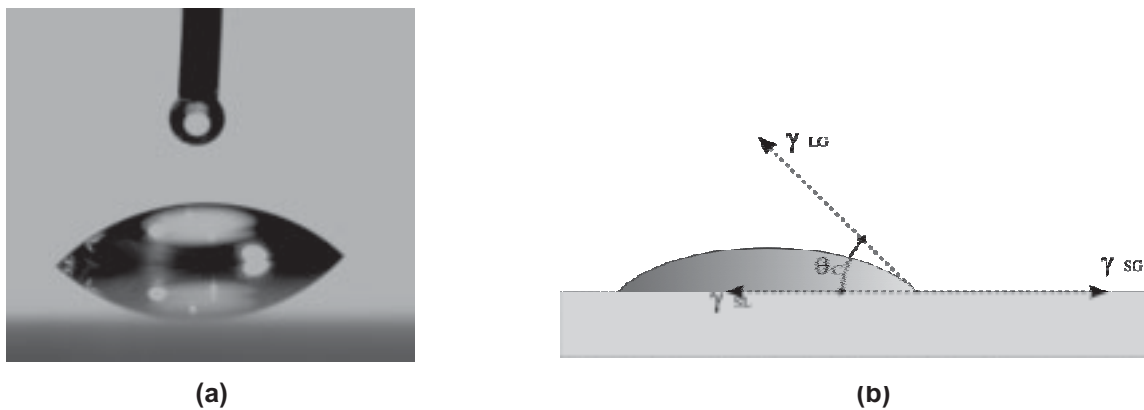

(a)   (b)

Figure 3.2 HMDS – priming of a SiO_2 surface (upper picture). Contact angle measurement. (a) Photo used by the image processing software for measurements. (b) Sketch showing the contact angle θ_c.

Detailed processing steps used for the HMDS-priming were as follows:

1. Preparation of SiO_2 surface: 3 inch wafers with the S/D electrodes were cut into discrete devices, each piece having 1 pair of S/D electrodes. These substrates were cleaned with acetone in ultrasonic bath for 5 minutes and then in isopropanol for 1 minute. After that, they were washed in de-ionized water, blown with nitrogen and dried on a hot-plate at 100ºC. At this step, surface contact-angle with water was measured as 52º. Next, samples were dipped in an ammonia solution (25% water) for 15 minutes where the solution was mixed slightly. The samples were then sonicated in isopropanol for 1 minute to remove the rests of ammonia solution. Right after that, the samples were rinsed with water and dried. With this process, SiO_2 surface was **hydrogen-terminated**, where it becomes hydrophilic with a measured water contact-angle of 25º. The samples were finally ready for HMDS exposure.

2. HMDS-treatment of wafers: Samples were placed on a hot plate which was covered with aluminum foil. Hot-plate was heated to 100ºC for 5 Minutes. Around 5 drops of HMDS was put into a small bowl which was then put next to the samples on the hot-plate. Hot-plate was covered with a bigger glass bowl right after placing the HMDS-bowl, where the sides were sealed air-tight with a tape. Heated HMDS started to evaporate and built vapor on the samples. After 15 minutes of exposure, hot-plate was turned off and cooled down before opening the cover.

3. Removal of HMDS-rests: As explained in the literature review in this thesis, HMDS molecules bind themselves chemically onto the surface of SiO_2. However, during the HMDS exposure additional molecules are also placed on the HMDS monolayer, which is bonded on the SiO_2. Excessive molecules adhere by weak physical forces and therefore could be removed by simple washing. For that reason, treated samples were washed with chloroform to get rid of the residue. Whenever this step was not applied, there were adhesion problems of semiconductor polymer. After this process, the contact angle with water became 80-85, which indicates a hydrophobic surface.

3.1.3 Solution-Processing of P3HT

<u>P3HT</u>

In this work two different P3HT from two producers were used:

1. Rieke Metals Inc. (~1% Zn salt)
2. Merck-Darmstadt

   <u>Physical Properties</u>

   Mn: 10600, Mw: 21200, Tm: 209 ºC

   Regioregularity (by ^{1}H NMR): 93.7

   Residual Analysis (ppm): Na: 1.5, Mg: 0.6, Ni: 13

Although the chemical structures of both polymers were the same, they differed first of all in purity. Therefore both materials delivered quite different semiconductor properties which are further discussed in section 3.2.6.

<u>Solvents</u>

During the production of hybrid OFETs there are various solvents involved in different stages of the process. Solvents are necessary during cleaning of Si-wafers, HMDS-treatment of the surface, dissolving and spin-coating of semiconductor and for the purification of P3HT. Solvents used to dissolve the semiconductor should be of very high purity, since the impurities could be detrimental to the electrical properties of P3HT. The impurities may act as dopants or even charge carriers themselves, or they interact with the charge carriers and affect charge carrier mobility. Therefore, highest purity grade solvents were used for this purpose.

<u>Spin-coating of P3HT on Si-wafers</u>

Solutions of P3HT were prepared and spin-coated in a glove-box under nitrogen atmosphere, since P3HT is sensitive to oxygen and humidity. Solutions were deposited with different spin-parameters according to the desired film-thickness and the viscosity of the prepared solutions. Parameters ranged between 1000 and 3000 rpm, which gave thickness values between 30 to 50 nm. After spin-coating, films were dried and annealed on hot-plate in the glove-box, under a vacuum of -1 mbar. Relationship between spin-parameters vs. film-thickness was

determined for every solution, where a Dek-Tak surface profilometer was used to measure the thickness and roughness of polymer films.

3.1.4 Measurement and Evaluation of Transistors

Agilent 4156C semiconductor parameter analyzer was used for the measurements. With this equipment it is possible to apply up to 100V to all 3 semiconductor measurement units and measure electrical currents as small as 50 pA with high precision, from all 3 lines simultaneously.
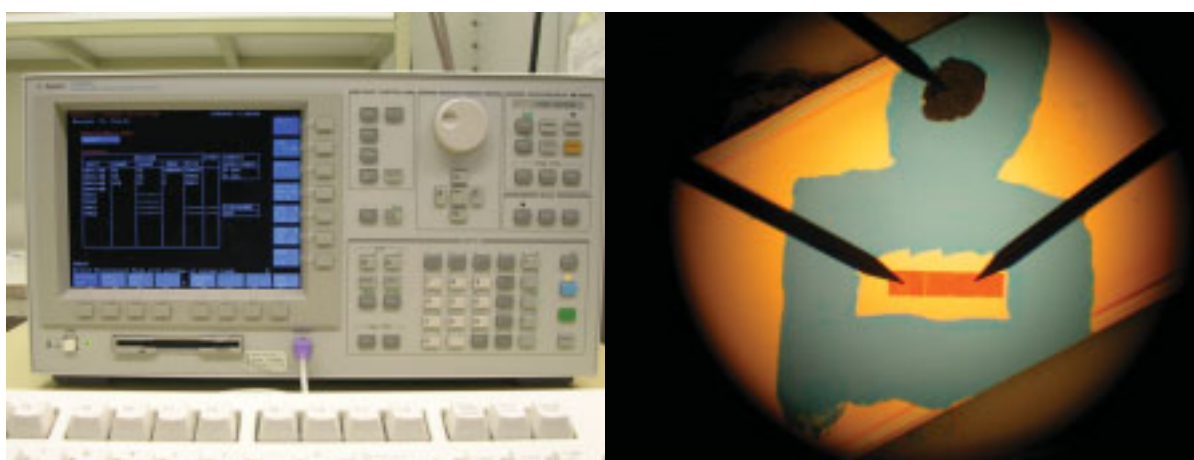

Figure 3.3 Pictures of semiconductor parameter analyzer (left) and a hybrid OFET during measurement (right).

Three different measurements were taken successively from hybrid devices; output characteristics (I_D vs. V_{DS}), transfer characteristics (I_D vs. V_{GS}) and the direct determination of the threshold voltage from $I_D^{1/2}$ vs. V_{DS}. Up to 100 V were applied for the measurements, which did not create any leakage problems in hybrid transistors. Charge carrier mobility, in linear and saturation regimes; subthreshold slope and I_{on}/I_{off} current ratio were the other parameters calculated from the measured electrical characteristics.

3.2 Production and Characterization of Hybrid Transistors

Silicon wafers were coated with Cr/Au electrodes via shadow mask, by electron beam deposition. The wafers with gold electrodes were cut into small pieces, about 2x3 cm size, where every piece had an S/D electrode pair. After deposition of S/D electrodes, the wafers were cut into pieces with a diamond. Every transistor was coated with the semiconductor in

discrete spin-coating steps, to test the reproducibility of the transistors. The last step before deposition of semiconductor was the preparation of the gate contact. This was done by mechanically removing the oxide layer at one place on the wafer and placing a drop of silver paste at that point.

Substrates with interdigitated electrode structures (supplied by Philips Research Eindhoven) with different W/L ratios and with thinner oxide layers were also used in this work. As expected, both the shape of the electrodes and the thickness of oxide layer affected the transistor performance dramatically. These effects are also discussed in a particular section. However, the aim of this work was to improve the device characteristics by developing organic semiconductor films and interfaces.

3.2.1 Effect of dielectric-semiconductor interface: HMDS-coating

In this set of experiments the aim was to investigate the effects of HMDS-priming of SiO_2 surface on transistor properties. As discussed in chapter 2.2.6, improved device properties were expected due to the improved crystallinity of P3HT-polymer and well-defined interface. In order to have statistically reliable results, 10 transistors without HMDS-priming were compared with 9 transistors with HMDS-priming. The samples were prepared as described in the previous section. P3HT solutions of 0.4 % in chloroform were spin-coated and the films were annealed overnight under vacuum.

Table 3.1 Transistor parameters measured or determined from devices without HMDS-priming.

Sample	Linear Mobility (cm^2/Vs)	Saturation Mobility (cm^2/Vs)	Subthreshold Slope (V/dec)	Threshold Voltage (V)	I_{ON}/I_{OFF}	W (mm)
T1	7.01×10^{-5}	7.66×10^{-5}	-59	40.00	23.23	1.3
T2	4.46×10^{-5}	9.98×10^{-5}	-54.6	23.46	225.38	1.5
T3	8.03×10^{-5}	9.26×10^{-5}	-20.38	13.83	280.98	1.5
T4	5.81×10^{-5}	7.07×10^{-5}	-19.31	12.59	174.80	1.4
T5	6.82×10^{-5}	7.35×10^{-5}	-27.92	17.17	209.32	1.5
T6	7.50×10^{-5}	8.61×10^{-5}	-18.98	14.22	330.07	1.4
T7	2.77×10^{-5}	2.76×10^{-5}	-132.99	74.40	6.14	1.3
T8	4.86×10^{-5}	5.56×10^{-5}	-44.66	35.27	100.12	1.3
T9	4.26×10^{-5}	5.52×10^{-5}	-54.02	31.92	85.90	1.4
T10	1.89×10^{-5}	5.7×10^{-5}	-27.82	17.26	149.61	1.3

Table 3.2 Transistor parameters measured or determined from devices with HMDS-priming.

Sample	Linear Mobility (cm^2/Vs)	Saturation Mobility (cm^2/Vs)	Subthreshold Slope (V/dec)	Threshold Voltage (V)	I_{ON}/I_{OFF}	W (mm)
TL1	2.05×10^{-4}	2.23×10^{-4}	-26.03	10.41	571.51	1.8
TL2	2.69×10^{-4}	3.18×10^{-4}	-21.39	14.58	731.82	2.0
TL3	2.97×10^{-4}	4.73×10^{-4}	-20.58	16.72	691.51	1.7
TL4	3.14×10^{-4}	1.01×10^{-4}	-29.70	3.99	602.16	1.7
TL5	1.94×10^{-4}	2.33×10^{-4}	-33.33	14.76	407.33	1.9
TLL1	6.21×10^{-5}	1.02×10^{-4}	-22.30	2.55	277.51	2.0
TLL2	2.45×10^{-4}	3.07×10^{-4}	-24.54	-13.39	609.62	1.9
TLL3	2.91×10^{-4}	3.45×10^{-4}	-19.20	-0.23	517.24	1.8
TLL4	5.03×10^{-4}	5.85×10^{-4}	-19.12	-4.83	843.93	2.0

<u>Mobility:</u> Average value for linear-region mobility increased from 5.3×10^{-5} cm^2/V.s to 2.9×10^{-4} cm^2/V.s., and for saturation-region mobility increased from 6.8×10^{-5} cm^2/V.s to 3.2×10^{-4} cm^2/V.s. This is a slight increase. A greater improvement in mobility was not possible in this case, since chloroform was used as solvent for P3HT. Chloroform evaporates in 3-5 seconds during spin-coating, therefore the polymer chains do not have time to orient them and increase crystallinity.

<u>On/off current ratio:</u> Average value for I_{on}/I_{off} increased from 158.5 to 583.6. On-currents increased due to the improved mobility and off-currents decreased. In order to explain the latter, several factors come into question: Purity of semiconductor and semiconductor/dielectric interface, semiconductor film-thickness, conductivity (doping-state) of semiconductor and measurement conditions. In this study, purity of semiconductor, film-thickness and measurement conditions were not altered. Therefore, it can be concluded that interface purity and conductivity were the responsible factors. Surface of a silicon wafer is classified as a surface with certain amount of defects and impurities on the microscopic level. Devices are working at a molecular level and additionally, the semiconductor is extremely sensitive to chemical and physical states of its surroundings. Improvement in device properties by HMDS-treatment is therefore explained by the modified growth of semiconductor films and by the reduction of initial defect density at the interface [84]. These factors lead to the improvement in off-current.

<u>Threshold voltage:</u> Decreased from +27.8 V to +4.9 V. Since P3HT is a p-type semiconductor, a negative voltage should be applied to turn on the devices. Since organic transistors are "normally-on" devices, threshold voltage is desired to be either negative or close to zero. With help of HMDS-priming it was possible to shift the threshold value to values that are very close to zero.

<u>Reproducibility:</u> Surface treatment increased the reproducibility drastically. Threshold values changed between 12.5 V and 74 V without any surface treatment. HMDS-primed transistors, on the other hand, showed threshold values from -14 to +16 V, which are quite stable values for organic transistors.
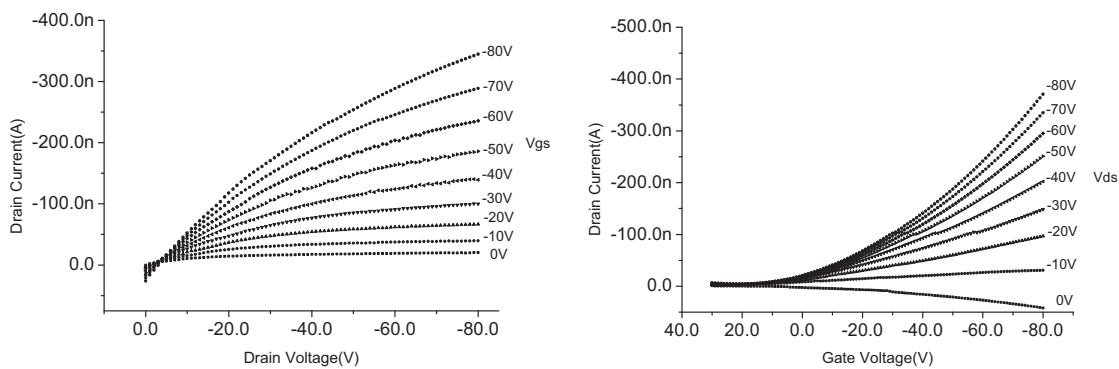

Figure 3.4 Exemplary transistor characteristics of an OFET without HMDS treatment.
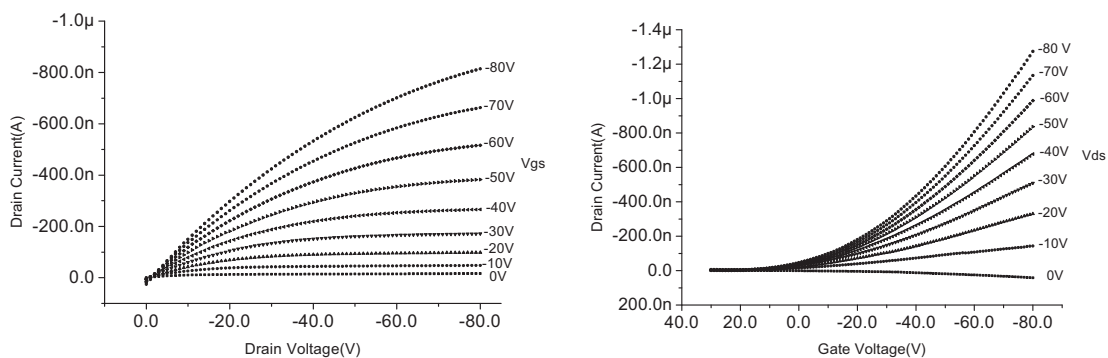

Figure 3.5 Exemplary transistor characteristics of an OFET with the HMDS treatment.

3.2.2 Effects of annealing time of semiconductor

In this part, effects of extended semiconductor annealing time on device properties were investigated. Extended annealing time under vacuum leads to following improvements:

1. Semiconductor crystallinity increases, therefore mobility increases.
2. Unintentional doping is reduced, as a result of which the off-current decreases, and therefore on/off ratio is improved.

18 transistors were produced similar to section 3.2.1, using HMDS-treatment. After spin-coating of P3HT they were annealed under two different conditions:

1. 150°C for 90 minutes under vacuum.
2. 150°C for 24 hours under vacuum.

Following tables present the determined transistor parameters.

Table 3.3 Transistor parameters measured and determined from devices with HMDS-priming, which were annealed for 90 minutes.

Sample	Linear Mobility (cm^2/Vs)	Saturation Mobility (cm^2/Vs)	Subthreshold Slope (V/dec)	Threshold Voltage (V)	I_{ON}/I_{OFF}	W (mm)
TT1	1.44×10^{-4}	2.82×10^{-5}	-26.68	17.4	175.92	1.7
TT2	4.37×10^{-5}	8.17×10^{-5}	-42.05	7.04	190,83	1.7
TT3	8.45×10^{-5}	1.22×10^{-4}	-30.96	10.12	249,41	1.6
TT4	3.70×10^{-4}	7.77×10^{-5}	-38.49	1.90	293.96	1.6
TT5	2.35×10^{-4}	2.60×10^{-4}	-34.41	-3.08	405.05	1.7
TS1	5.15×10^{-5}	2.09×10^{-4}	-27.73	-8.63	351.68	1.8
TS2	2.65×10^{-5}	5.19×10^{-5}	-25.18	4.73	174.09	1.7
TS3	1.53×10^{-4}	2.24×10^{-4}	-23.52	-1.46	287.12	1.9
TS4	2.52×10^{-4}	3.50×10^{-4}	-24.6	-5.50	319.11	1.9

Table 3.4 Transistor parameters measured and determined from devices with HMDS-priming, which were annealed for 24hours.

Sample	Linear Mobility (cm^2/Vs)	Saturation Mobility (cm^2/Vs)	Subthreshold Slope (V/dec)	Threshold Voltage (V)	I_{ON}/I_{OFF}	W (mm)
TL1	2.05×10^{-4}	2.23×10^{-4}	-26.03	10.41	571.51	1.8
TL2	2.69×10^{-4}	3.18×10^{-4}	-21.39	14.58	731.82	2.0
TL3	2.97×10^{-4}	4.73×10^{-4}	-20.58	16.72	691.51	1.7
TL4	3.14×10^{-4}	1.01×10^{-4}	-29.70	3.99	602.16	1.7
TL5	1.94×10^{-4}	2.33×10^{-4}	-33.33	14.76	407.33	1.9
TLL1	6.21×10^{-5}	1.02×10^{-4}	-22.30	2.55	277.51	2.0
TLL2	2.45×10^{-4}	3.07×10^{-4}	-24.54	-13.39	609.62	1.9
TLL3	2.91×10^{-4}	3.45×10^{-4}	-19.20	-0.23	517.24	1.8
TLL4	5.03×10^{-4}	5.85×10^{-4}	-19.12	-4.83	843.93	2.0

Mobility almost doubled with extended annealing and achieved mobility values were statistically more stable than those of shorter annealing. It can be observed that the variation between the measured highest and lowest mobility values was smaller in case of extended annealing. On/off current ratio also increased dramatically with extended annealing. The improvement in charge carrier mobility is attributed to increased crystallinity with extended annealing time. The improvement in on/off current ratio is due to the reduction in unintentional doping in the semiconductor. Selected examples of output and transfer characteristics of the devices are presented below (Fig. 3.6, Fig. 3.7).
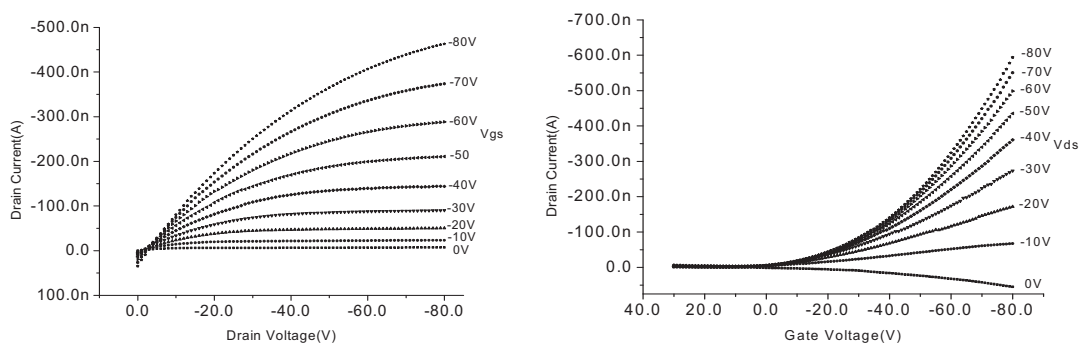

Figure 3.6 Exemplary transistor characteristics of an OFET with short annealing time.
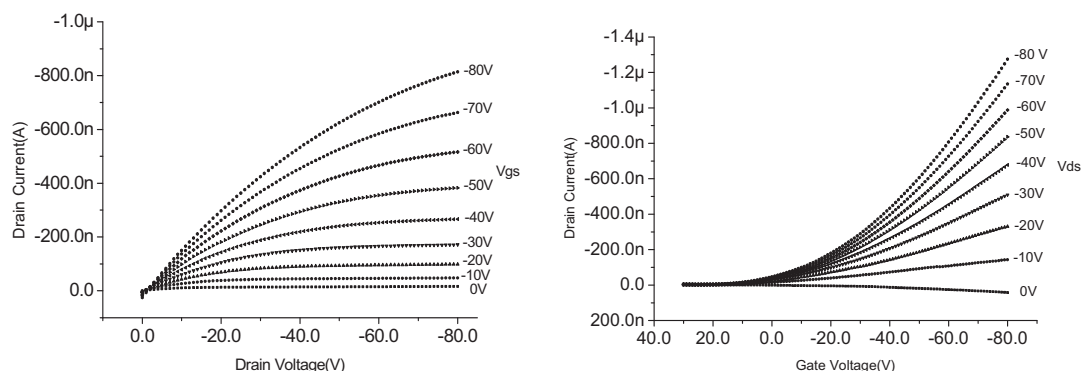
Figure 3.7 Exemplary transistor characteristics of an OFET with long annealing time.

3.2.3   Effects of high boiling point solvents for P3HT

The aim of this study was to investigate the effects of solvents, which were used to dissolve P3HT, on transistor characteristics. As already discussed in chapter 2, growth of semiconductor film takes place during and right after spin-coating. During the drying process, self-ordering P3HT chains start to interact with each other as soon as the solvent starts to evaporate. Therefore the time left for ordering during solvent evaporation is what determines to what extent the semiconductor grains grow [100]. It is known that with increased ordering in the semiconductor π – conjugation overlap is improved, which leads to improved mobility. The following experiments investigate this phenomenon.

Xylene and 1,2,4- trichlorobenzene (TCB) are used as alternative solvents for P3HT. Boiling points of selected solvents were as follows: Chloroform: 61 ºC, Xylene: 132 ºC, TCB: 204 ºC. Therefore, according to the theory, increasing order of field-effect mobility values should be:

$$\mu_{chloroform} < \mu_{xylene} < \mu_{TCB}$$

Results of the experiments are presented in the tables below. Discrete devices, or in average, all mobility values ($cm^2/V.s$) agreed with the order stated above. Here are the measured average mobility values:

$$\mu_{chloroform} = 2.9 \times 10^{-4} < \mu_{xylene} = 5.4 \times 10^{-4} < \mu_{TCB} = 1.3 \times 10^{-3}$$

In addition to field-effect mobility, on/off current ratios were also improved, with respect to chloroform transistors. Instead of an average of 583.6 for chloroform, 1663 for xylene and 1.5 x 10^4 for TCB was measured. With these results, it was confirmed that high boiling point solvents lead to higher performance transistors with P3HT as the semiconductor.

Table 3.5 Transistor parameters measured and determined from devices with HMDS-priming, where high boiling point solvents, *TCB and xylene* were used to deposit P3HT.

Sample	Linear Mobility (cm^2/Vs)	Sat. Mobility (cm^2/Vs)	Subthreshold Slope (V/dec)	Threshold Voltage (V)	I_{ON}/I_{OFF}	W (mm)
TCB1	8.86×10^{-4}	8.63×10^{-4}	-9.12	12.00	2293.57	1.6
TCB2	1.65×10^{-3}	2.53×10^{-4}	10.94	7.88	18695.51	1.6
TCB3	1.3×10^{-3}	1.78×10^{-3}	-5.41	6.71	22135.28	1.7
XY1	5.02×10^{-4}	5.78×10^{-4}	-14.0	17.9	1126.0	1.5
XY2	5.73×10^{-4}	6.25×10^{-4}	-10.43	19.45	2200.91	1.7

Table 3.6 Transistor parameters measured and determined from devices with HMDS-priming, where *chloroform* was used to deposit P3HT, is given once more for comparison. Mobility and on/off current ratio improved significantly.

Sample	Linear Mobility (cm^2/Vs)	Saturation Mobility (cm^2/Vs)	Subthreshold Slope (V/dec)	Threshold Voltage (V)	I_{ON}/I_{OFF}	W (mm)
TL1	2.05×10^{-4}	2.23×10^{-4}	-26.03	10.41	571.51	1.8
TL2	2.69×10^{-4}	3.18×10^{-4}	-21.39	14.58	731.82	2.0
TL3	2.97×10^{-4}	4.73×10^{-4}	-20.58	16.72	691.51	1.7
TL4	3.14×10^{-4}	1.01×10^{-4}	-29.70	3.99	602.16	1.7
TL5	1.94×10^{-4}	2.33×10^{-4}	-33.33	14.76	407.33	1.9
TLL1	6.21×10^{-5}	1.02×10^{-4}	-22.30	2.55	277.51	2.0
TLL2	2.45×10^{-4}	3.07×10^{-4}	-24.54	-13.39	609.62	1.9
TLL3	2.91×10^{-4}	3.45×10^{-4}	-19.20	-0.23	517.24	1.8
TLL4	5.03×10^{-4}	5.85×10^{-4}	-19.12	-4.83	843.93	2.0

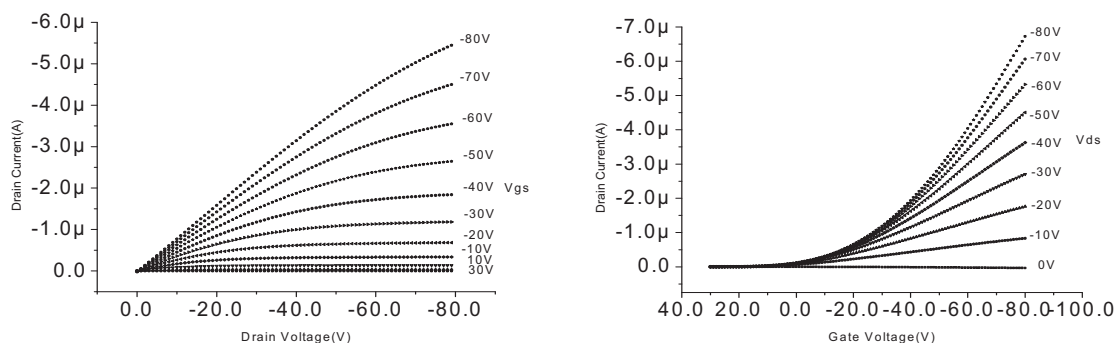Selected examples of output and transfer characteristics of the devices are presented below.

Figure 3.8 Exemplary transistor characteristics of hybrid OFETs, where P3HT was deposited from TCB.
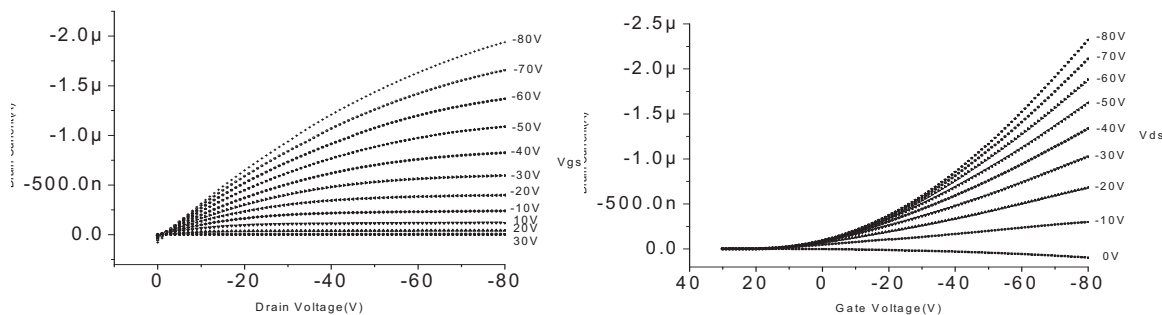

Figure 3.9 Exemplary transistor characteristics of hybrid OFETs, where P3HT was deposited from xylene.

3.2.4 Interaction of P3HT transistors with atmosphere

In this study, sensitivity of the semiconductor P3HT to atmospheric conditions was tested with a series of experiments. Generally, P3HT transistors were prepared and measured in a nitrogen atmosphere glove-box, with humidity and oxygen values around 1 ppm. However, it is essential to observe the reaction of P3HT devices to ambient atmosphere, since potential fabrication processes could take place in ambient conditions.

In these experiments, semiconductor P3HT was spin-coated from chloroform solution and annealed for 1 hour at 100 ºC under vacuum. Then device characteristics were measured. After this, the samples were taken out of glove-box and exposed to ambient air, at approximately 20 ºC and 30% relative humidity, for 24 hours. Device characteristics were taken once more and compared to those taken before the atmospheric exposure.

To understand whether the effects are reversible, transistors were annealed again at 100 ºC under vacuum. The aim was to remove chemically bound or physically adsorbed oxygen and water molecules from P3HT. After this final annealing transistors were measured again. Results of all three stages are presented below: Output and transfer characteristics of transistors at the initial-state, doped-state, and de-doped-state.
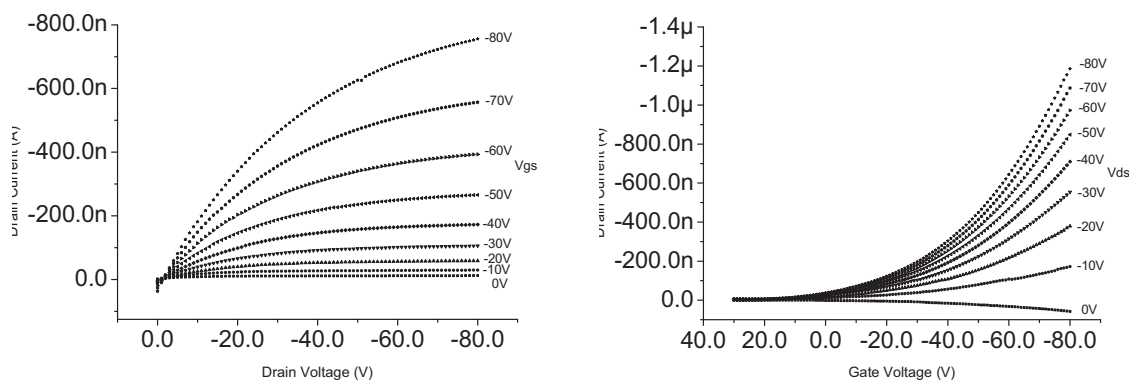

Figure 3.10 Characteristics of devices measured after annealing at 100°C for 1 hour. This transistor showed an I_{off} of 12.07 nA and an I_{on} of 755.55 nA. Threshold voltage was -4.77 V. On/off current ratio was 63.
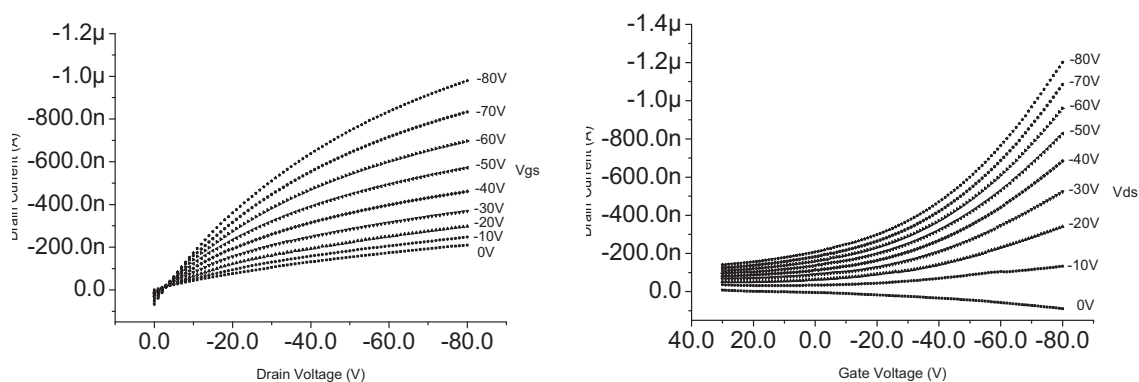

Figure 3.11 The transistor was exposed to ambient atmosphere for 24 hours. It was then realised that the I_{off} was 209.86 nA and I_{on} was 979.16 nA. The threshold voltage also shifted to 21.49 V. These results indicate an increase in conductivity of P3HT, which also means "doping" in the terminology of organic semiconductors. On/off ratio degraded to 5.
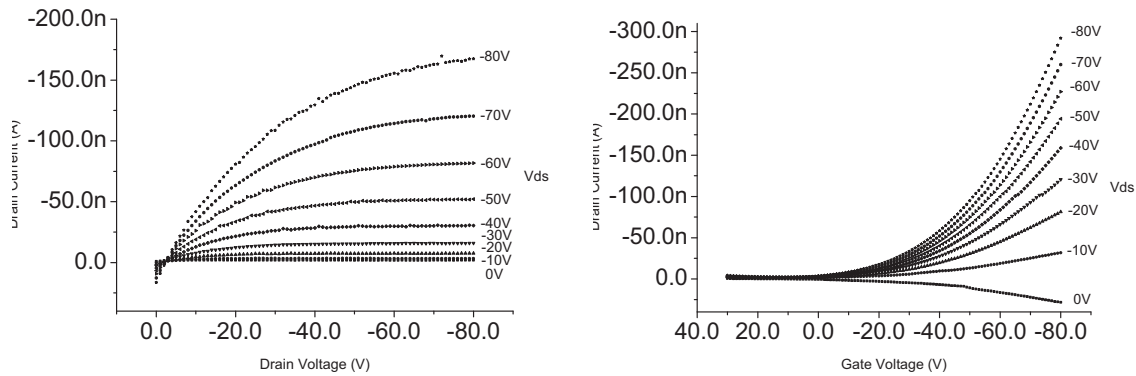
Figure 3.12 Transistor characteristics after the second annealing, de-doping. This time, measured values read I_{off} = 1.85 nA, I_{on} = 167.46 nA and threshold voltage 11.86 V. It was possible to decrease the currents back, but not without a loss in mobility. Output current was lower than the initial state, on/off current ratio improved to 90.

Below, decreasing trend of mobility is presented once more. At this point it makes sense to discuss the interaction mechanisms of P3HT with atmospheric conditions, in order to understand this behavior.

$$\mu_1 = 5,6.10^{-4} \text{ cm}^2/\text{V.s} > \mu_2 = 4,0.10^{-4} \text{ cm}^2/\text{V.s} > \mu_3 = 1,4.10^{-4} \text{ cm}^2/\text{V.s}$$

Interaction of P3HT with oxygen

P3HT based OFETs that are processed in ambient conditions exhibit lower mobility and significantly lower current on/off ratio [101-103]. Most interference from ambient air comes from oxygen. Oxygen can form change transfer complex (CTC) with P3HT. In this case, the π-conjugated polymer P3HT is an electron donor (D), and oxygen with high electron affinity is an electron acceptor (A). Electron donor and electron acceptor forms a weakly bound donor-acceptor complex or CTC as shown in Fig. 3.13 and Equation (2.4). Upon association, the physical properties of the donor and acceptor are perturbed and new properties arise.

$$D \ + \ A \ \Leftrightarrow \ \left[D^{\delta+} \cdot A^{\delta-} \right] \tag{2.4}$$
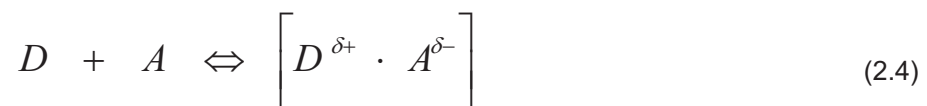
The formation of CTC will introduce more charge carriers (holes) into the bulk of P3HT OFET, thus the increase in conductivity significantly increase the off state current reducing the on/off ratio of the device. The CTC formed between P3HT and oxygen is a weakly bound

complex. CTC can be easily broken down under certain conditions, such as heating in absence of oxygen [101]. However, if oxygen is introduced under exposure to light, oxygen reacts with the polymer chemically disturbing the conjugation, which degrades the mobility [102, 104]. Hence, this kind of oxygen doping is not reversible.
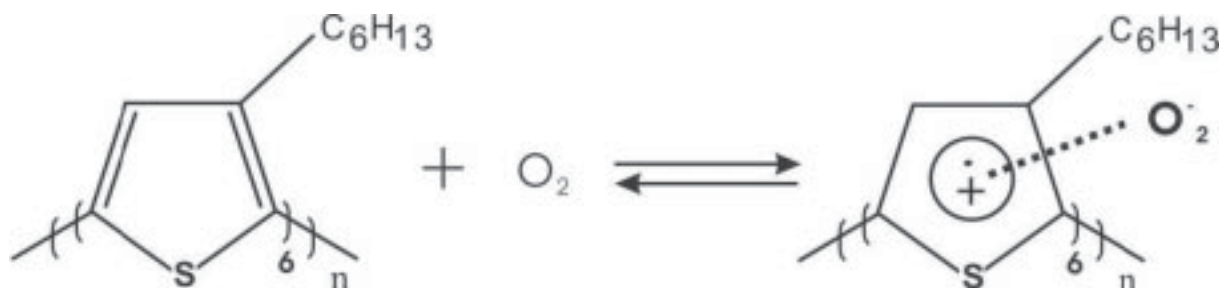

Figure 3.13 Schematic diagram of poly(3-hexylthiophene)-oxygen charge transfer couple complex formation.

3.2.5 Effects of device configuration: Channel length, channel width, dielectric thickness

In this series of experiments effects of device dimensions on transistor characteristics were investigated. New substrates with lithographically structured electrodes were used, which were supplied by Philips Research Eindhoven. There were many electrodes with different shapes (round, interdigitated) and sizes (W, L), and the wafers had an oxide thickness of 60nm. According to equation 3.2 or 3.5, the drain current depends on channel width, channel length and capacitance; where capacitance depends on dielectric constant and thickness of the dielectric. Both in standard test transistors and in new substrates, SiO_2 was the common material for dielectric. Therefore capacitance values could only be affected by the thickness of dielectric. The standard transistors for tests which were reported until this section, dimensions of devices were as follows:

$$W = 1500 – 2000 \ \mu m, L = 26 \ \mu m, \text{oxide thickness} = 300 \ nm.$$

A sample device with following dimensions (will be called as device 2) was selected and compared with the standard transistor, in terms of device characteristics and performance:

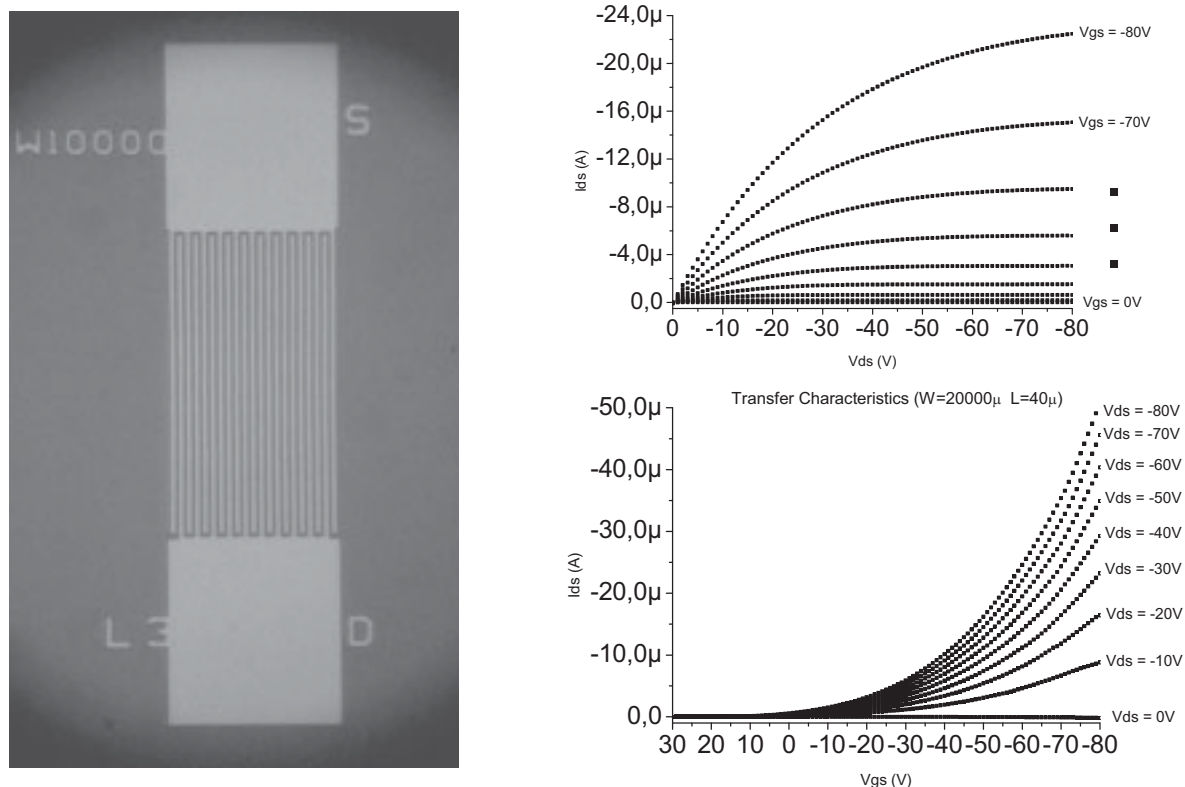$$W = 20000 \ \mu m, L = 40 \mu m, \text{oxide thickness} = 60 \ nm.$$

Figure 3.14 Interdigitated electrode structures (left). Exemplary output and transfer characteristics of a transistor with W=20mm, and L=40µm.

It was possible to reach much higher output currents with the interdigitated electrode structures. Device 2 exhibited a mobility of 10^{-4} cm^2/Vs, which was also reached with the simple devices. Therefore material-related performance, which includes the crystallinity of the semiconductor and interface quality, was the same. There were two simple reasons for the high current output at the same applied voltage: Greater W/L ratio and higher gate capacitance. These size-related effects played also a role in the shape of output characteristics. The devices with complex electrode structures and thinner dielectric showed a more discrete and better saturation of drain current during the output measurements.
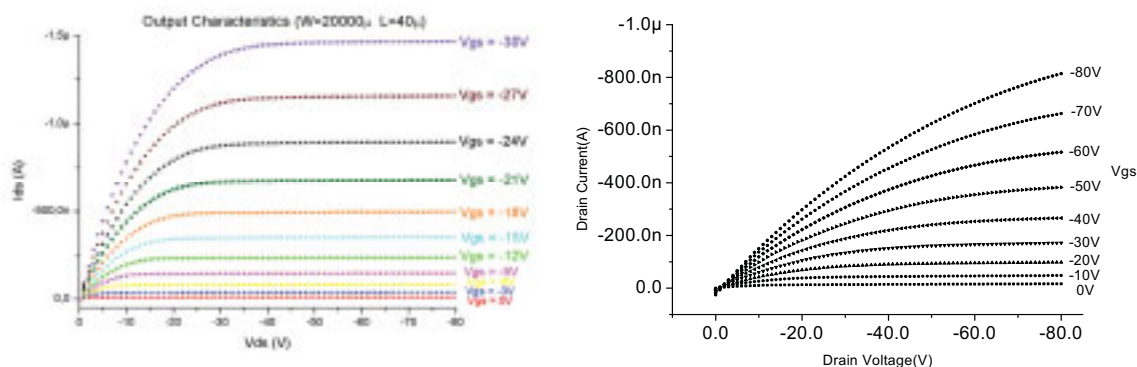
Figure 3.15 Comparison of output characteristics of two hybrid transistors. On the left: t_{ox} = 60 nm, W=20mm, L=40µm. On the right: t_{ox} = 300 nm, W=2 mm, L=26µm.

3.2.6 Effects of semiconductor purity

Chemical purity of the semiconductor is very important for the electrical characteristics of organic devices [105, 106]. Impurities change the electronic structure of organic semiconductors and directly influence the conductivity, which is the basic property or the definition of a semiconductor. An organic semiconductor is expected to have very low conductivity in order to keep the off-current low and the threshold (turn-on) voltage close to zero volts.

There are two kinds of impurities in organic semiconductors: Inorganic rests in the polymer resulting from the polymerization stages, and lower or higher molecular weight molecules [106]. Polymers are such materials whose properties could only be defined for a given molecular weight. That means two polymers of same molecular structure but different molecular weights are two different materials. A typical example is polyethylene; high-density and low-density derivatives show completely different properties. Therefore, the second type of impurities could simply be defined as blending a new material into the semiconductor. Especially the smaller molecules are known to be detrimental to transistor characteristics, since they directly contribute to the conductivity. Different molecular weight parts also affect the ordering characteristics of semiconductor film, therefore the charge carrier mobility. Two different P3HT samples, one low-purity and one in methanol purified, were used in this study. P3HT was purchased from the company Rieke Metals Inc.

Comparison of devices with low-purity P3HT vs. high-purity P3HT

For this set of experiments with low-purity semiconductor P3HT was used as received. For the high-purity set of transistors, the same material was purified by a process called recrystallization or reprecipitation. This process is basically dissolving the polymer in a good solvent and giving the solution very slowly into a non-solvent. As soon as the solution gets into the non-solvent, the polymer will be precipitated out of the solution, which is actually nothing but recrystallization of the polymer. During this process, the impurities in the P3HT and hence in P3HT solution are also dissolved in the non-solvent. In this work, P3HT was dissolved in chloroform (1 wt. % solution) and added drop wise into cold methanol. Finally, the precipitated P3HT was filtered and dried.

Both P3HT samples were dissolved in chloroform, filtered with a 0.2 μm PTFE filter and then spin-coated onto the Si-substrates with electrodes. Samples were then annealed under N_2-atmosphere at 150°C for 2 hours before they were measured.

Electrical Characteristics

Output characteristics of both transistors can be seen in the Fig. 3.16 below. Both transistors have the same configuration; same L, W and oxide thickness. There are two main differences to observe in the output characteristics: First one is that the drain currents are much higher in the P3HT with impurities, both in the off-state and in the on-state. This indicates increased number of undesired charge carriers in the material. Off-current at $V_g = 0$ V shows that the conductivity of impure material is much higher than the pure one. The second significant difference is that, although there was a clear control of the current via gate contact, saturation behavior is completely absent in the device with the non-purified semiconductor. Drain current never goes into saturation, continues to show a linear dependence on drain voltage. This shows that the parallel resistance in the semiconductor was very high. There were too many mobile charge carriers in the bulk film to contribute to the current, acting as a parallel resistance.

As explained before in this section, different impurities act as charge carriers. After the removal of these, by the reprecipitation process, currents decreased tremendously and transistor characteristics come to the expected form, with linear and saturation regions. This work was conducted at the beginning of the project. At that time there were a very limited number of reports investigating influence of semiconductor purity. Later during this study a high-purity P3HT material was purchased.
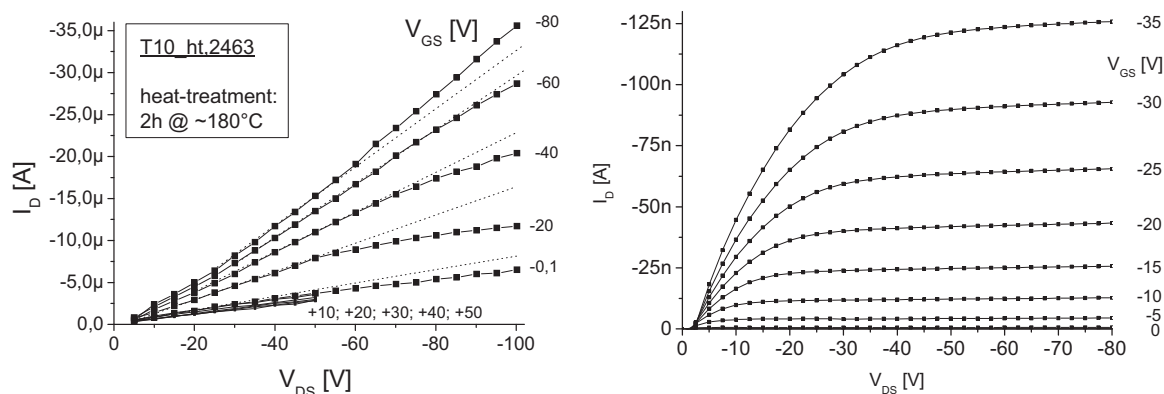
Figure 3.16 Comparison of output characteristics of hybrid devices. On the left: using a non-purified P3HT, on the right: using a purified (recrystallized in methanol) P3HT.

3.3 Conclusion

In this chapter, semiconductor and semiconductor/dielectric interface related factors that influence the performance of hybrid OFETs were investigated. While performance was optimized, methods used for the optimizations also helped understanding the chemical and physical properties of organic semiconductor films.

In section 3.2.1, it was demonstrated how HMDS-priming of SiO_2 surface lead to an increase in mobility, improvement of threshold voltage and reproducibility. Since organic transistors are interface devices it is crucial to have a pure, homogeneous dielectric/semiconductor interface together with optimized semiconductor ordering conditions, to achieve high performance. Dielectric surface treatment not only prepared a better surface for semiconductor ordering but also provided a physically well-defined interface for device operation.

The effect of extended semiconductor annealing time on device performance was observed as improved mobility and on/off current ratio. It was shown that crystallinity and unintentional doping of P3HT could be affected by the duration of annealing. Similarly, solvents used to deposit P3HT affected crystallinity and therefore the device performance directly. Since slower solvent evaporation lets more time for the self-ordering of semiconductor, crystallinity was improved by using high boiling-point solvents like xylene and 1,2,4- trichlorobenzene. The devices presented here showed mobility values up to 2.10^{-3} $cm^2/V.s$ and on/off current ratio of 2.10^5. It was managed to improve mobility without affecting other transistor characteristics like threshold voltage and saturation behavior. In

other words, mobility could be increased without changing the doping significantly. Except HMDS-treatment and usage of high boiling-point solvents, which were applied in this work, it is already known that performance could be further improved by controlled deposition and crystallization of P3HT. Micrometer size single crystals of P3HT can be formed [107]. This can be achieved by a fully controlled solvent evaporation rate, which should occur at a thermodynamic equilibrium.

In section 3.2.4, a simple test procedure was presented to investigate the behavior of P3HT devices under atmospheric conditions. The reaction of P3HT with oxygen and humidity, and the extent of reversibility were tested in terms of device properties. Devices exhibited increased off-currents after exposure the atmospheric conditions, whereas on-currents were not affected dramatically. That means the number of charge carriers increased, whereas mobility values of these were unaffected. In other words, P3HT was doped with oxygen and humidity; therefore its conductivity increased. On the other hand the highest current remained almost unchanged since the accumulated charge carrier dominated the channel current. The doping effect was reversed by annealing under vacuum. However, mobility decreased probably due to destructive interaction of oxygen with P3HT. This study clearly indicates that P3HT systems should be encapsulated towards potential applications.

In the next part of this chapter, devices on complex electrode structures and thinner dielectric films were investigated. P3HT devices exhibited almost ideal output and transfer characteristics with a clear saturation of drain current and switching at much lower voltages. Field-effect mobility of P3HT was not changed since materials were the same. This study showed the importance of electrode structures and dielectric capacitance for device operation. In the last section, a low purity P3HT was used in hybrid transistors, where the excess of charge carriers lead to very high channel currents and poor transistor characteristics. The material was then purified successfully by recrystallization and high-performance devices were demonstrated. The polymer had around 1% Zn ions inside before purification, so it was demonstrated how these contribute to channel current by a factor of up to 10^3. Therefore it is once more shown that an intensive purification of the semiconductor is crucial to achieve high-performance devices.

4 Organic Transistors with Polymer Dielectrics

In this part of the work, four thermosetting polymers were investigated to be used as the dielectric layer in OFETs. SiO_2, which was used in hybrid devices in the previous chapter, was replaced with organic dielectrics. This is one of the most important and difficult steps towards all-organic devices. Similar to hybrid devices, bottom-gate configuration was used for this study. The chapter starts with a detailed materials selection where four different thermosetting polymers were chosen to be tested as gate-dielectrics for OFETs. Selected materials are systematically examined for film-quality, insulation and solvent resistance before they are utilized in OFETs. Metal-insulator-metal (MIM), as well as metal-insulator-semiconductor (MIS) structures are used for further characterization and understanding of electrical properties of devices. Selected materials were used as dielectric layers in P3HT and pentacene transistors. The chapter also includes electrical characterization of devices and comparison to their hybrid counterparts. An all-organic device is also presented in the end of this chapter, replacing gold electrodes with a laser-structured PEDOT layer.

4.1 Dielectric materials for bottom-gate organic transistors

Critical parameters affecting device performance in bottom-gate transistors with P3HT semiconductor are already investigated in the previous chapter. This part of the work aims to select high-performance insulators and process them into thin dielectric films, and finally compare their dielectric performance in OFETs with that of SiO_2. First, a systematic selection of dielectric materials among the organic materials will be presented. In the following sections, critical details of film-processing will be explained and also dielectric properties of the produced films will be investigated.

4.1.1 Constraints for materials selection and candidate materials

Any polymer which can be dissolved in an organic solvent is a potential candidate to be used as a dielectric in OFETs. This brings the advantage of selecting materials from the wide selection of polymers and organics. Therefore, any research group searching for novel devices with different materials has to take the challenge and try to process new materials. This makes the field extremely open to new ideas which were already discussed in chapter 2.

In this research new materials were introduced to organic transistors and materials that were already reported were tested to compare with these novel devices. Materials selection starts by addressing the requirements from dielectric layers in OFETs. Bottom-gate, bottom-contact OFET design was used in this study. The most important difference of a bottom-gate device from a top-gate device is that the semiconductor is deposited onto the dielectric. The dielectric/semiconductor interface, where the transistor operation takes place is defined by this deposition step. Additionally, since the semiconductor is processed from a solvent on the dielectric, dielectric material should be capable of resisting this solvent; without getting dissolved, or swollen. The films and interface formed during this step is the most critical part of production in terms of functionality and performance.
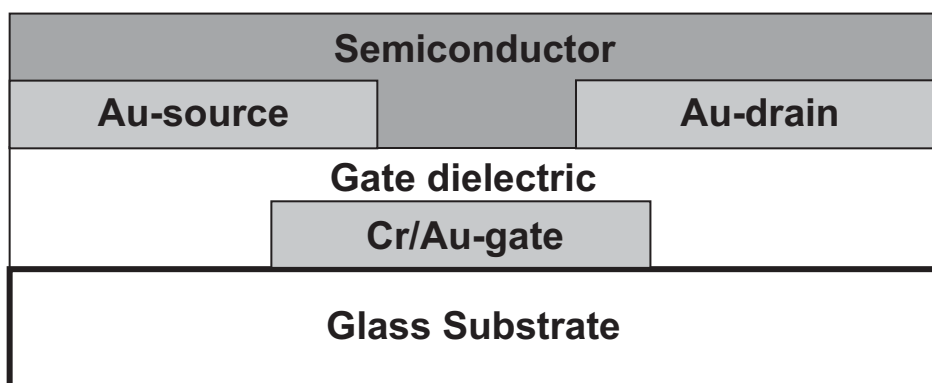

Figure 4.1 Bottom-gate, bottom-contact OFET with a polymer dielectric.

Transistor configuration and layer stacking must be taken into consideration for a systematic materials selection. Glass slides were used as substrates. Gate-electrode, which was made up of Cr (5 nm, adhesion layer) and Au (35 nm), was deposited by electron-beam deposition via a shadow mask. Gate dielectric was then spin-coated onto the substrates, which was followed by the thermal evaporation of S/D electrodes (Au, 30 nm), via another shadow mask. The S/D electrodes were exactly the same as they were in hybrid transistors, therefore L and W values were 26 μm and 1-2 mm respectively. Finally, P3HT was deposited on the electrode structure. Considering this device configuration, six constraints for the materials selection are listed below:

1. Organic, or inorganic, insulator materials which could be solution-processed into smooth and homogeneous thin-films, without any defects or pin-holes.

2. The material should wet the surface and adhere to the surface of the substrate.

3. Deposited films should be insulating, so a certain film-thickness is required. On the other hand, the film thickness should be minimized to lower operating voltages. Minimum film-thickness is limited by the breakdown voltage of dielectric layer. For this study it is essential that the film thickness can be varied simply. The solutions should be capable of forming smooth films of varying thicknesses, i.e. stable solutions should be available in different concentrations.

4. Dielectric films should withstand the solvents used for P3HT, since it will be spin-coated onto the dielectric. This is also critical since a good interface with P3HT is only obtained when the surface of the dielectric is not affected by the solvents.

5. Drying/curing temperature and time should be minimized, to demonstrate fast and simple processing conditions, such as for reel-to-reel printing.

6. Dielectric constant of the material should be as high as possible, to lower the operating voltages by increasing the induced capacitance.

It is possible to find many different polymeric materials that satisfy these conditions. A theoretical selection of dielectric polymer and its solvent would possibly succeed in thin-film production, whereas it can only be suspected that the combination would deliver smooth, defect-free thin-films on required surfaces. It is also difficult to estimate the physical properties of the interface that will be formed between semiconductor and dielectric since it depends on different factors. Previous studies showed that even the materials which were extensively studied could be further optimized for higher performance. The challenges faced in that sense can be listed as follows:

1. Solvent evaporation: Rate of solvent evaporation directly affects film-morphology. This rate depends on spin-coating speed, ambient temperature, surrounding atmosphere, boiling point of the solvent. All of these parameters should be optimized for a perfect film-formation. In addition, the solvent should evaporate completely and leave the film; otherwise solvent residue will degrade the insulating properties of the films, like specific resistivity and breakdown voltage.

2. Extent of solubility of polymer in the selected solvent: During and short after spin-coating, solvent leaves the wet film and the concentration of the wet film starts to increase. Therefore the solubility range of the polymer should be wide enough to

prevent early precipitation of polymer out of solution before film-formation. Otherwise the film-formation will be inhomogeneous and film-quality will be affected.

3. Adhesion and wetting properties of solvent/material combination on coating substrate: The surface to be coated should be wetted by the solution. An aqueous solution, for example, can not be coated on a hydrophobic polytetrafluoroethylene (PTFE-Teflon) surface, without any modification of surface energy. Also the polymer molecules, after drying, should be compatible with the surface in order to build strong adhesive bonds. In case of a flexible application, adhesion is very important.

4. Adhesion of semiconductor on the dielectric: It was already mentioned that dielectric films should be resistant to solvents that are used to deposit semiconductor. On the other hand, surface energies should be compatible so that the solution and the drying polymer should adhere on the surface during spin-coating process. A certain balance should be provided between surface energies of the solvent for semiconductor and the dielectric.

These four factors indicate that the successive deposition of dielectric and semiconductor layers requires a great amount of experimentation and know-how in the field of coatings and formulation. Further points could be added to this list, when the electronic properties of transistors during their operation are considered. For OFETs, however, a successful materials selection could most probably be reached by a systematic experimental study.

Selected Materials

Under these circumstances, four thermosetting polymers were selected and tested for gate insulation purpose in bottom-gate devices. All of the materials deliver smooth films in a range of thicknesses on glass-substrates. Also, since they are all thermosetting polymers, they are not dissolved by solvents once they are completely cured. As discussed in chapter two, thermosets build strong covalent bonds which can not be broken thermally or by standard solvents. Selected materials and their detailed description are presented below:

1. Benzocyclobutene (BCB)
2. SU-8
3. Norland Optical Adhesive, NOA74
4. VP Bectron EL37A

Benzocyclobutene (BCB)

BCB has a chemical name cyclo[4.2.0]octa-1,3,5-triene, is available under the trade name Cyclotene and developed by The Dow Chemical Company. Cyclotene resin is the dielectric material of choice for many applications in the electronic industry because of its low dielectric constant, a low electrical current loss factor at high frequencies, low moisture absorption, low cure temperature, high degree of planarization, low level of ionic contaminants, high optical clarity, good thermal stability, excellent chemical resistance, and good compatibility with various metallization systems. Two of the key advantages of BCB-based polymers are that the curing process does not emit any volatiles and that the products from the BCB ring-opening reaction are nonpolar hydrocarbon moieties.

BCB has already been successfully used in organic transistors as the dielectric layer [79]. Previous research showed that all-polymer transistors with a very thin BCB dielectric layer exhibit good transistor characteristics. However, although it shows very good dielectric properties, BCB is not feasible for the low-cost processing of transistors on plastic substrates due to the need for very high curing-temperature and vacuum or inert atmosphere processing. Important properties of BCB-resin are listed in table 4.1 below.

Table 4.1 Electrical properties of BCB films, given by DOW Chemical Company [108].

Property	Value
Dielectric Constant	2.65 – 2.5 (1MHz – 10 GHz)
Dissipation Factor	0.0008 – 0.002 (1MHz – 10 GHz)
Breakdown Voltage	$5.3 \pm 0.2 \times 10^6$ V/cm
Volume Resistivity	$1 \times 10^{19} \Omega$-cm

SU-8

The SU-8 is a negative, near-UV photoresist based on EPON SU-8 epoxy resin that has been originally developed, and patented by IBM. It is available from the company Microchem Corp. [109]. The photosensitive components in SU-8 only indirectly affect the solubility of the resist, different from other positive photoresists. The photoinitiator triarylsulfoniumhexafluorantimonate is here also called as "Photo acid generator, or PAG". After spin-coating the resist, a pre-bake step is applied at 95 °C, to remove the solvent in the film. The film is then exposed to UV-light, where PAG is transformed into an acid. This acid starts a chain-reaction in the resist, during the final post exposure baking, at 60-150 °C.

Hydrogen ions are separated from EPON molecule and due to the free bonds; crosslinking (polymerization) starts between epoxy molecules.

SU-8 was used as a dielectric in this work, for the first time in organic transistors. Since epoxy resin is known to be an outstanding insulator, proper films of SU-8 are good candidates to be used as gate dielectric layers in organic transistors.

Norland Optical Adhesive 74

Norland Optical Adhesive is a product of the company Norland Products Inc [110]. This optical adhesive is formulated as very low viscosity adhesive for bonding CAB, glass and other plastics. It offers very good adhesion on glass and forms very smooth, thin films by spin-coating. Its chemical ingredients include mercapto-ester, isodecylacrylate, trimethylpropane polyoxypropylene. NOA74 can be cured by a UV-lamp (253.7 nm).

VP Bectron EL37A

VP Bectron EL37A is a modified epoxy resin based coating, developed by the company Elantas Beck [111]. It is available as a solution that can be further diluted or concentrated according to the application. After coating, the solvent leaves the film and the modified epoxy molecules start to react under temperature. EL37A forms very strong films of very high chemical resistivity. This coating material is generally used in electrical machines, in their production or maintenance, to insulate and protect coil windings. In this study it is used for the first time in organic transistors as the chemically resistant gate insulation. EL37A hardens at 160°C in 60 minutes or at 130°C in 4 hours.

4.1.2   Processing of dielectric films and surface properties

Out of four selected insulator solutions the viscosities of BCB (Cyclotene 3022), NOA74 and SU-8 (2), in their original states, were already formulated to process $1.0 - 1.4$ μm thick films at spin parameters ranging from 2000-4000 rpm for 60 seconds. Therefore, they were used as received. EL37A solution was diluted by 35 wt %, where 3.5 units of solvent were added to 10 units of EL37A solution. After spin-coating, the films need to be dried and cross-linked. The required processing parameters for these materials are listed in Table 1.

Film thickness values were determined by a Dek-tak profilometer. Surface energy plays a very important role in semiconductor film formation. Surface energies of dielectrics

were determined by measuring contact angle values of dielectric layers with water and diiodomethane by the method explained in chapter 3. Surface energy values of spin-coated dielectric films were then calculated by the method defined by Owens and Wendt [112]. Results are presented in table 4.1. In the table also the contact angle values of films with water are given, since hydrophobicity is also an important factor that affects semiconductor interface. Values found were as follows: 93 for BCB, 80 for SU-8, 60 for NOA74, 96 for EL37A (see Table 1). Except NOA74, dielectrics generally showed a hydrophobic character, which is an advantage when ambient processing conditions are concerned. A hydrophobic surface could hinder water condensation to some extent, therefore protect the semiconductor/dielectric interface from potential defects or trap states. Trap states are known to affect mobility, as well as threshold behavior, since they alter the doping state of the semiconductor.

Effect of solvents on dielectric surface roughness

In bottom-gate devices, P3HT is spin-coated on the dielectric from different solvents. Therefore in this part of the study, the change in the film quality upon exposure to these solvents was examined. It is expected that dielectric films provide a smooth and defect-free interface to semiconductor. However, the solvents used for semiconductor may affect the film and/or surface quality by dissolving or swelling the dielectric films. This could end up in an improper, defective interface affecting the device characteristics. Soluble species that originate from dielectric films could mix into the semiconductor and form a mixture at the interface. Or roughness of dielectric surface might increase. Both of these could lead to a decrease in mobility and deteriorate the threshold properties
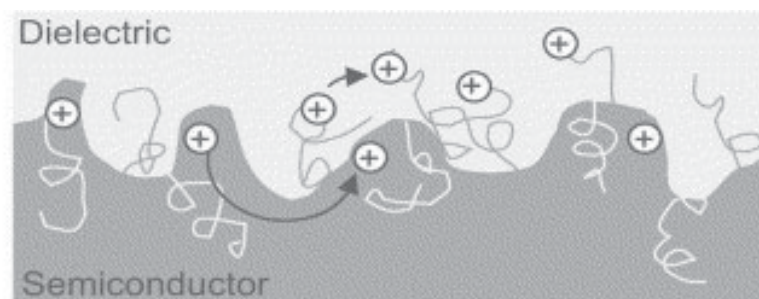

Figure 4.2 Charge carrier transport takes place at the interface between the semiconductor and the dielectric. In this picture the influence of interface mixing and roughness on the charge transport are demonstrated [83].

To determine the surface roughness of polymer films White Light Interferometer (WIM) was used. This technique allows optical 3D investigation of a smooth surface in nanometer precision. It delivers surface scans similar to atomic force microscopy (AFM), much faster and easier. However, the vertical resolution is limited to nanometers, where the AFM can measure even in Angstrom range. Detailed explanation and operation principles of white light interferometry can be found in various references [113-115].

Four different solvents were dropped onto dielectrics to investigate solvent effects: chloroform, 1,2,4-trichlorobenzene (TCB), xylene and toluene. Boiling points of the solvents used to deposit P3HT were as follows:

Chloroform: 61 ºC, Xylene: 132 ºC, TCB: 204 ºC, Toluene: 111 ºC

Film thickness and roughness were measured before and after solvent exposure. Rms roughness of the dielectric films that were measured by WIM before and after the exposure to solvents, generally showed no considerable variation. The films withstand the solvents showing small amounts of variation in the roughness values. Even after prolonged exposure, dielectric films were extremely stable with minimal changes in rms roughness. For example, in case of BCB layer upon exposure to TCB, the rms roughness increased to 3 nm which could be considered as an exception for those samples. Also the peak-to-valley (PV) roughness increased from 12 nm to 48 nm. (Fig. 2) Indicating a slight swelling of the dielectric film during the measurements made on MIM-devices this swelling did not appear to be detrimental to insulating properties. A considerable influence of PV-roughness on device properties was not observed therefore it will not be discussed any further. Below, the WIM investigation screenshots are presented. Complete data of rms and PV roughness values are given in Table 1 in following pages, together with the other measured properties of all films.
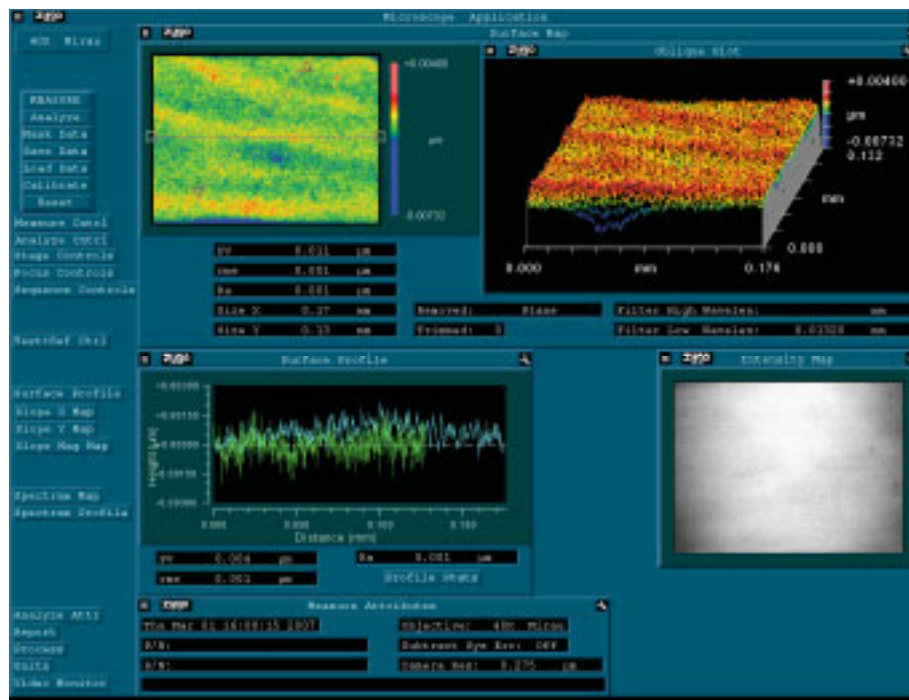
Figure 4.3 Screenshot of a WIM investigation from the surface of an NOA74 film, showing an RMS roughness of 1 nm and a PV roughness value of 11 nm.
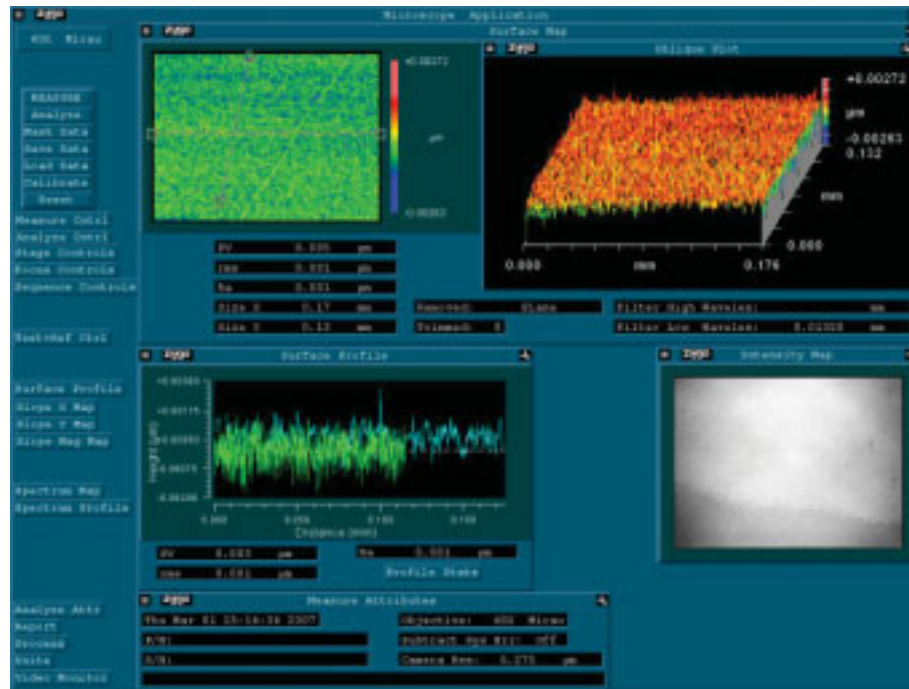

Figure 4.4 Screenshot of a WIM investigation from the surface of an SU-8 film, showing an RMS roughness of 1 nm and a PV roughness value of 5 nm.
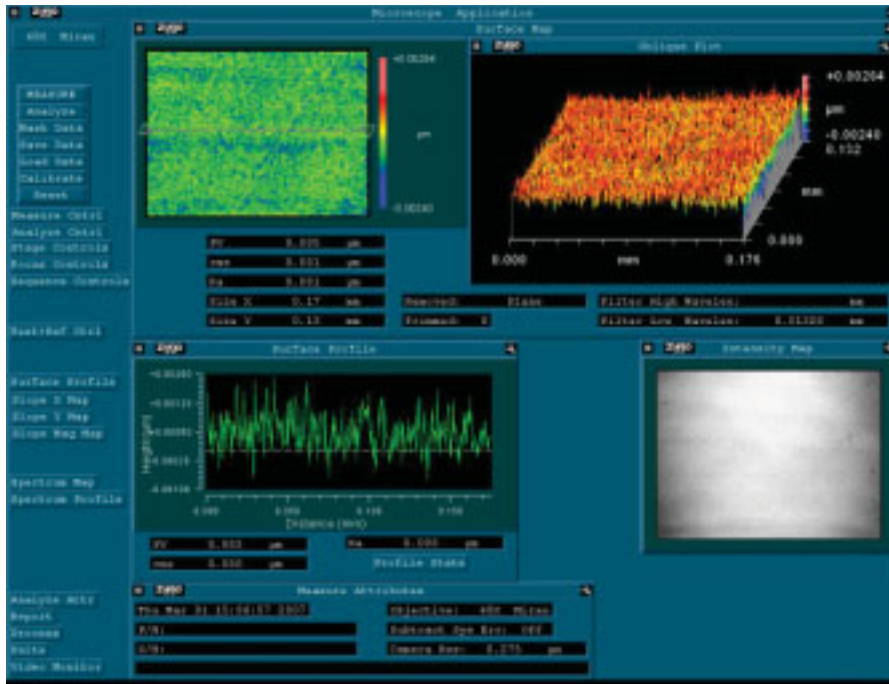
Figure 4.5 Screenshot of a WIM investigation from the surface of an Bectron EL37A film, showing an RMS roughness of 1 nm and a PV roughness value of 5 nm.
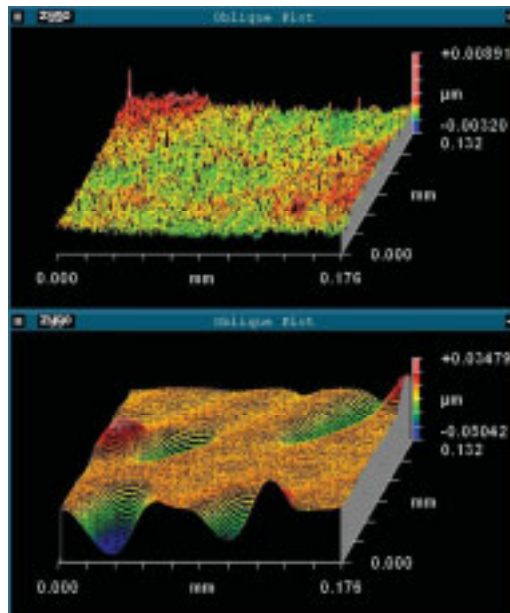

Figure 4.6 Screenshot of a WIM investigation from the surface of an BCB film, showing the roughness change on the surface after the exposure to TCB. Peak-to-valley roughness increased from 12 to 48 nm.

4.1.3 Dielectric properties of selected materials

Dielectric films were deposited by spin-coating on glass substrates in a clean room. Concentrations of solutions and spin-parameters were adjusted to get films of $0.5 - 2.0$ µm thickness. MIM capacitor structures were used in order to determine volume resistivity and dielectric constant.
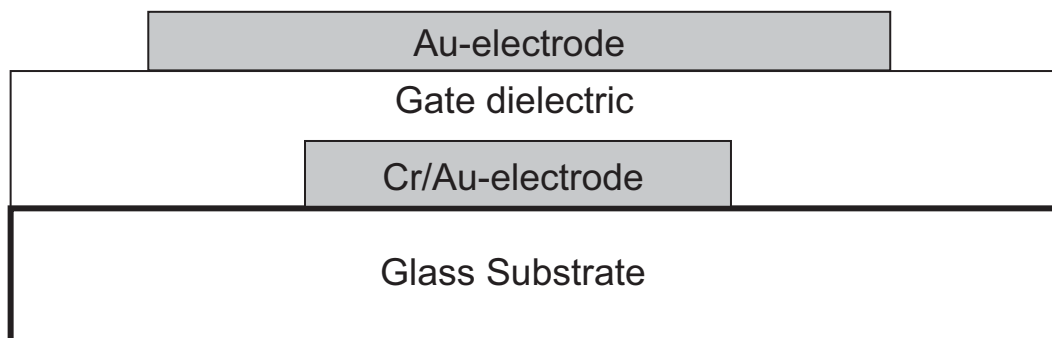

Figure 4.7 Schematic metal-insulator-metal (MIM) capacitor structure, which was used to test the dielectric properties of dielectric films.

During the efforts to measure the leakage through MIM-devices, it was observed that dielectric films of thickness under 1 µm exhibit increased leakage currents. In Fig. 4.8, a study showing statistical insulation quality of NOA74 is presented. The films which did not insulate either shorted or exhibited high leakage currents. Similar results were observed also with the other dielectrics. The sudden decrease in insulating properties with decreasing thickness was probably due to the quality of glass substrates and electrode on the glass. Spin-coated films are always prone to defects and these defects could dominate with decreasing film thickness. Therefore to realize high-performance organic transistors by solution-processing it is crucial to have a very smooth substrate surface in addition to the film-forming quality of the dielectric solution. This subject directly affects the reproducibility and still remains as one of the most important problems of organic electronics towards printed circuits.
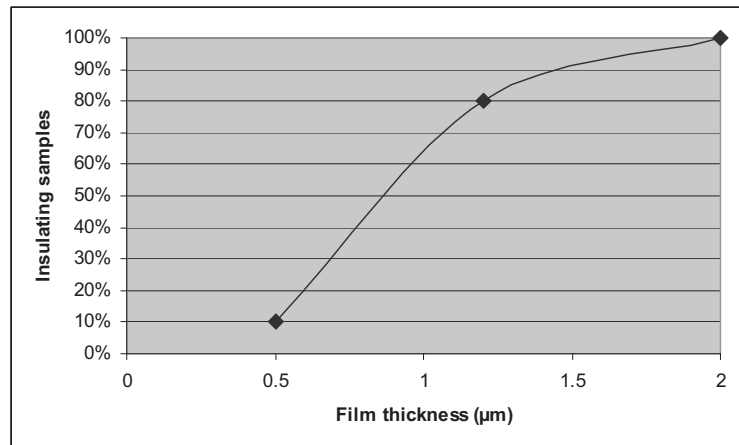
Figure 4.8 A plot showing the decrease in the percentage of insulating films with decreasing film thickness on glass substrates.

1.0 - 1.4 μm thick films were prepared for the reliable investigation of dielectric properties. MIM-devices with BCB, SU-8, NOA74 and EL37A were prepared, with thermally evaporated gold electrode at the top. In order to find out dielectric constant and volume resistivity of the dielectrics, capacitance and resistance values were measured.

Determination of dielectric constant

Capacitance values were measured from the MIM-capacitors by an LCR-Meter HP 4282A at 20Hz and 100 kHz. Dielectric constant was derived from:

$$\varepsilon_r = \frac{d \cdot C}{A \cdot \varepsilon_0} \tag{4.1}$$

where C is the measured capacitance and ε_0 is the permittivity of vacuum.

Determination of volume resistivity

In order to determine the specific volume resistivity, current passing through the dielectrics was measured in the MIM-capacitor structure under different voltages. Then, resistivity values were calculated by using Ohm's law and general formula for resistance:

$$\rho = \frac{V \cdot A}{I \cdot d} \tag{4.2}$$

where V is the applied voltage, A is the area of the capacitor plates, I is the measured current through and d is the distance between the plates.

Influence of solvent exposure on volume resistivity of dielectric films

To measure the resistivity, 80 V were applied on the capacitors. Leakage current values of 10 to 50 pA were measured from the MIM-capacitors of all four dielectrics, where the areas of capacitors were approximately 1 mm^2. When the resistivity values were calculated it was seen that all of the films offered good insulation. Volume resistivity values between 10^{12} and 3.2×10^{13} Ωm identify a good insulation. It is known that epoxy polymers exhibit around 10^{15} Ωm in their bulk states. Therefore it is reasonable that a thin layer which was deposited using great amount of solvents show slightly lower values. Corresponding volume resistivity values can be found in table 4.1.

Solvents were dropped onto the capacitors to test the influence of solvents (for P3HT) on dielectric films. Films were then dried at 150˚C for 1 hour, demonstrating the processing conditions of P3HT. Leakage current values increased slightly from 10-50 pA to 17-75 pA. Therefore, the layers proved to be good insulators even after the solvent exposure.

Table 4.1 Processing conditions and measured properties of selected dielectric materials

Polymer	UV Time	Curing Conditions	k (20 Hz / 100 kHz)	Resistivity (MIM) (Ω.m)	Roughness RMS/PV (nm)	Contact angle H$_2$O	Surface Energy (mJm^{-2})
BCB	-	*250˚C - 60 min. (vacuum)*	3.3 / 3.0	3.2×10^{13}	1 / 4	93º	34.3
SU-8	1 min.	150˚C - 30 min.	4.0 / 3.8	1.0×10^{12}	1 / 5	80º	41.5
NOA 74	30 min.	-	4.8 / 4.0	1.2×10^{12}	1 / 8	60º	43.1
EL37A	-	160˚C - 60 min.	4.0 / 3.3	1.7×10^{13}	1 / 15	96º	32.1

It can be observed from table 1 that NOA74 exhibits the highest dielectric constant. It contains polar groups, which also makes its surface hydrophilic. It is an advantage to have high polarity in dielectric films that increases induced gate capacitance. On the other hand polar groups could interfere with the semiconductor deteriorating device performance by affecting the charge transport, as mentioned in chapter 2. Therefore it is not trivial to conclude which dielectric would give the best result in an OFET, by examining this detailed table with material properties. Electrical characterization is the only method to observe the electrical properties of the dielectrics in a transistor.

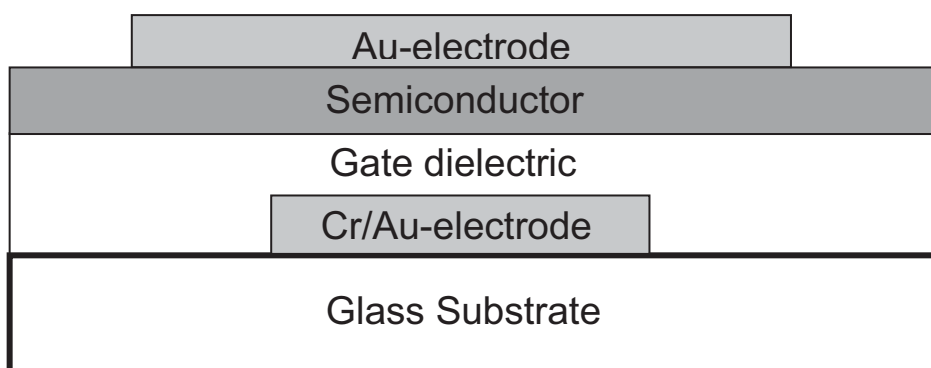### 4.1.4 Metal-insulator-semiconductor devices

Figure 4.9 Schematic metal-insulator-semiconductor (MIS) capacitor structure, which was used to test the insulation behavior of dielectric-semiconductor combinations in OFETs.

MIS devices were used to study gate-leakage in OFETs. MIS-devices have the similar structure as the OFET when the vertical cross-section is considered. For these tests, two dielectric materials were selected, where P3HT was deposited from 4 different solvents. Concentrations (0.4 – 0.7 wt. %) and deposition parameters of the solutions were adjusted to form layers with 30-40 nm thickness.

Dielectric films were proven to be good insulators and solvent resistant during MIM-investigations. However, when the semiconductor layer was stacked in between the top electrode and the dielectric, the leakage behavior changed significantly. In the MIS-configuration, where everything except the additional semiconductor was the same as MIM-devices, leakage currents increased up to values of 1 nA to 10 nA. Although the insulators were the same and solvents for the semiconductor did not affect the dielectrics considerably, the leakage current increased by almost 3 orders of magnitude. The observation was confirmed by depositing P3HT films from four different solvents on NOA74 and EL37A dielectrics, so that the measurement was independent of solvent effects (Fig. 2). It can be concluded that the current through the dielectric increases when a semiconductor layer replaces an electrode. This phenomenon was already reported by M. Raja, et al. It was explained by the increased amount of charge injection into the dielectric, due to the displacement of dopant ions or impurities in the semiconductor [116]. Dependence of leakage current on the doping state of the semiconductor was also investigated in MIS-devices. To do that, an extra annealing step was applied under vacuum so that the unintentional doping level of P3HT was decreased. In every material-solvent combination, lower leakage currents were

obtained in the de-doped states, which also support the previous efforts (Fig. 3). This effect explains the increased leakage in the transistors. The current does not flow directly from S/D electrodes into the dielectric, but through the semiconductor. Therefore, part of the semiconductor layer overlapping with the gate electrode should be minimized in transistors to decrease the leakage current.
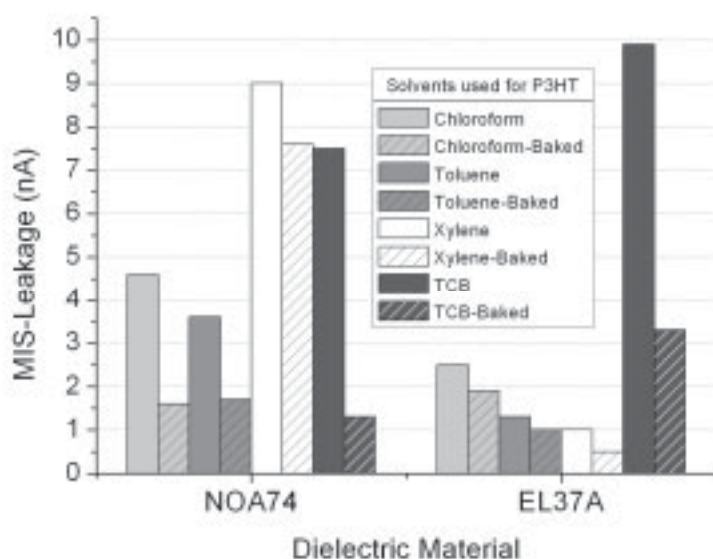

Figure 4.10 Leakage currents flowing at 80 V measured from Au/ dielectric/P3HT MIS-devices. P3HT as deposited from four different solvents on two different dielectric materials. Currents decreased with decreased doping level in all cases.

4.2 OFETs with polymer dielectrics

4.2.1 Production and characterization of bottom-gate OFETs

Bottom-gate transistors were prepared with all four dielectric layers, by using a shadow mask for the source and drain electrodes. Channels of length 26µm and width of 1-2 mm (Fig. 1) were formed. P3HT was used as semiconductor layer and spin-coated under nitrogen atmosphere, from 0.5 wt. % chloroform solutions. After the deposition of P3HT, the devices were heat-treated at 150 °C.
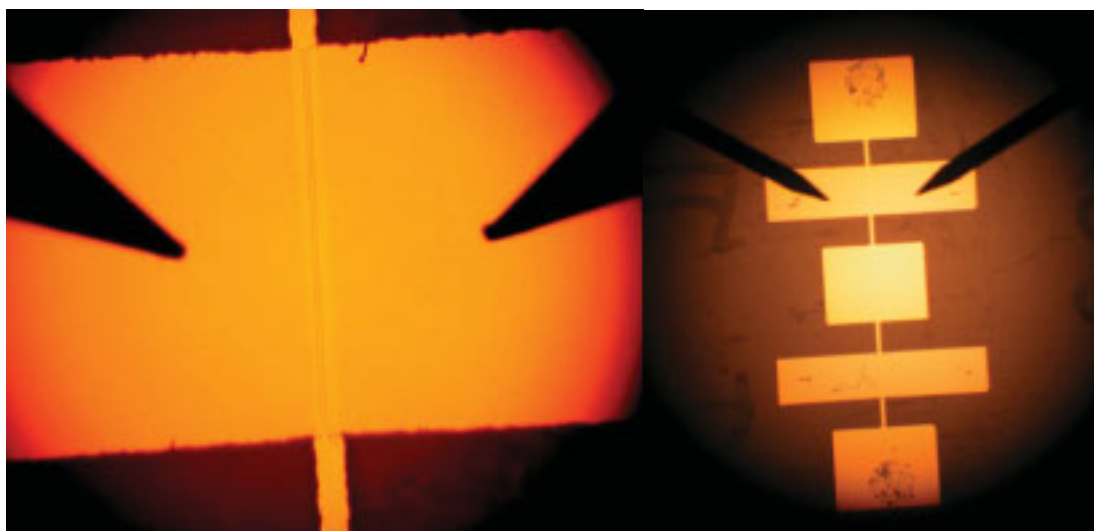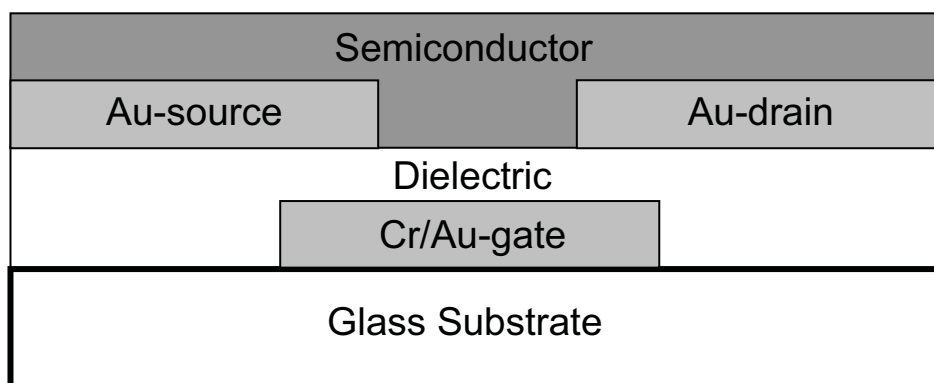
Figure 4.11 Schematic view of a bottom-gate OFET with organic dielectrics (top) and optical microscopy pictures of such an OFET (bottom).

Electrical Characteristics

Output and transfer characteristics of devices were measured in a glove-box under nitrogen atmosphere. Measurement and evaluation of these transistors were conducted following the same methods for hybrid devices. Mobility and threshold voltage values were calculated. Devices with organic dielectrics exhibited similar field-effect mobility values to their hybrid counterparts: 10^{-5} to 10^{-3} cm^2/V.s in P3HT devices, and 10^{-1} to 10^{-3} cm^2/V.s in pentacene devices. These values are typical for devices with polymer dielectrics. Since polymer dielectric layers were 3-4 times thicker than SiO$_2$ dielectric, the induced capacitance values at the gate dielectric were lower. As a result, these devices exhibited lower output drain current values at the same operating voltages.
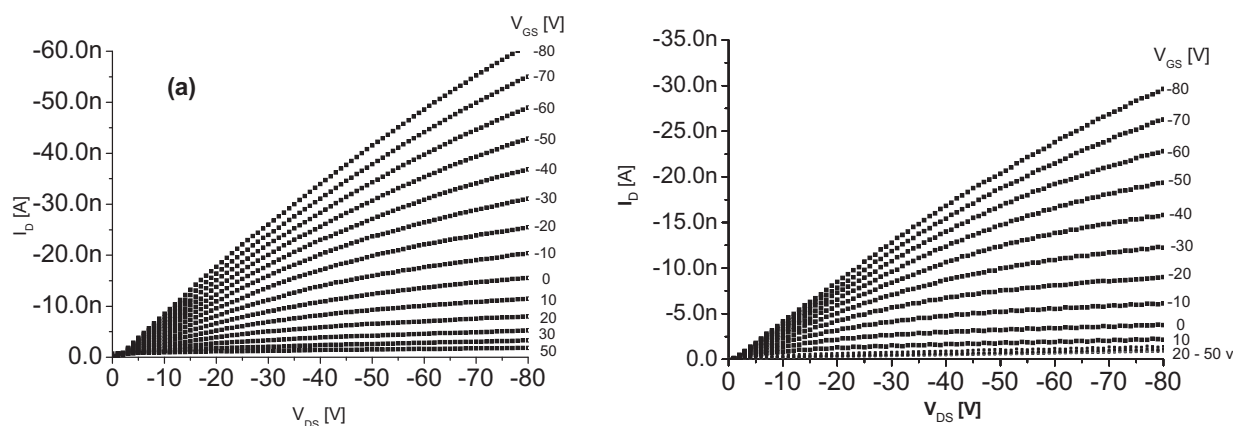
Figure 4.12 Exemplary output characteristics of OFETs with (a) SU-8 and (b) BCB dielectrics.

Threshold voltage values of the transistors were determined by extrapolating the tangent to the plot $I_D^{1/2}$ vs. V_G to the V_G – axis where the applied V_D was – 80 V. Saturation field-effect mobility values were calculated from the slope of the transfer curves (V_D = – 80 V) by using the equation for transconductance g_m. These conventional methods were used to compare the transistors prepared in this work. They do not consider the differences in transistor configuration and characteristics which may affect the evaluation [117].

A common observation in almost all of the devices was that they exhibited slightly higher off-current values, I_D (V_G = 0 V), than their hybrid counterparts (Fig. 4.13). This indicates a high conductivity in semiconductor. It was possible to turn off the channel by applying positive voltages to the gate. In Fig. 5 there is a comparison of a hybrid transistor with a transistor of NOA74 dielectric. It can also be observed from the comparison of transfer characteristics (hybrid vs. polymer) that the threshold voltage was shifted to positive values where NOA74 was the dielectric. Mobility was slightly higher in the hybrid transistor, due to the proper interface offering higher crystallinity in P3HT. Increased conductivity can be explained by the purity/doping state of the films, whereas mobility is generally related to the quality of the dielectric/semiconductor interface and the ordering of the semiconductor [29, 118]. Almost all of the P3HT-transistors with an organic dielectric suffered from a slight unintentional doping at the interface. As a result off-current values increased dramatically. This was most probably due to the impurities originating from the dielectric during the solution-processing of the semiconductor. Such impurities were absent in hybrid devices due to high-purity and homogeneous HMDS interface. The lacking adequate saturation at high drain currents and non quadratic increase of the saturation drain current with the gate bias are

observed along with these devices. The latter can be explained by a gate voltage dependence of the mobility, whereas a parallel resistance (doped semiconductor bulk) is attributed to the lacking saturation at high drain voltages. These two effects are typical for organic transistors and often discussed together with the threshold behavior in previous studies [119].
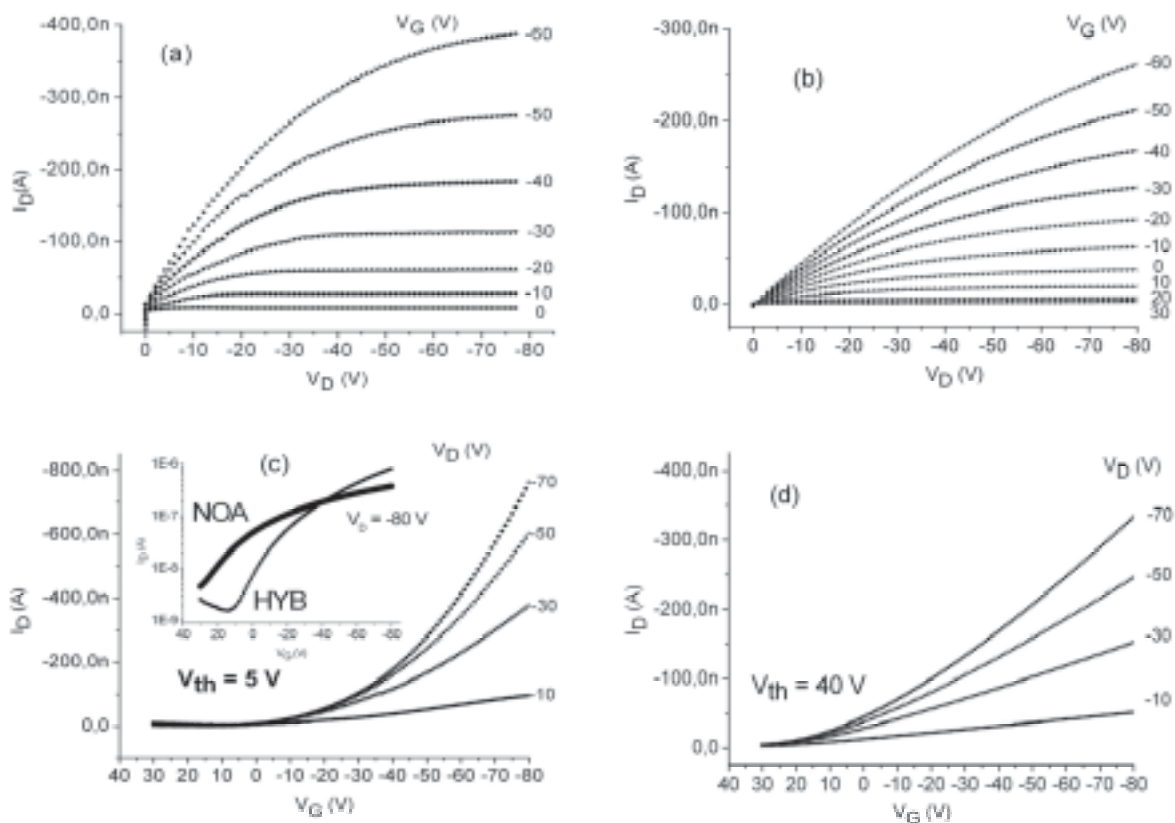

Figure 4.13 Comparison of electrical characteristics of a transistor with NOA gate dielectric, shown in the graphs (b) and (d), with a hybrid transistor shown in part (a) and (c). In the inset of part (c) a comparison of transfer curves for V_D = -80 V is presented. On/off current ratios of 523.6 and 83.6 were extracted for hybrid and NOA transistors, respectively.

4.2.2   Comparison of devices with different semiconductors

Five different dielectric materials were tested in this research until now: SiO_2, BCB, SU-8, EL37A and NOA74. In this section, OFETs that were prepared using pentacene in addition to P3HT will be presented. P3HT was deposited from 4 different solvents, forming thin-films of 30-50 nm thickness. Varying annealing times were used according to the boiling points of the solvents. Since TCB is a high boiling point solvent, extended annealing times were used to get the solvent completely out of P3HT. Pentacene (Aldrich, purity: 99.8%) layers of 120 nm

thickness are thermally evaporated at 1 Å / s through a shadow mask in vacuum with 3×10^{-6} Torr. Since P3HT shows significantly different electrical behavior when it is deposited from different solvents it can also be said that five different semiconductors were used for this study. Therefore a complete matrix of dielectrics and solvents was formed through which a comparison of devices can be made (Table 4.2).

Table 4.2 Dielectric capacitance values presented with threshold voltages and saturation field-effect mobility values of different transistors.

Dielectric Material	C_i (nF/cm^2)	V_{th} / Saturation Field-Effect Mobility (cm^2/V.s)			
		P3HT-CHL	**P3HT-XYL**	**P3HT-TCB**	**Pentacene**
SiO$_2$	11.5	**+5 V** / 3.2×10^{-4}	**+19 V** / 5.5×10^{-4}	**+8 V** / 1.3×10^{-3}	**-10 V** / 0.1
BCB	2.7	**+32 V** / 5.6×10^{-5}	-	-	**-21 V** / 2.1×10^{-2}
SU-8	2.7	**+75 V** / 6.2×10^{-5}	**+59 V** / 9.5×10^{-5}	**+64 V** / 3.3×10^{-4}	**+16 V** / 1.2×10^{-2}
NOA74	3.0	**+30 V** / 5.7×10^{-4}	**+72 V** / 1.7×10^{-5}	**+24 V** / 6.1×10^{-4}	**+25 V** / 2.3×10^{-3}
EL37A	2.7	**+35 V** / 1.2×10^{-4}	**+67 V** / 2.2×10^{-4}	**+32 V** / 8.0×10^{-4}	**-2 V** / 2.3×10^{-2}

Solution-processed transistors generally exhibited the highest mobility where the semiconductor P3HT was deposited from the solvent TCB, due to the high boiling point of TCB. The values increased with increasing boiling point of the solvent for almost every dielectric. However, it can be observed by the comparison output characteristics in Fig. 4.14 that in some cases the conductivity values ($V_G = 0V$) were higher where the mobility was higher. A relationship between mobility and conductivity was already discussed in previous studies [120, 121]. Therefore, it can be concluded that transistors showing a high mobility value together with a low threshold voltage exhibit a proper dielectric/semiconductor interface and a highly ordered semiconductor.
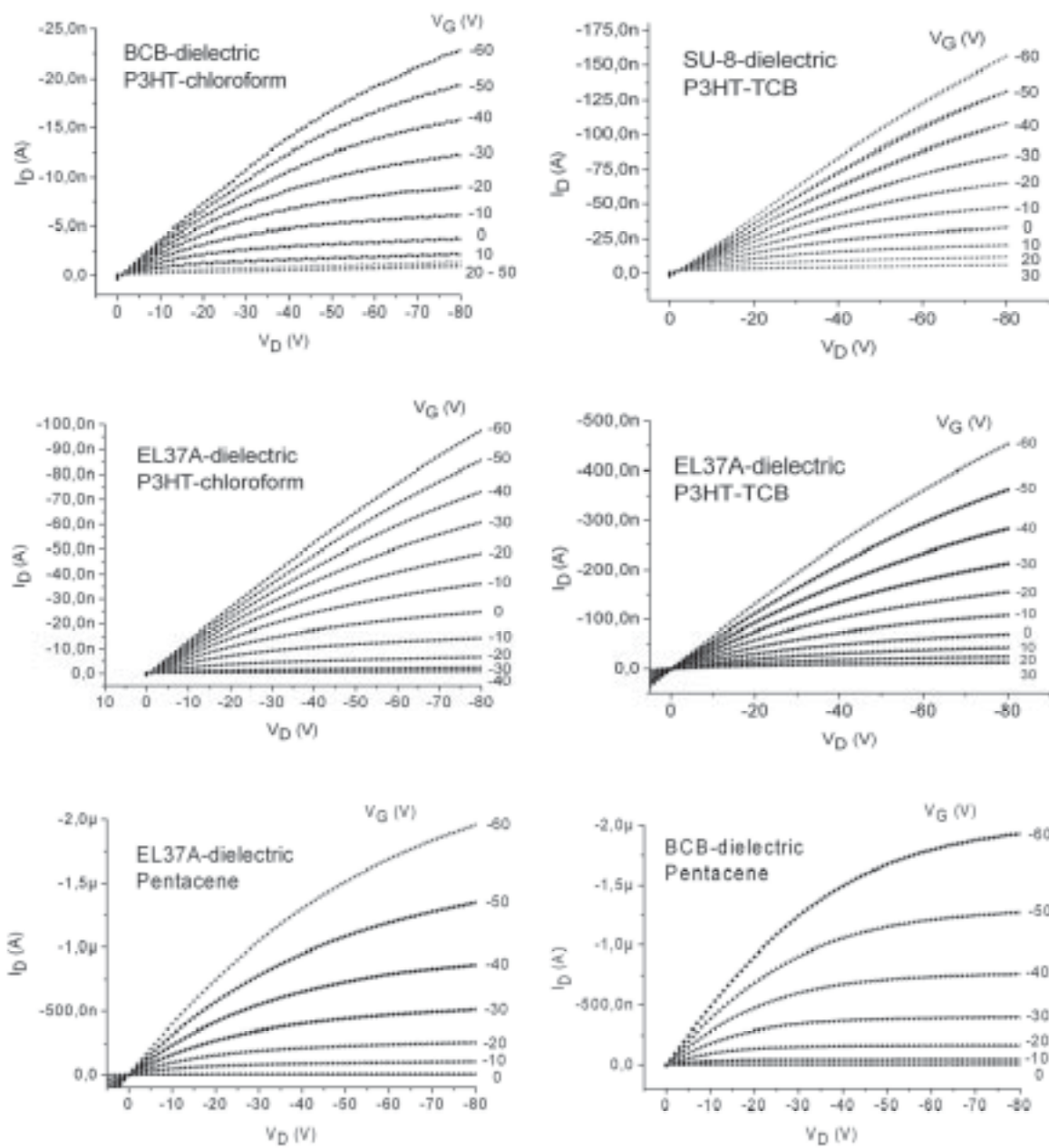
Figure 4.14 Exemplary output characteristics of OFETs with different dielectrics using P3HT and pentacene as the semiconductors.

Pentacene Transistors

In case of pentacene as the semiconductor the transistors exhibited better saturation behaviour of drain current in output characteristics. Also the measured off-current values were lower due to high-purity and vacuum processing of pentacene without using solvents.

Field-effect mobility values were approximately two orders of magnitude higher than those of P3HT transistors, as expected (Table 2). It was observed that the mobility values of pentacene transistors decreased with increasing surface energy of the dielectric; as discussed by Yang, et al. [122] NOA74-pentacene combination probably suffers from a bad interface, exhibiting improper transistor characteristics. NOA74 also had the highest surface energy. However, a direct dependence of mobility on dielectric surface energy can not be concluded here since the dielectrics not only have different surface energies but also different chemical groups.

When the output characteristics of pentacene transistors with BCB and EL37A dielectrics are compared, it can be seen that the saturation behaviour of the drain-current is better where the conductivity is lower. This was also confirmed by the threshold voltage values of BCB-pentacene combination -21 V whereas that of EL37A combination was -2 V. BCB transistors showed a slightly better saturation, since the parallel resistance caused a smaller current.
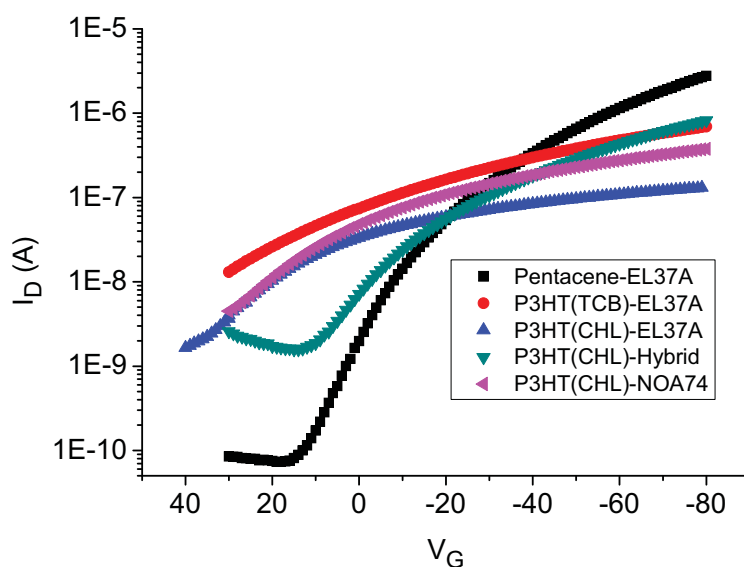

Figure 4.15 Comparison of transfer characteristics of different devices showing the differences in the turn-on behavior.

In Fig. 4.15, transfer characteristics of five transistors with different semiconductors are compared in one plot. Significant difference between the performances of pentacene and P3HT; not only in terms of mobility but also on/off current ratio can be observed from transfer characteristics. The off-state current not only depends on the film conductivity but also on the **contact resistance** between electrodes and semiconductor, affecting the charge injection. Pentacene exhibits a high contact resistance to gold, leading to low off-state current values [21]; whereas P3HT has a similar work function to gold, which leads to higher off-state current values [123].

Patterning of the semiconductor for improved gate-leakage

In an additional study to decrease gate leakage-current through the dielectric outside the channel area, semiconductor around this area was carefully removed by a scalpel (Fig. 4.16a). This simple patterning of semiconductor resulted in a considerable reduction in gate current (Fig. 4.16b). Gate-leakage affects the device performance when it was in the same range as the drain-current, which ranged between 10-400 nA in P3HT devices. Therefore a reduced leakage value of 200 pA is acceptable.
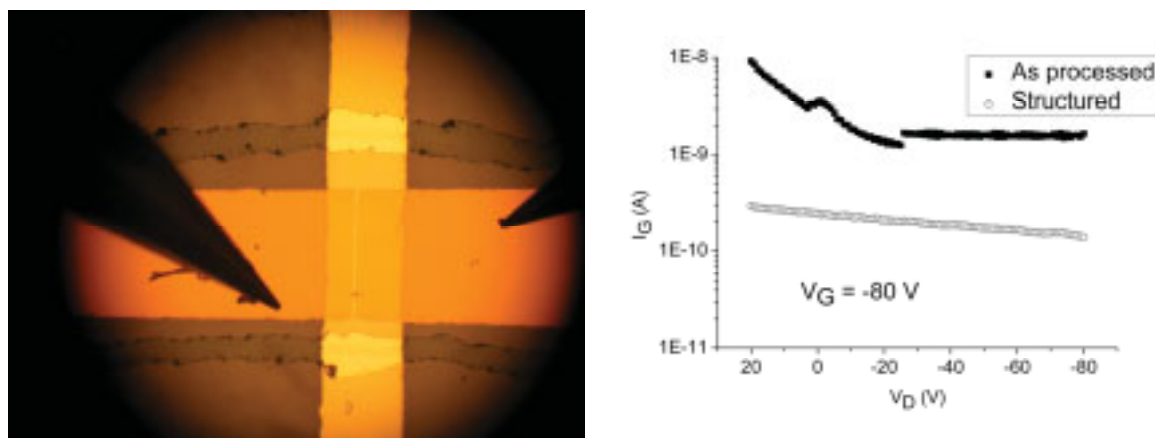

Figure 4.16 (a) Picture of a scalpel-structured OFET (b) Influence of structuring on the gate-leakage.

Leakage current was successfully reduced by at least one order of magnitude by the structuring of semiconductor. This improvement was critical for the selected configuration since the leakage currents were sometimes in the range of channel currents. The importance of this patterning step would be less in case of a device with higher current output.

4.2.3 All-organic transistors with NOA74 by laser structuring

This section presents laser-structured all-organic transistors with NOA74 as the gate dielectric, poly(ethylenedioxythiophene)/polystyrenesulfonate (PEDOT/PSS) as the electrode material and P3HT as the semiconductor. This work was conducted in cooperation with the Department of Electronics, Helmut-Schmidt-University/University of Federal Armed Forces in Hamburg, where the laser ablation process was developed. The main goal of this study was to demonstrate all-organic devices with the selected materials and solution-processing techniques. NOA74 has already shown a very good dielectric performance in the previous section, where gold electrodes were used. In this study, the final step towards all-organic devices was taken and gold electrodes were replaced with PEDOT/PSS, which were patterned by laser.

The patterning of the electrode structures was accomplished with a laser system that was originally designed and employed for surface cleaning purposes. This prototype – called Scanning Excimer Laser Cleaning Unit (SELCU) – consists of the Excimer Laser Lumonics PM 848 followed by an variable attenuator, a beam homogenizer, a field-lens, two galvo scanners and finally an F-Theta lens (80 mm in diameter, front lens is 66 mm in diameter at a length of 40 mm) [14]. The scanning rate and consequently the deflection of the beam is adapted to the pulse repetition rate (up to 1 kHz) and therefore allows for extremely fast automated processing. An accurately controlled beam positioning together with the top-hat profile ensures a very homogenous, uniform and reliable irradiation of each surface element with almost identical laser fluence. In order to process large areas, the beam moves step by step to adjacent sites of action where the scanning speed is adapted to the pulse frequency of the excimer laser. The whole setup is computer controlled so that exact and highly reproducible positioning is possible. A more comprehensive description of this laser ablation system can be found in a recent article [64].

Fabrication of all polymer FETs starts with the formation of the gate electrode on a glass substrate. This is done by spin-coating filtered (PVDF 0.45 µm pore size) PEDOT/PSS in the formulation CPP 105D from H.C. Starck with 2000 rpm for 10 s. This formulation of PEDOT/PSS was chosen due to its high conductivity in comparison to other PEDOT/ PSS formulations and its good adhesion, especially on glass. After spin-coating, the sample undergoes a hot-plate annealing for about 10 min at 80°C. For the formation of the gate

electrode, the SELCU is set to a fluence of 1500 mJ/cm^2 since lower values left residue of CPP105D on the glass substrate.
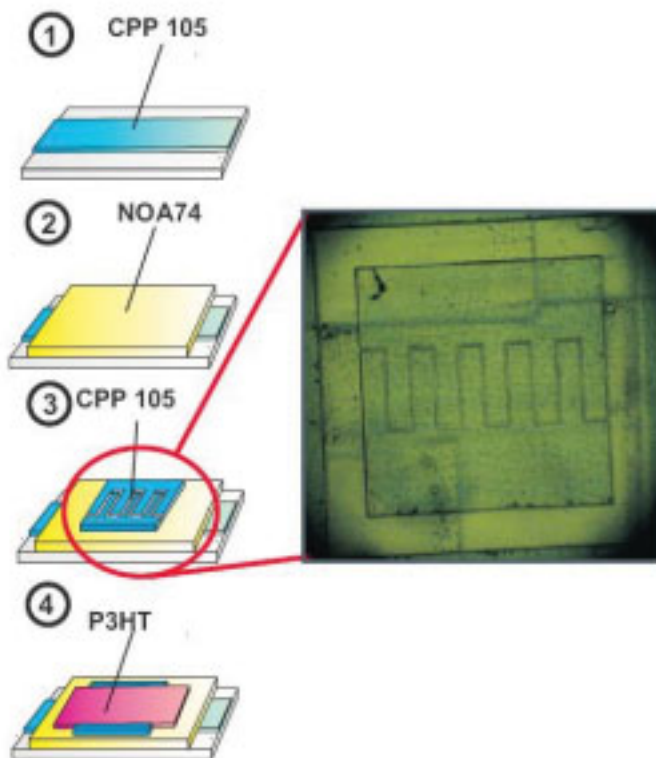

Figure 4.17 Simplified process flow: (1) glass substrate with CPP 105D – patterned in the scanning mode (2) followed by the gate dielectric NOA74 and (3) source and drain electrode from laser patterned CPP 105 in the shot mode. (4) The last layer consists of the semiconductor P3HT. Additionally to the process flow two magnified images ((a) optical, (b) AFM) of the 10 μm channel are displayed [64].

Subsequently, the laser beam is moved across the surface by the x- and y-scanner so that large areas are ablated and only one small stripe of CPP 105D with a length of 2.6 cm and a width of 0.35 mm remains. The next process step is the deposition of the insulating layer of NOA74 (filtered PTFE 0.2 μm pore size) diluted in n-methylpyrrolidone (NMP). This material is spin-coated for 60 s at 6000 rpm resulting in a 1.2 μm layer. NOA74 is then cured under an UV lamp (253.7 nm) for approximately 1 h. The resulting film has a dielectric constant of 5.46 at 10 MHz and an average roughness of 15 nm. The next layer – as a preparation for the source and drain electrodes – is again spin-coated from filtered CPP 105D and structured in shot mode. As mentioned before, a positive chromium mask is inserted into the first focal point and the pattern on the mask is projected onto the CPP 105D layer on the insulating NOA74

layer. This patterning technique is being strongly supported by the ductile surface properties of the optical adhesive. The image projection of 1:3 reduces the actual size of the square mask and results in a channel length of 10 μm. The best results are obtained using 200 shots at a repetition rate of 200 Hz and with fluences between 150 and 200 mJ/ cm^2. For the semi-conducting layer poly(3-hexylthiphene) (P3HT) – 0.5 weight percent in CHCl$_3$ (99.9%+ purity, <0.01% H2O) – is filtered (0.2 PTFE μm pore size) and spin-coated (3 s at 800 rpm, 10 s at 2000 rpm) on the electrode structure. Solvent residue is removed with a temperature treatment at 120 °C for 60 min in vacuum. The resulting thickness of the P3HT layer is 50 nm on average, determined by profilometry on a flat glass surface. After preparation the devices were characterized in a glove box using an Agilent parameter analyzer 4156C. Fig. 4.17 shows a simplified process flow.
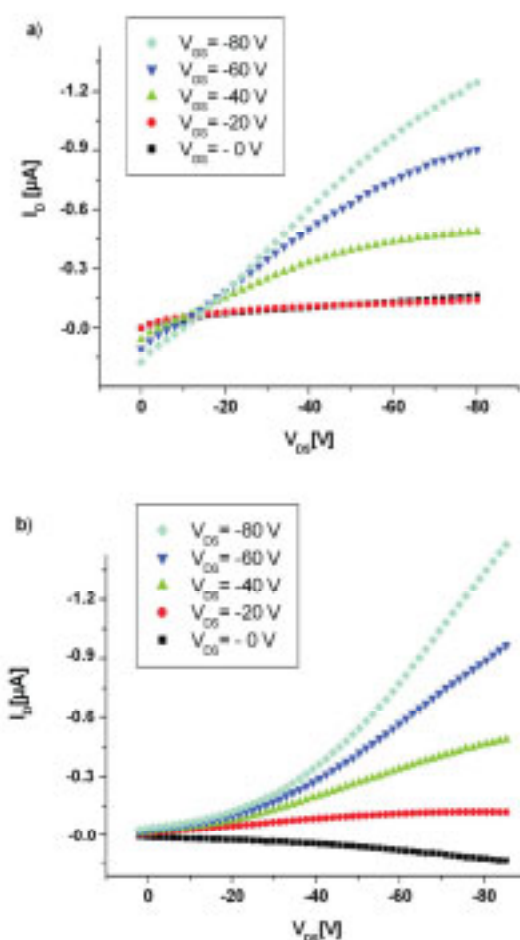

Figure 4.18 (a) Output and (b) transfer characteristics of an all polymer transistor with an NOA-NMP gate dielectric.

Evaluation of measured transistor characteristics in the saturation regime yields mobilities around $4.2 \cdot 10^{-4}$ cm^2/Vs, on/off-ratios of 182 and threshold voltages of approximately 33 V. Fig. 4.18 depicts the exemplary output and transfer characteristics of one of the fabricated transistors.

As a conclusion, all polymer FETs employing a laser system were presented. The laser system allows precise and quick structuring of gate source and drain electrodes in a bottom gate configuration. With a throughput of 6 cm^2/s, this method certainly enables a route towards a roll-to-roll process – especially in connection with ink-jet printing or doctor blading. FETs – with a mobility of $4.2 \cdot 10^{-4}$ cm^2/V.s – were produced at a minimum feature size of 10 μm.

4.3   Conclusion

This chapter elaborated on organic transistors with polymeric dielectric films and their electrical properties. A systematic materials selection and characterization was conducted, considering simple solution-processing conditions for organic gate dielectrics. Chemical stability required for the stack integrity, film-forming and surface properties, low-temperature processing and compatibility with the semiconductor were some of the most important constraints in materials selection.

Four thermosetting polymers were selected and processed into dielectric thin-films. Electrical properties of the dielectrics, BCB, SU-8, EL37A and NOA74, were investigated in MIM and MIS capacitors and OFET configuration. All of the materials formed solvent resistant and smooth films. They exhibited high volume resistivity values at 1.2-1.4 μm thickness. With its fast UV-curing property and higher dielectric constant, NOA74 turned out to be a very attractive candidate for simple solution-processing of organic transistors.

OFETs were produced with P3HT and pentacene layers as semiconductors. Solvents with different evaporation rates were used to deposit P3HT. Highest field-effect mobility values were obtained from devices with EL37A and NOA74 dielectrics, with 8.0 and $6.1 \cdot 10^{-4}$ cm^2/V.s respectively. In both of these cases P3HT was dissolved in TCB which has a very high boiling point of 204°C. The devices exhibited lower mobility values with respect to hybrid devices. This was an expected behavior since hybrid devices use an HMDS treated oxide surface, which favored the crystallization of P3HT during spin-coating. HMDS surface also leads to a homogeneous, high purity dielectric/semiconductor interface which decreases

the number of traps and defect states; therefore increases the effective contribution of charge carriers on the current.

Another common observation from the devices with polymer dielectrics was the high current in the off-state. Although the device configurations were the same as hybrid devices, off-current values were approximately one order of magnitude higher. Probably impurities resulting from the dielectric during the deposition of P3HT act as dopants and increase the semiconductor conductivity. In some cases impurities also caused a poor reproducibility of devices, since currents in the off-state were varying from device to device. The importance of a high purity dielectric material and surface was therefore addressed at this point once more. Finally a completely solution-processed all-organic transistor was demonstrated successfully by utilizing laser-patterned PEDOT electrodes and NOA74 dielectric. Gold electrodes were simply replaced with spin-coated and laser-patterned PEDOT electrodes. PEDOT, NOA74 and P3HT can be stacked together without limiting the device performance dramatically. Transistors exhibited a mobility value of around 10^{-4} cm^2/Vs which is in good agreement with the devices using metallic electrodes. Electrical characteristics of the transistors could be further improved by optimizing the electrode configuration and material purity. On the other hand, these devices can be produced via a low temperature processing route (T<100°C), which is extremely interesting for a possible mass production. Additionally, laser-ablation proved to be a fast and reliable production method for the precise structuring of PEDOT electrodes, without damaging the underlying layers.

5 Solution-processed nanocomposite gate insulator for low driving-voltages and ferroelectric memory effect

In this part of the research, ferroelectric functionalized OFETs prepared with high-*k*, pure and composite gate-insulation layers are presented. There were two different goals in this study:

- Reducing the voltage of operation by modulating the dielectric constant of the composite gate insulator;
- Demonstrating ferroelectric memory function in P3HT transistors.

In order to realize this, pure PVDF/TrFE layers, and composite layers where PVDF/TrFE was blended with barium titanate (BT) nanopowder were used. Since BT-particles exhibit high dielectric constant values, they contributed to the dielectric properties of composite layer. In that sense, dependence of dielectric constant on the amount of BT in composite films was investigated. Solution-deposited nanocomposite layers were then introduced into ferroelectric OFETs with this study.

The most attractive advantage of these layers is that the implementation of composite films neither requires complex processing steps nor limits the functional operation of the organic devices. Therefore, composite layers that were produced in this work could integrate easily into an existing technology based on organic devices. However, to achieve this, homogeneous dispersion of the fine ceramic powder in polymer matrix is essential where highly insulating, defect-free films should be obtained. Therefore, to examine the film quality, optical microscopy and white-light interferometer studies were also conducted.

Composites are engineered materials made from two or more constituent materials with significantly different physical or chemical properties and which remain separate and distinct on a macroscopic level within the finished structure. The aim is to benefit from the properties of both materials and additionally from their cooperation. In this work, high dielectric constant of BT nanopowder was combined with PVDF/TrFE to be solution-processed into flexible layers. Therefore, simple processibility is offered together with a very high dielectric constant and mechanical flexibility. Noting that these films require only 150°C

for the physical drying process after deposition, the dielectric constant values achieved in this study are extremely high.
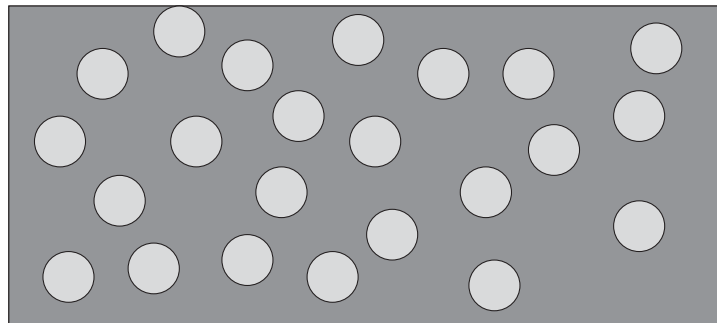

Figure 5.1 A schematic cross-sectional view of a composite film, where ceramic powder particles are blended into a polymer.

While improving a property, loss in other properties are expected since by blending nanopowder into polymer matrix some defects are introduced. It is required that the polymer forms a continuous matrix in the composite, covering powder particles without agglomeration and therefore insulating capability of the films should not be affected dramatically. For this reason, dielectric properties of the films were examined in a metal-insulator-metal capacitor structure. Two critical insulation properties were investigated from capacitors: Specific volume resistivity and dielectric constant. Pure PVDF/TrFE layers are known to exhibit very good dielectric and ferroelectric properties. Taking properties of pure polymer as reference, insulation and dielectric properties of composite layers were investigated.

Organic transistors with both pure and composite layers were produced and investigated. Effects on operating voltages by the application of composite layers were investigated. Finally, ferroelectric hysteresis and memory retention properties were demonstrated.

5.1 *Materials and methods*

Poly (vinylidene fluoride)

PVDF and its copolymers are among the most intensively studied ferroelectric polymers [88, 124, 125]. In addition to their promising electrical properties they have high solubility in organic solvents, which makes their simple solution processing into thin polymer films

possible. With operations such as annealing, poling and film stretching one can obtain at least 4 different polymorphs (phases). The most interesting polymorph is the β polymorph in which the chain conformation is all-trans. β polymorph has the highest ferroelectric response, due to an optimized alignment of all the dipoles in the crystal unit cell. In order to obtain the β polymorph by solution-processing, PVDF is copolymerized with PTrFE. This is said to enhance the all-trans conformation associated with the β polymorph because PTrFE has three fluoride atoms per monomer, which are larger than hydrogen and therefore induce a stronger steric hindrance. The ferroelectric phase is obtained for molar ratios between 50 and 80 % of PVDF [88]. Although PVDF offers high dielectric constant and good ferroelectric properties there has always been interest in improving its dielectric, ferroelectric, and piezoelectric properties by blending them with functional inorganic powders such as lead zirconium titanate or barium titanate [126-130]. These studies generally elaborated on bulk materials or thick films, whereas some studies on thin-films were also conducted. Dielectric constant values of higher than 300 were reported for thick pellets [126] and 63.5 for thin films [127] of such composites. Also improved ferroelectric properties such as remnant polarization and coercive field were reported. Such a flexible, solution-processed thin insulator layer with improved properties is very attractive for usage in organic transistors.
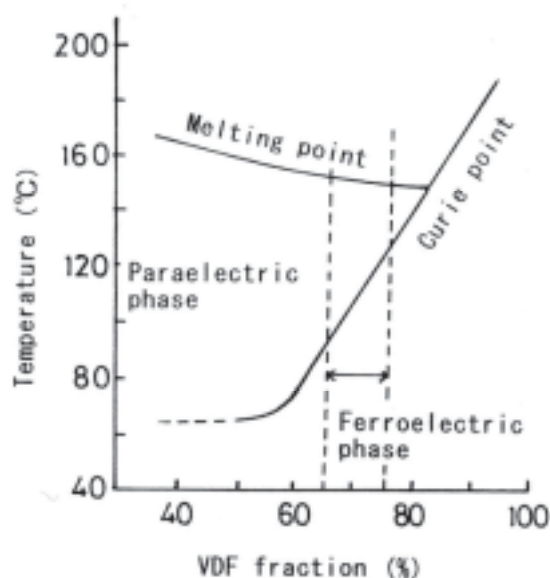

Figure 5.2 Vinylidene fluoride (VDF) – trifluoroethylene (TrFE) phase diagram showing the stable ferroelectric phase [88].

Solution and dispersion preparation

Ferroelectric copolymer PVDF/TrFE (SOLEF 05018TA, 0001) was dissolved in a 1:1 mixture of N-methyl pyrrolidone and acetone. This solution was used for the pure polymer films. In order to prepare composite films, BT nanopowder (99,6% purity, APS 85-128 nm) was added to these solutions and mixed for 10 min on a magnetic stirrer at 500 rpm. In order to improve the dispersion of BT particles 1 wt % of a surfactant was added to the solution (TEGO WET 280). Surfactants favor the dispersion by decreasing the surface energy between particles and the solvent. Prepared mixtures were then stirred for 24 h at 1000 rpm, finally sonicated for 30 min.

Films were deposited by spin-coating, on glass substrates or on P3HT layers, depending on the application. Different concentrations were used in order to get films of 2-12 μm thickness. For the composite films, higher film thicknesses were preferred to prevent increased leakage currents through the layers.

5.2   *Optical and surface characterization of pure and composite films*

Pure and composite films were spin-coated on glass substrates to examine the film quality. Film thickness and roughness values were determined by Dektak 3030 ST surface profilometer. However, to get a better idea about the film surface and morphology, white-light interferometry was used. Since the performance of composite films depends on the quality of dispersions, it was crucial to control whether increased agglomeration of nanoparticles affected the film quality. In case of a serious agglomeration, insulation capability of the films decreases and therefore the performance is affected.

It can be observed in Fig. 3 that both pure and composite films are continuous and homogeneous. Grain size was smaller in the composite films. This is possibly due to the increased number of nucleation sites and pinning of the moving grain boundaries by the nanoparticles, during the crystallization stage.
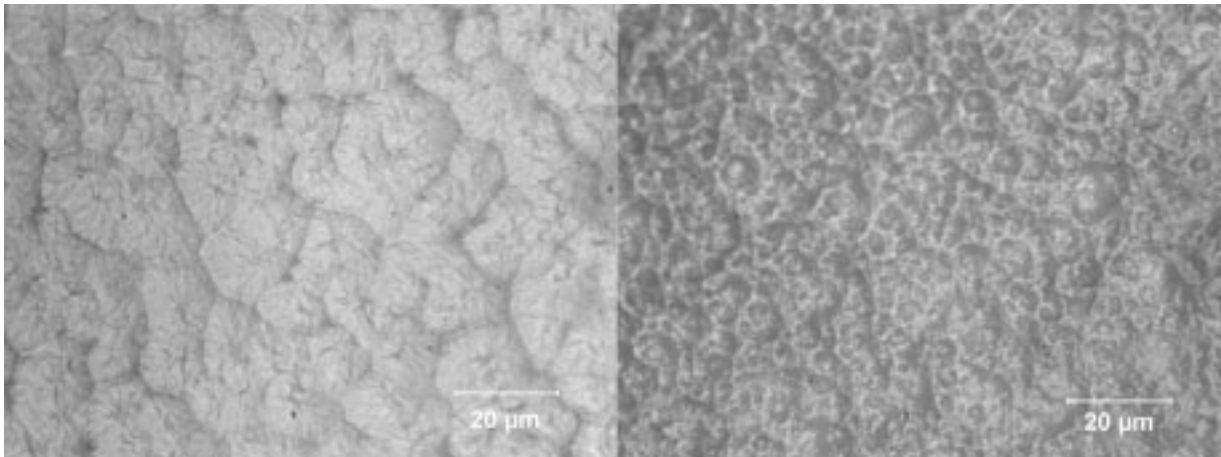
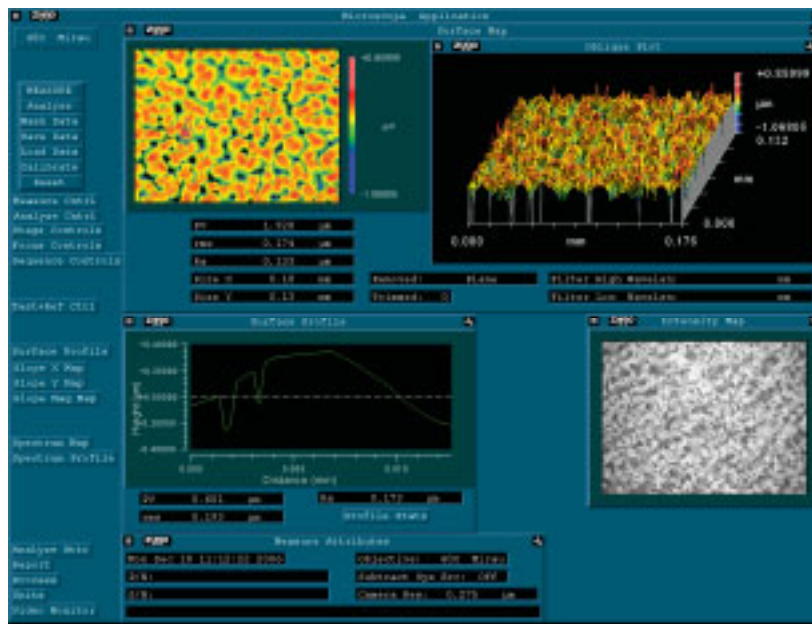**Figure 5.3** Optical microscopy pictures of pure PVDF/TrFE (left) and 50 vol % BT (right) composite.

Figure 5.4 Screenshot of a WIM investigation from a 3.6%BT blended PVDF-TrFE composite film.

5.3 *Determination of dielectric properties of pure and composite layers*

Metal-insulator-metal capacitor structures were used to determine the dielectric properties of pure and composite layers. Similar to those presented in chapter 4, dielectric films were deposited on glass substrates with gold electrodes. Finally top gold electrode was deposited to form capacitors. Dielectric constant and specific volume resistivity values were determined as described in chapter 4, similar to dielectric layers for bottom-gate transistors. Current passing

through the capacitors at 80 V was measured to find the resistance and determine specific volume resistivity. Capacitance values were measured at 1 kHz and 100 kHz through which the dielectric constant values were calculated. The results are listed in TABLE 1, together with the film thickness and roughness properties. Properties of pure polymer film and composite films with various BT concentrations can be observed.

Resistivity values obtained for both the pure and the composite films were in the range of 10^{10} Ω m, which indicates a proper electrical insulation. Composite films exhibited slightly lower resistivity values than pure PVDF/TrFE films. Since the film thickness was increased for composites of increasing ceramic content, decline in resistivity stayed in acceptable limits. Although thinner composite films which performed good insulation properties were produced, they were not reported since the reproducibility decreased dramatically.

Table 5.1 Dielectric properties of the pure and composite films measured from MIM-capacitor configuration, presented together with the film thickness and roughness data.

Vol. % ceramic	$\rho_s \times 10^9$ (Ω.m)	ε_r (1 kHz/100 kHz)		Thickness/Roughness (μm)	
0	68.0	15.8	12.2	2.6	0.138
3.6	10.2	20.4	15.7	5.2	0.170
10	4.6	26.1	19.7	6.0	0.148
14	15.8	27.7	21.2	4.8	0.195
25	8.3	34.7	27.8	8.5	0.299
50	25.0	51.5	42.3	12.0	0.318

ε_r values increased with increasing BT content in the composites, and for every discrete composite they decreased with increasing frequency. High frequency dependence of dielectric constant is typical in ferroelectric materials, due to ionic structure. Ionic and orientation polarization always require more time compared to electron polarization. Maximum measured value of 51.5 at 1 kHz was reached in composites with 50 volume percent BT content. This is an extremely high value for a simple solution-processed layer. It should be noted that free-standing composite films of even 50 volume % BT content were flexible due to the low glass-transition temperature of the polymer matrix. This also implies a homogeneous dispersion of particles in the polymer, which hinders brittleness. In this state, high-*k* composite layers are fully suitable for application in flexible, printed organic devices.

5.4 Ferroelectric functionalized OFETs: Device Characterization

Transistors were fabricated on glass substrates and HMDS-treated, thermally oxidized n^{++}-silicon wafers (t_{ox} = 300 nm). Source and drain electrodes (Au) were evaporated onto the substrates forming a channel of 26 μm length and 1-2 mm width. In an N$_2$-atmosphere glove-box, regioregular poly(3-hexylthiophene) (rr-P3HT) was dissolved in xylene and filtered with 0.2 μm PTFE-filter. This solution was spin-coated onto the electrodes and annealed at 150ºC in a vacuum oven. Thickness of P3HT layer was around 30 nm, with a roughness value of 4 nm. Pure and composite ferroelectric layers were coated onto the P3HT layer. Therefore the active semiconductor/dielectric interface, which is critical for the charge transport was defined by the roughness of the P3HT layer [82].

In case where Si-substrates were used, it was possible to observe the properties of the semiconductor after the deposition of the composite film onto it. For that, the bottom-gate hybrid configuration was used, where the doped silicon was used as the gate-electrode. Measurements were conducted like in hybrid transistors, discussed in chapter 3. Transistor was measured before and right after the deposition of the composite layer. Since the solvents used to deposit composite layer, acetone and N-metyhlpyrrolidone, are non-solvents for P3HT, its processing only influenced the off current of the bottom-gate transistor by increasing it slightly. This implies a slight shift of the threshold voltage and therefore no destructive interaction of solvents with P3HT. Finally, top gate electrode (Au) was thermally evaporated onto the insulation layer. Fig. 5.6(a) shows the output characteristics of a device with a 2.5 μm thick composite gate-dielectric of 10 volume % BT. Due to the high capacitance at the composite dielectric, we were able to switch the transistor by applying 2 V increments at the gate electrode. However, in the case of a pure polymer dielectric, 10 V increments were needed to reach similar drain current values. Therefore, it can be concluded that the composite layer provides higher capacitance values, without leading to higher leakage currents.
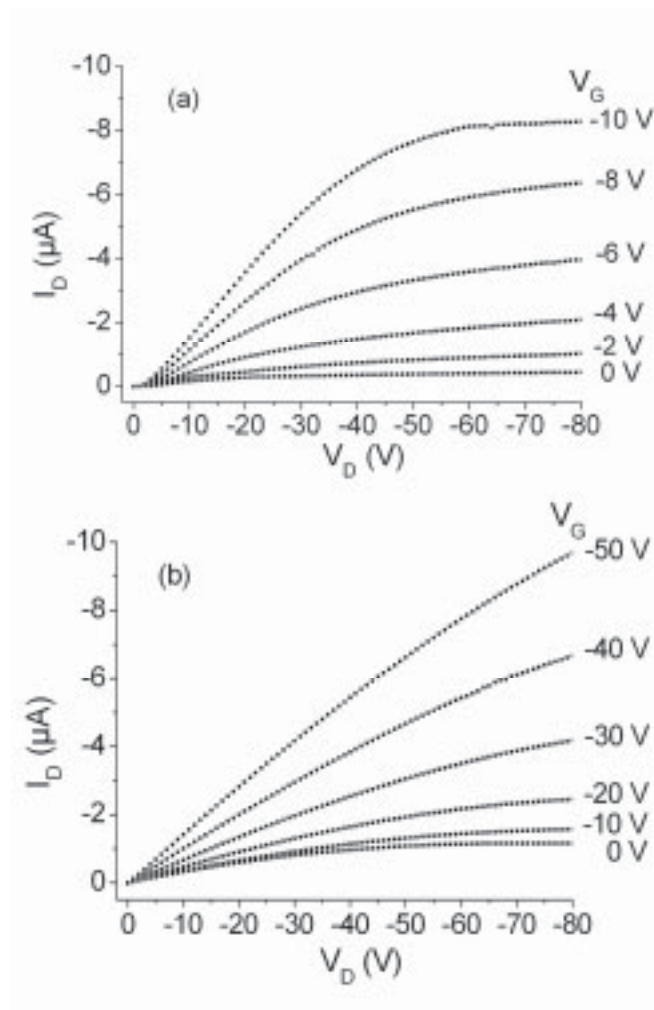
Figure 5.5 (a) Output characteristics of a transistor using a 10 vol. % BT composite dielectric, demonstrating the low-voltage gate switching. (b) The output characteristics of a transistor using a pure PVDF/TrFE dielectric of same thickness value.

In order to observe ferroelectric hysteresis behaviour gate voltages of up to 30 V were applied during the measurement of the transfer characteristics. In Fig. 5.7, transfer characteristics at $V_{ds} = -3$ V and $V_{ds} = -6$ V are presented, where a large ferroelectric hysteresis can be observed. Due to direct depolarization of the ferroelectric, hysteresis was much smaller in the measurements where higher drain-source voltages are applied. A mobility value of $\mu = 2.6 \cdot 10^{-2}$ cm^2 /V s was calculated from the slope of the transfer curve by using the equation for transconductance, g_m. The value for capacitance per unit area was taken as 14.2 nF/cm^2, which was calculated by assuming $\varepsilon_r = 50$ (@100 Hz) measured for this composite from the MIM-structures. 100 Hz value was taken since it represents the closest value to constant voltage conditions that were used to measure the transistor characteristics.
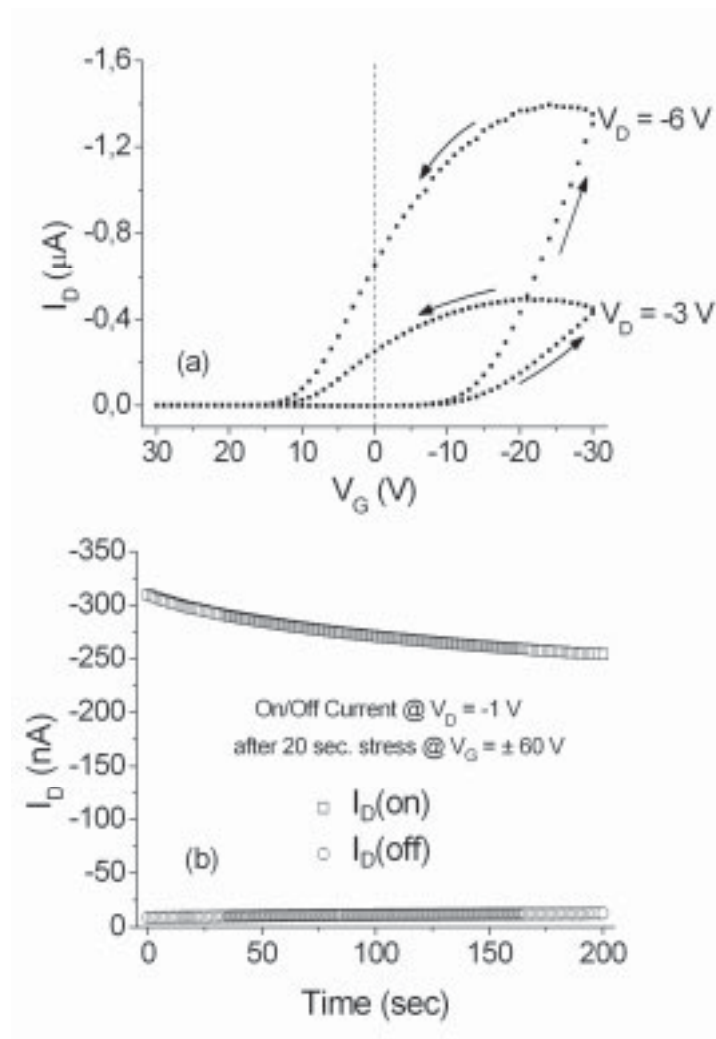
Figure 5.6 (a) Ferroelectric hysteresis behavior exhibited by a transistor with a composite layer of 10 vol. % BT content during the sweeping of the gate voltage. Applied electric field here had a peak value of 12 MV/m. (b) On- and off-state drain current of a device with a 25 vol. % BT composite layer.

After observing the hysteresis behaviour, the on- and off-state drain currents of transistors were measured, for the data retention property. The presented results are from a transistor using a composite layer of 25 volume % BT content. In order to turn the transistor to the on-/off-states, gate-source voltages of respectively -60 V/ +60 V was applied for 20 seconds. Drain current was then measured for 200 seconds at -1 V drain-source voltage. On/off current ratio was measured to be 40 at the beginning, and decreased to 20.5 after 200 seconds. An asymptotic behaviour was observed in both on- and off-currents, which is very similar to the cases presented in other previous efforts [93, 94].

5.5 Conclusion

Pure PVDF/TrFE copolymer and its composites with up to 50 volume percent barium titanate powder content were solution-processed into composite insulator films. Dielectric constant of 15.8 for the pure polymer was increased with increasing barium titanate content, where a maximum dielectric constant of 51.5 at 1 kHz was reached. This is a very high value when the low-temperature processing conditions are considered. Such high values are normally observed in inorganic thin films, which need annealing temperatures over 500 °C. The investigated layers formed defect-free films and also exhibited good insulation properties. This was achieved by the homogeneous dispersion of the BT nanopowder in the PVDF/TrFE polymer solution and the optimization of the processing conditions and solvents.

Ferroelectric functionalized organic field-effect transistors were produced by using both pure PVDF/TrFE and composite insulation layers. Presented devices were by no means optimized or ideal. However, operating voltages of the devices were successfully reduced by the increased capacitance when composite layers were used. In cases of high BT content, film thickness was increased up to 8-12 µm in order to hinder fluctuation of electrical measurement data. Thinner layers were produced where even lower voltage operation was achieved, whereas an optimization with respect to the layer thickness was not made. Therefore optimization of dispersions and film production are still needed for these composite materials.

In the final part of this work, ferroelectric hysteresis behaviour and memory retention properties were presented. Samples showed a large hysteresis in the transfer characteristics, which indicates the spontaneous ferroelectric polarization of composite layers. In various studies presented in literature the optimization of hysteresis curves and memory retention behaviour were demonstrated, whereas this work focused on the contribution of composite layers to the electrical properties. However, the contribution of composite composition to the memory retention and the hysteresis behaviour of the transistors were not quantitatively examined.

6 Conclusions and Outlook

6.1 Conclusions

Organic electronics is an exciting research field that attracts growing interest from institutional and industrial establishments. Uninterrupted reports on successful achievements and extremely innovative research efforts are the driving force of the field, although the field still needs more time to come up with its fascinating products into the market. Nevertheless, it can be said that organic electronics has now completed its initial phase and moving towards its goals in a determined fashion. Scientific contributions of multidisciplinary basis are performed tackling the multifaceted challenges on materials and processing technologies. This interdisciplinary study aimed at broadening the vision of OFET research on materials basis, presenting a systematic materials selection and characterization. It is demonstrated by introducing new insulating materials as well as designing new composite films that there is substantial room for improvement of materials. It is already recognized by many research groups that the ultimate solution to many problems would be overcome by developing new materials and understanding their interaction at interfaces in organic devices [33].

The main topics this study aimed to cover were:

- Understanding and improvement of the performance of hybrid devices by the optimization of semiconductor processing and dielectric/semiconductor interface
- Systematic selection of new materials for solution-processed gate insulators
- Exploring the electrical insulation performance, size limits and surface properties of the selected insulators and optimization of these for the selected OFET configuration
- Investigation and comparison of device performance based on material properties, surfaces, solvents and processing parameters
- Preparation and modification of new high-*k* nanocomposite materials for the reduction of operating voltages
- Demonstration of an all-polymer field-effect transistor by the selected materials
- Demonstration of memory retention and hysteresis behavior in ferroelectric OFETs

Despite the fact that this research was mainly carried out to investigate materials and device properties, a completely solution-processed low-cost all-organic transistor was also demonstrated. In that sense this thesis has also proven the practical applicability of this research considering the materials, methods and the scientific outcome achieved in this work.

The first chapter of experimental work (chapter 3) focused on hybrid organic FETs. The active semiconductor layer P3HT was deposited from solutions of different solvents, via spin-coating. Performance of hybrid devices was improved by optimizing the processing conditions of P3HT and modifying SiO_2 surface by a self-assembled monolayer of HMDS. It is shown how π – orbital overlap in semiconducting polymer can be improved by optimizing the solvent of deposition, dielectric surface and atmospheric factors. During these studies the charge carrier mobility of P3HT devices could be improved by almost two orders of magnitude from 10^{-5} to 10^{-3} cm^2/Vs. Additionally; off-state current values were decreased and threshold voltage was stabilized by the dielectric surface treatment. Surface impurities and defects were prohibited by means of surface treatment. Field effect mobility values of up to $2 \cdot 10^{-3}$ cm^2/Vs together with an on/off current ratio of $2 \cdot 10^5$ was reached, when high boiling point solvents were used to deposit P3HT. Hybrid devices give essential information on the electrical properties of the semiconductor layer. This information was very useful for the understanding of devices with organic dielectrics. In that sense hybrid devices are very efficient devices for the characterization of organic semiconductors.

In chapter 4, an important step was taken towards all-organic devices. Inorganic SiO_2 dielectric traditionally used in hybrid systems was replaced with different organic dielectrics, to demonstrate the possibility of producing OFETs by using simple processing techniques and low temperatures. A careful selection of dielectric materials was conducted, where following materials were selected: Benzocyclobutene (BCB), SU-8 photoresist, Bectron EL37A, Norland Optical Adhesive NOA74. The common property of these four materials is that they are thermosetting polymers, which chemically crosslink and present very good chemical stability after curing. Except BCB, which was used for comparison reasons, selected materials offer the possibility of curing at low temperatures and even only via UV-light. Films of these four materials showed good solvent resistance and low surface roughness, which makes them extremely attractive for bottom-gate OFETs. In metal-insulator-metal capacitors, layers of 1.2μm thickness exhibited excellent insulation properties and dielectric constant values between 3.0 and 4.8.

OFETs were prepared with these dielectric layers by using P3HT. The charge carrier mobility and threshold behavior of devices with different dielectrics were compared. Properties like dielectric surface energy, surface roughness, chemical purity, polarity and interface formation with P3HT has influenced the electrical behavior of transistors. Taking the hybrid devices as reference, it was observed that the devices using polymer dielectrics exhibited higher off-state currents, which decreased the I_{on}/I_{off} current ratio. The increased off-state current indicates an increased conductivity in P3HT, which was attributed to the interaction (doping) with the impurities at the interface. Dielectric surface did not only serve as a substrate for the semiconductor film growth, but also it affected the electrical device properties with the surface states after film formation. Mobility values of up to $8.0 \cdot 10^{-4}$ cm^2/Vs were demonstrated with the dielectric EL37A. These observations were also confirmed by the experiments by producing devices with pentacene as the semiconductor. Threshold voltage and mobility values of - 21 V ($2.1 \cdot 10^{-2}$ cm^2/Vs) and +16 V ($1.2 \cdot 10^{-2}$ cm^2/Vs) were observed for BCB and SU-8 dielectrics respectively. Although mobility values differed slightly, there was a significant difference in threshold behavior, which affects device characteristics significantly. This difference came from the surface properties of dielectric. Low-polarity and high-purity of BCB formed a more desirable interface with pentacene. Bectron EL37A and SU-8 were introduced into OFET research as new dielectric materials. The significance of the choice of dielectric material is once more pronounced in this study.

In the final experimental chapter (chapter 5), ferroelectric PVDF/TrFE copolymers and their composites with BT nanopowder were used instead of dielectric layers. By the optimization of depositing solvents and processing parameters, smooth films of pure polymer and composite materials were produced. BT nanopowder improved the dielectric permittivity of the films. Composite films exhibited permittivity values of up to 51.3. It should be noted that this is an extremely high value for a low temperature dried, solution-processed layer. By using these layers in transistors, operating gate voltages could be lowered by 80%. The spontaneous polarization of ferroelectric layers caused the gate capacitance remain charged even upon removal of the gate voltage. This was demonstrated successfully in the hysteresis behavior and the memory retention properties with time.

6.2 Outlook

Reproducibility has been one of the greatest challenges in OFET research, due to the nature of polymeric materials and solution-processing conditions. Reproducibility problems were also observed along with this thesis. In addition to the fact that P3HT is extremely sensitive to light and oxygen, the devices using polymer dielectrics also did not return the same electrical performance every time. The parameters which could affect reproducibility should be explored individually by a systematic experimentation.

In this study a materials selection was carried out for organic dielectric layers considering the basic requirements in bottom-gate OFETs. The next step in materials selection could be the design and "customization" of organic dielectrics for the selected semiconductor. Molecular design of the dielectric considering the solvents and the type of semiconductor would return successful devices. A common problem of organic devices, which is the interaction of dielectric with the semiconductor could be solved this way [29, 119]. In the demonstrated OFETs the off-current levels were higher than those in hybrid devices, although the device configurations were similar. The probable reasons (interface, impurities) are addressed in chapter 4, whereas a detailed research could be conducted to determine and understand the exact causes of interface doping. This research would reveal the required conception to further improve device properties. The starting point, which is the comparison of polymer dielectric devices with hybrid devices, was set within this thesis. Apparently, polymer dielectrics can not form a good interface with the required purity and homogeneity with P3HT, although they were tested to be chemically resistant to solvents. The perfect interface model was observed from hybrid devices with HMDS surface treatment. It is therefore plausible trying to imitate, or reach the performance of hybrid devices with organic dielectrics.

Detailed electrical properties of polymer devices should be investigated for the active charge transport mechanisms and the contribution of interface traps to the transport. C-V investigations from MIS devices, and other innovative physical methods such as interferometry and optical or electron microscopic inspection would be useful to explore interface issues. Furthermore, elaboration on contact resistance with various semiconductors also helps understanding and improving the device behavior.

Another interesting research topic which could benefit from further investigation would be on PVDF/BT composite layers for ferroelectric functionalized OFETs. First of all the influence of BT nanopowder size could be altered to optimize device properties. In this work powder particles of approximately 100 nm size were used. It is possible to synthesize finer particles, which could create finer, better dispersions and therefore homogeneous layers. By means of such a study also powder size-effects on electrical properties could be discovered. Even better dispersions could be produced by organic functionalizing BT powder. Similar methods have already been utilized for fullerenes and carbon nanotubes. Second fruitful work would be to elaborate on the effects of tetragonal (ferroelectric) BT particles on the performance of ferroelectric layers. In this work, cubic BT powder was used to improve the polarization properties. With the help of tetragonal crystals, also ferroelectric properties could be improved.

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List of Abbreviations

AFM	Atomic force microscope
BC, TC	Bottom – contact, top – contact
BCB	Benzocyclobutene
BG, TG	Bottom – gate, top – gate
BT	Barium titanate
CTC	Charge transfer complex
CYEPL	Cyano etyhl pullulan
F8T2	poly[9,9-dioctylfluorene-co-bithiophene]
HMDS	Hexamethyldisilazane
HOMO	Highest occupied molecular orbital
ITO	Indium tin oxide
LUMO	Lowest unoccupied molecular orbital
MIM	Metal – insulator – metal
MIS	Metal – insulator – semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
NMP	N-methyl pyrrolidone
NMR	Nuclear magnetic resonance
OFET	Organic field-effect transistor
OLED	Organic light emitting diode
P3AT	Poly(3-alkylthiophene)
P3HT	Poly(3-hexylthiophene)
PANI	Polyaniline
PCBM	Methanofullerene
PEDOT-PSS	Poly(3,4-ethylene dioxythiophene) – Poly(styrene sulfonate)
PHEMA	Poly(hydroxyethyl methacrylate)
PMMA	Poly(methyl methacrylate)
PQT	Poly(quarter thiophene)
PS	Polystyrene
PTAA	Poly(triarylamine)
PTFE	Poly(tetrafluoroethylene)
PTV	Poly(thienylene vinylene)

PV	Peak – to – valley
PVA	Poly(vinyl alcohol)
PVAc	Poly(vinyl acetate)
PVC	Poly(vinyl chloride)
PVD	Physical vapor deposition
PVDF	Poly(vinylidene fluoride)
TrFE	Trifluoroethylene
PVP	Poly(vinyl phenol)
RF-ID	Radio frequency identification
S/D	Source and drain
SAM	Self-assembled monolayer
TCB	1,2,4 - trichlorobenzene
TFT	Thin-film transistor
WIM	White-light interferometer

Acknowledgements

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