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SiGe HBT ICs with High Operational to Transit Frequency Ratio: Design and Design Re-use

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SiGe HBT ICs with High Operational to Transit Frequency Ratio: Design and Design Re-use

DISSERTATION

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von

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So little space for so many people to thank ...

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To my father, Jean-Pierre Chartier

Contents

Chapter 1

Introduction

The millimeter-wave (mm-wave) region of the electromagnetic spectrum covers the range of wavelengths from one centimeter to one millimeter. It corresponds to radio band frequencies of 30 GigaHertz (GHz) to 300 GHz (by extension, 24 GHz is also often considered as part of the mm-wave domain). The high frequency of mm-waves as well as their propagation characteristics make them a real asset for a variety of applications including high-data-rate wireless communication systems [1], and Radio Detection and Ranging (radar) [2].

An essential advantage of mm-waves is the possibility to transmit large amount of informations with a small ratio $\frac{BW}{f_o}$ (where BW is the assigned bandwidth of the application and f_o its center frequency). Therefore consumer electronics in the mm-wave domain will allow in the future the transmission of e.g. video data suitable for high-definition television (HDTV) [3].

Radar sensors take advantage of the mm-waves. Due to the shorter wavelength, significantly smaller antenna dimensions are required in e.g. a collision-avoidance automotive radar, which might lead in the future to fully integrated systems including on-chip antenna [4].

The mm-wave domain presents a large spread in atmospheric attenuation. A wide spectral window centered around 35 GHz allows the realization of long range communication systems. At 60 GHz, the oxygen molecules will interact with the electromagnetic radiation and absorb a large amount of energy. This means that while 60 GHz is not a good frequency for long-range radar or long-range communication systems, it is perfectly suitable for short-range communications, such as local wireless area networks used for portable computers [5]. Another possible application operating at 60 GHz is a communication system between satellites in high earth orbit.

Another benefit of mm-waves is the low amount of currently existing applications, which

drastically reduces the chances of interference.
Now that various advantages of mm-waves have been highlighted, the question of suitable technologies remains.
In the late 1980s, Silicon (Si) bipolar technologies reached their limit with transit frequencies (f_T) around 30 GHz. At that time, the compound semiconductor industry was leading the market of applications operating in the millimeter-wave domain. In the early 1990s, the first SiGe heterojunction bipolar transistors (HBTs) came out of the research laboratories and entered production [6–8]. Since then, the technologies have improved and reached outstanding speed performance with f_T far above 300 GHz and even 500 GHz under certain conditions [9]. These advances toward higher speed make SiGe HBTs one of the greatest competitor of III-V compound semiconductor devices such as High Electron Mobility Transistors (HEMTs) in area such as optical fiber transmission systems, high data-rate wireless communications, and radar. While III-V compound semiconductors suffer from major issues such as high cost, low integration density and even yield problems for advanced technologies, SiGe bipolar technologies overcome all these problems [10].
Unfortunately, SiGe bipolar devices require a large amount of masks during fabrication process which leads to high cost if a low amount of integrated circuits (ICs) is required. This aspect is progressively worsened because of complex devices containing features that allow to improve their speed and to decrease critical parasitics (such as e.g. substrate coupling using deep trench isolation). Another critical issue of very high-speed SiGe HBTs is their low breakdown voltage, which inevitably leads to a lower power capability for transmitters. As a rule of thumb, battery based applications (such as mobile phone) should use technologies with an f_T at least ten times higher than the f_{op} (where f_{op} is the operational frequency of the application) and applications which are not using batteries should be designed with technologies with an f_T of at least three times the f_{op}. However, using specific topologies, these barriers can be broken, thus leading to a drastic cost reduction. Circuit topologies which are capable of achieving such performance are emphasized in this work. These ICs were developed through several projects and therefore operate at different frequencies. But more importantly, all these ICs achieved a high f_{op}/f_T ratio.
In order to significantly decrease the cost of an IC, special emphasis can be placed on design re-use and reconfigurability. The layout of an IC can be designed in a way that easy modifications can be made in future designs. In this way, once a design has been successful and the accuracy of its simulation has been demonstrated, it will be possible to use it as a foundation to develop other similar ICs operating at different frequencies. By reducing the amount of redesign steps and modified masks, drastic cost and time reduction can be achieved. This design aspect will be described as well.

Because the presented circuits were designed to be implemented in a super heterodyne receiver or in a short range automotive radar, the next chapter gives an overview of possible architectures. Then, the technologies used to design the ICs will be presented. Afterward, because reactive elements with inductive behavior were realized using thin-film microstrip lines or on-chip spiral inductors, a chapter will be dedicated to these two elements and to their implementation in the simulation environment. Finally, the four main blocks of an RF front-end of a super heterodyne receiver and a short range automotive radar (amplifiers, VCOs, mixers, frequency dividers) will be described in details.

Chapter 2

Super Heterodyne Receiver and Automotive Radar

2.1 Introduction

As previously explained in Chapter 1, the developed ICs were realized for a wide range of applications which, however, can be narrowed down to two major system architectures: the superheterodyne receiver (SHR) and the frequency modulated continuous wave (FMCW) radar. In order to give a brief overview of the systems on which the circuits will be implemented in the future, a chapter is dedicated to these two approaches.

2.2 Super heterodyne receiver

The SHR [11] was invented by Armstrong and patented in 1918. In the SHR, a weak incoming RF signal at frequency f_{RF} is amplified using a LNA and then converted to a lower frequency (f_{IF}) using a local oscillator (LO) and a mixer. The signal with frequency f_{IF} is then demodulated to recover the initial data. A block diagram of a potential mm-wave SHR front-end is presented in Fig. 2.1. As can be seen, the receiver is fully differential. This is highly recommended for silicon based technologies in order to reduce the influence of packaging, which may be very critical and costly at this frequency range [12]. The advantages of such an approach are:

- On-chip noise generation is substantially reduced [13, 14]
- Clock generation in optical fiber systems is simplified due to the differential clock input of the driven circuits [15].

- Decoupling of supply and bias voltages is less critical due to the virtual ground nodes [16].
- Virtual ground nodes allow the realization of adjustable on-chip inductors (discussed in Chapter 5). Hence, the same IC can be used for different applications in a wide frequency range.

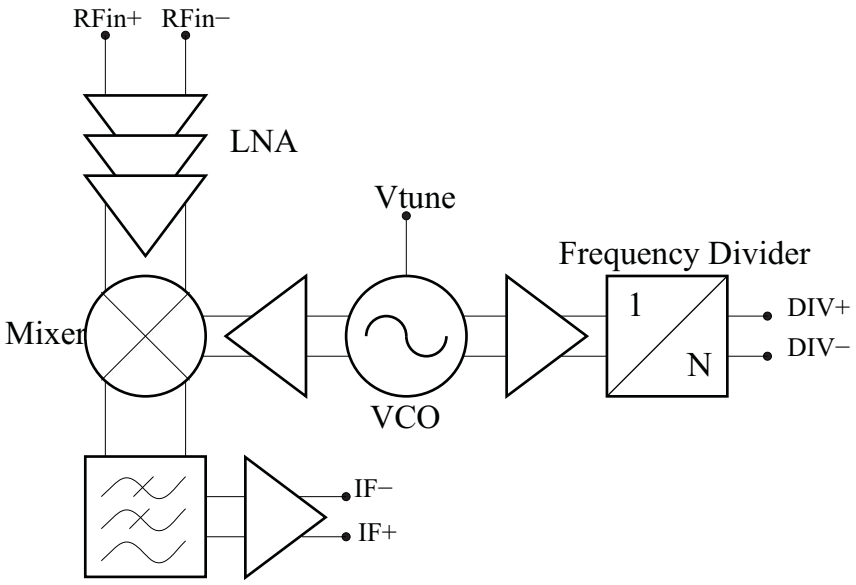

Fig. 2.1: Block diagram of a potential millimeter-wave SHR front-end

The use of a frequency divider is necessary to build a phase lock loop (PLL). This addition is not mandatory, however the implementation of a PLL leads to a drastic improvement of the oscillator phase noise as well as frequency stability and therefore to a higher overall performance of the SHR.

2.3 Short range and long range automotive radar

At the beginning of the third millennium, each year worldwide, over one million persons are killed in traffic and over 50 million are injured. In Germany alone, in 2001 over two million accidents resulting in almost 500 000 casualties occurred. The table 2.1 gives an overview of the accidents and the resulting casualties and deaths that occurred between 2001 and 2003 in Germany [17].
An important study was recently performed to try and understand the reasons of these traffic accidents worldwide [18]. The table 2.2 gives a very good insight to explain the great interest in automotive radar. As it can be seen, all accidents in categories marked

	2001	2002	2003
Number of vehicles	52 487 300	53 305 900	53 655 800
Number of accidents	2 373 556	2 289 474	2 259 567
Number of accidents with casualties	375 345	362 054	354 534
Number of casualties	494 775	476 413	462 170
Number of deaths	6 977	6 842	6 613

Tab. 2.1: Overview of the accidents occurring in Germany between 2001 and 2003

reason	percentage
Inattentiveness of the driver	68 % $\surd$
Driver driving too close from the front vehicle	9 % $\surd$
Driver driving too close from the front vehicle and inattentiveness	11 % $\surd$
Alcohol	9 %
Other	3 %

Tab. 2.2: Overview of the reasons resulting in car accidents

with a $''\surd''$ could be avoided or at least drastically reduced by using radar sensors.
Research on automotive radar had already begun in the early 1970s [19]. However, such systems were only implemented e.g. in the class-S of Mercedes at the very end of the 20th century. In 1999 the first automotive long range radar (LRR) sensors operating at 76.5 GHz were introduced for adaptive cruise control (ACC). Furthermore in autumn 2005, the first cars equipped with 24 GHz short range radar (SRR) sensors in combination with a 76.5 GHz LRR sensor were brought onto the market enabling new safety and comfort functions such as e.g. stop-and-go operation, autonomous pre-safe braking, pre-crash warning, and parking assistance. Future advanced driver assistance functions are under way. In Europe, however, the 24 GHz ultra wideband (UWB) frequency band is only temporarily allowed until end of June 2013 with a maximum fleet penetration rate of 7% [20]. This limitation is due to the fact that the SRR radar is sharing the frequency band with other applications such as radioastronomy and this can lead to highly critical interference (the incoming signal in radioastronomy applications is always extremely weak). From the mid-2013 new cars will have to be equipped with SRR sensors operating in the frequency band from 77 GHz to 81 GHz [21].
The most adopted system architecture for SRR is the FMCW radar [22]. This is a system where a continuous wave radio energy with known stable frequency is modulated by a triangular modulation signal so that it varies gradually. This signal is then mixed with the signal reflected from a target to produce a beat signal. Variations of modulation are possible (sine, sawtooth, etc), but the triangle modulation is used in FMCW radars

where measurements of both range and velocity are desired, as in ACC systems. The beat signals are passed through an Analog to Digital Converter (ADC), and digital processing is performed on the result. FMCW radars can be built with one antenna using e.g a circulator. Many modern systems use separate transmitter and receiver antennas. Because the transmitter is on continuously at effectively the same frequency range as the receiver, special care must be exercised to avoid saturating the receiver stages. A block diagram of a potential 77-81 GHz SRR front-end architecture is presented in Fig. 2.2.

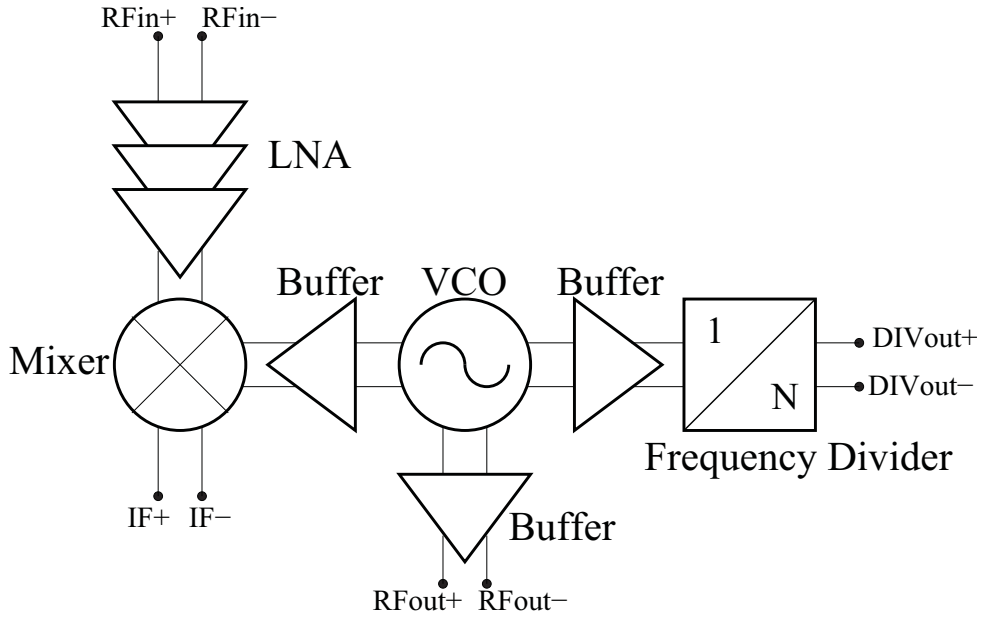

Fig. 2.2: Possible topology of a 77-81 GHz SRR front-end architecture

In this configuration, the VCO drives three output buffers which are connected to a frequency divider, the transmit antenna (RF_{out+} and RF_{out-}) and a down-converter mixer. The frequency divider is used to build a phase-locked loop (PLL) which is necessary to improve the phase noise of the VCO. As it can be seen, the topology of the whole FMCW radar is differential. The motivation for such approach was previously presented in Section 2.2.

Chapter 3

SiGe Heterojunction Bipolar Technologies

For this work, two technologies were available: the second generation of Atmel's SiGe HBT technology (SiGe2RF) and IHP's high-speed SiGe BiCMOS technology (SG25H1). The first one was used for designing high performance mm-wave ICs operating below 50 GHz. Because of the stringent requirements of the 77-81 GHz SRR, a faster technology was necessary. Therefore the 0.25 μm SiGe BiCMOS process of IHP had to be used. In this chapter, a brief description of these two technologies is provided.

3.1 Atmel's SiGe HBT technology

The second generation of Atmel's SiGe technology was presented for the first time in [23]. This technology brings several modifications compared with the first generation (SiGe1), therefore leading to a substantial performance improvement. The main features of the technology are highlighted here.
In order to obtain a faster device, a first technique consists in reducing the lateral dimensions of the transistor. This was performed by reducing the effective emitter width from 0.8 μm (1.1 μm drawn emitter width) to 0.5 μm (0.8 μm drawn emitter width). The effective base thickness was also reduced in order to achieve higher f_T.
Another important aspect of this device is the constant Germanium (Ge) content in the base. The high Ge mole fraction (20 %) allows a high base doping concentration due to the wide-gap emitter effect, which in term provides for a high maximum frequency of oscillation and low microwave noise despite the relaxed emitter scaling.
One of the most important feature of the SiGe2RF process is the selective implanted

collector (SIC). The SIC technique allows to achieve a high collector doping in the intrinsic collector while keeping low the extrinsic collector doping. Hence, it is possible to improve the trade-off between f_T and collector-base capacitance (one of the most critical parasitic capacitance, mostly because of its influence on f_{max}). Another transistor type is implemented within the technology without SIC but with higher BV_{CEo}. Isolation of a device from all the adjacent devices (very critical in highly integrated ICs) is mandatory. In SiGe1, a recessed local oxidation of Silicon (LOCOS) was used to improve isolation. In SiGe2RF, a more advanced isolation technique was implemented in the process: the shallow trench isolation (STI). The STI process is performed by etching a pattern of trenches in the silicon and depositing $Si(C_2H_5O)_4$ also called tetraethoxysilane (TEOS) to fill the trenches and removing the dielectric excess using a chemical-mechanical polishing technique (CMP).
Using the aforementioned techniques and features, the SIC-NPN SiGe HBT transistors reach an f_T of 80 GHz and an f_{max} of approximately 90 GHz with a BV_{CEo} of 2.5 V. Additionally, the technology features three aluminum (Al) metal layers, four types of resistors with different sheet resistances, MIM and Nitride capacitors as well as several types of diodes. The chosen transistor model is the HIgh-CUrrent Model, more commonly called HICUM [24]. The table 3.1 summarizes some of the key figures of Atmel's SiGe2RF technology.

NPN HBTs	SIC (f_T/f_{max}/BV_{CEo}: 80 GHz/90 GHz/2.5 V) non-SIC (f_T/f_{max}/BV_{CEo}: 50 GHz/90 GHz/4 V)
lateral PNP	1 (not suited for RF)
Metal layers	3 (Al) and scalable model for spiral coils
Resistors ($\Omega/\square$)	4, 150, 500, 1500
Capacitors	MIM (0.93 fF/μm^2)/ Nitride (1.1 fF/μm^2)
Diodes	Schottky, Zener, ESD, varactor

Tab. 3.1: Overview of Atmel's SiGe2RF technology

3.2 IHP's SiGe BiCMOS technology

IHP's SG25H1 BiCMOS technology was presented in [25]. In this process the HBT module is introduced after gate spacer formation and before CMOS source/drain implantation. The bipolar module is constructed without epitaxially buried subcollector and deep trenches (at the opposite of many technologies such as e.g. [26]). The most innovative device features are the formation of the whole HBT structure in one active area

without STI between emitter and collector contacts and the complete lateral enclosure of the highly doped collector wells by STI side walls. This approach significantly reduces device dimension, collector resistance and parasitic capacitances. The standard HBTs have a drawn emitter width of 0.25 μm, f_T/f_{max} values of 190/190 GHz (at V_{CE} = 1.5 V) and breakdown voltage BV_{CEo}=1.9 V. The chosen model is the Vertical Bipolar Inter-Company model, usually called VBIC [27].
Beside this new type of transistors, the technology features four aluminum metal layers as well as an optional fifth thick Al metal module for high-Q transmission lines or lumped elements, silicon nitride (SiN) MIM capacitors with a capacitance density of 1 fF/μm^2, four types of polysilicon resistors and MOS varactors.
The table 3.2 gives a brief summary of IHP's high-speed BiCMOS technology.

NPN HBTs	NPN1 ($f_T/f_{max}/BV_{CEo}$: 190 GHz/190 GHz/1.9 V) NPN2 ($f_T/f_{max}/BV_{CEo}$: 180 GHz/220 GHz/1.9 V)
Metal layers	4 (Al) and optional 5^{th}
Resistors ($\Omega/\square$)	7, 210, 280, 1600
Capacitors	MIM (1 fF/μm^2)
Varactor	MOS

Tab. 3.2: Overview of IHP's SG25H1 technology

Chapter 4

Reactive Elements on Lossy Silicon Substrate

4.1 Introduction

In order to realize precise and reliable simulations, both modeling of reactive elements and deembedding of components placed within a test structure for on-wafer characterization have to be carefully performed. This chapter describes the simulation, measurements and modeling of thin-film microstrip lines which were widely used in this work. A short overview of spiral inductors is also provided.

4.2 Thin-film microstrip lines on lossy silicon substrate

4.2.1 Potential transmission line topologies for implementation on a low-resistivity Si substrate

Because silicon devices are now capable of operating at frequencies far beyond 30 GHz, thin-film microstrip lines (TFMSLs) have gained momentum recently and start to be implemented in prototype MMICs. TFMSLs are miniaturized microstrip lines placed on top of the Si substrate. A fundamental advantage of this approach is that the ground plane placed below the line shields it from the substrate. Therefore, low resistivity Si substrate can still be used without deteriorating the overall performance of the IC.
Before presenting ICs using TFMSLs, it is important to give an overview of previously

investigated line topologies in order to justify the use of such line type.

Coplanar waveguide lines and conductor backed coplanar waveguide lines: These line types were presented in e.g. [28]. In this work, the authors used the top metal layers to design the coplanar waveguide (CPW) line (a cross-section describing a CPW is presented in Fig. 4.1).

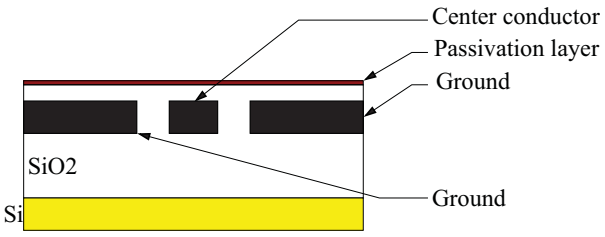

Fig. 4.1: Cross-section of a coplanar waveguide on a Si substrate (not to scale)

After measurements performed up to 110 GHz, it was demonstrated that the designed 50 Ω CPW line shows high loss (approximately 30 dB/cm at 30 GHz, which is five times higher than the losses of the TFMSLs measured in the same publication) therefore proving the little promise of this approach on low resistivity silicon substrate. This very high loss is mostly associated with parasitic conductance in the low-resistivity substrate. Such results can be easily transfered to any SiGe HBT/BiCMOS technologies due to the similarity of their metal systems (the oxide layer is always only a few micrometers thick). A high-resistivity Si substrate could be used to solve this problem. However, the combination of the signal line together with the field oxide and the silicon surface creates a parasitic MOS diode which can generate an inversion channel at the SiO_2/Si interface.
In [28], the conductor backed CPW (see cross-section in Fig. 4.2) line was not even fabricated. It was shown by simulation that the small oxide thickness separating the metal layers would lead to a center conductor smaller than that which is allowed by design rules to avoid the domination of the microstrip mode.

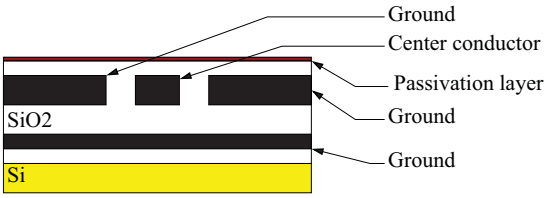

Fig. 4.2: Cross-section of a conductor backed coplanar waveguide on a Si substrate (not to scale)

Inverted microstrip lines:
Inverted microstrip line performance at high frequency (>20 GHz) was reported for the first time in [29] (a cross-section of an inverted microstrip line is presented in Fig. 4.3).

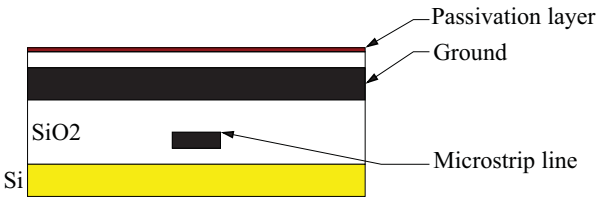

Fig. 4.3: Cross-section of an inverted microstrip line on a Si substrate (not to scale)

In this study, the elements were designed to show an impedance of 50 Ω and were fabricated on a standard low resistivity silicon substrate (20 Ω.cm) and characterized up to 50 GHz. The measurements performed on these lines showed a behavior (the attenuation increases at a higher rate than expected) which was explained by the presence of higher order modes at high frequency and the occurring coupling between these modes. It was therefore demonstrated that embedded inverted microstrip lines are not suitable for use beyond a few GHz. This topology was therefore not chosen for this work.
Thin-film microstrip lines:
TFMSL characterization and modeling were already presented in e.g. [28] and [30]. In [28], 50 Ω lines were realized by using 7 μm wide elements with different lengths. The ground plane was periodically slotted for planarity at higher physical level. The narrow width of the TFMSL is again explained by the thin oxide thickness (3.24 μm in this study). Two main different studies were performed. First the losses were characterized and then the influence of the ground plane width was evaluated. It was presented that the 50 Ω TFMSL has moderate losses and that for a ground plane width of more than three times the line width, the losses remain constant (for narrower ground plane, the losses increase significantly).
Therefore, based on the previously described studies, it can be concluded that TFMSLs are the most appropriate choice. Another great advantage of TFMSLs is the possibility to modify their electrical length on-chip. This design aspect is depicted in Section 5.3.2. The following section shows both the electromagnetic (EM) simulation of the TFMSLs using Atmel's SiGe80G technology [1] and the performance of these lines.

[1]The SiGe80G is a 0.35 μm SiGe HBT technology currently under development at Atmel Germany. IC measurements were not performed on this technology. However, due to the large available area (2x2 cm^2), very long and wide test structures could be implemented. Therefore, the TFMSL study was performed on this technology

4.2.2 Simulation of the TFMSLs

TFMSLs have very simple geometries but remain very difficult to simulate accurately. This is simply due to the very thin oxide layer, which has a thickness that can be compared with the one of the line (a comparison between TFMSL and standard microstrip line is presented in Fig.4.4). The common assumption of zero-thickness metal layers is therefore not allowed here.

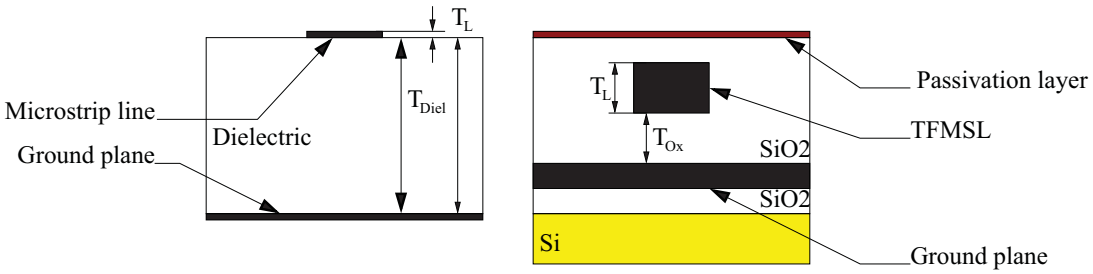

Fig. 4.4: A comparison between standard microstrip line (left) where $T_{Diel} >> T_L$ and TFMSL (right) where $T_{Ox} \sim T_L$ (cross-section not to scale)

Currently, two major types of EM field simulation tools are available: $2\frac{1}{2}$ dimensional ($2\frac{1}{2}$ D) and 3 dimensional (3D). 3D tools provide very good accuracy, however they remain complex to handle and often require a critical computation time. $2\frac{1}{2}$ D simulation tools only simulate planar conductor (with a "zero thickness"). However, the required simulation time is short and the accuracy remain acceptable. Therefore, the line simulations were performed using $2\frac{1}{2}$ D tools (momentum and sonnet). As previously mentioned, TFMSLs and oxide thicknesses are of the same order. Therefore the "zero thickness" approach provided by the $2\frac{1}{2}$ D tools is problematic. However, since recently, an option which approximates the behavior of a thick metal is included which makes these EM field solvers accurate enough for our purpose.
The following measurements, simulations and modeling were performed on Atmel's SiGe80G technology. Because of the similarity between metal systems of SiGe bipolar technologies, this study can be very easily transposed to another process. A cross-section of Atmel's SiGe80G metal system is presented in Fig.4.5. In order to perform a detailed study of the TFMSL behavior, a wide range of TFMSL geometries was studied. Because of the availability of an extremely wide area on the reticle, very long TFMSLs were laid out and characterized. The designed microstrip lines have lengths of 100 μm, 250 μm, 500 μm, 1000 μm and 5000 μm and widths of 2.8 μm (minimum allowed line width), 3 μm, 4 μm, 5 μm, 6 μm, 7 μm, 10 μm, 15 μm and 20 μm. The graphs provided in Fig. 4.6, 4.7 and 4.8 show the comparison between the measurements and simulation of a 5000 μm long

and 3 μm wide line.

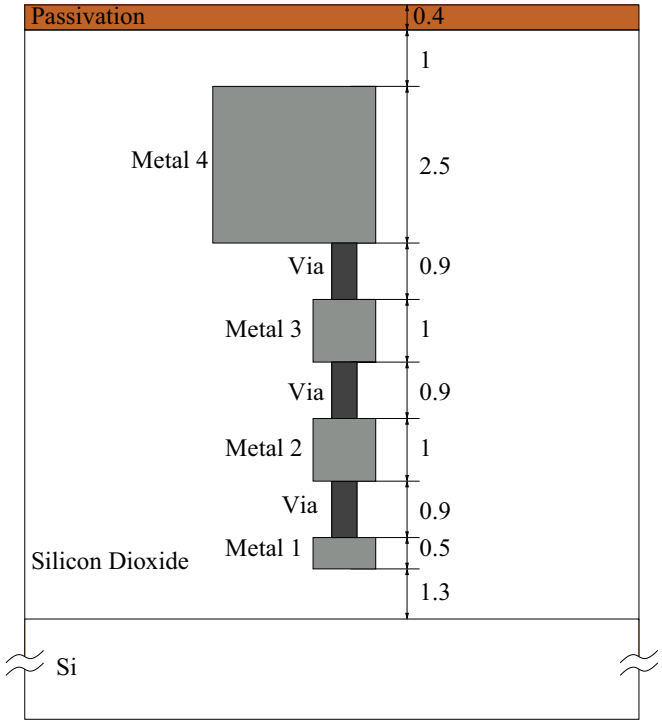

Fig. 4.5: Cross-section of Atmel's SiGe80G metal system (all figures are in μm)

As it can be seen, simulation and measurements agree very well, even for such a long line (it should be noted that a 5 mm long line will never be used for IC design at millimeter wave). From these S-parameters, characteristic impedance, effective relative permittivity, V_{ph}/C_0 and attenuation constant were extracted using the concept of even- and odd-mode

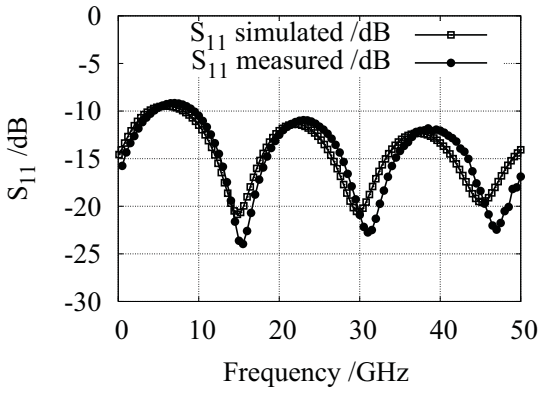

Fig. 4.6: Measured and simulated reflection coefficient of a 5000 μm long and 3 μm wide line

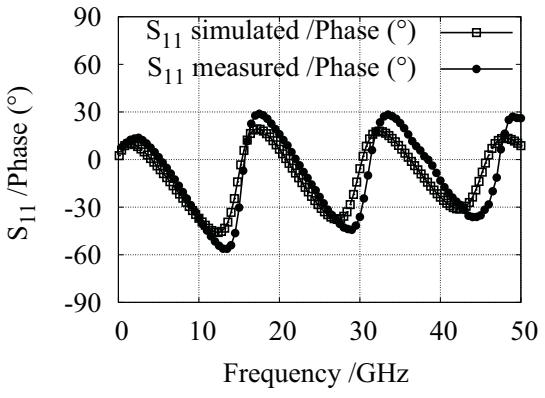

Fig. 4.7: Measured and simulated reflection coefficient (phase) of a 5000 μm long and 3 μm wide line

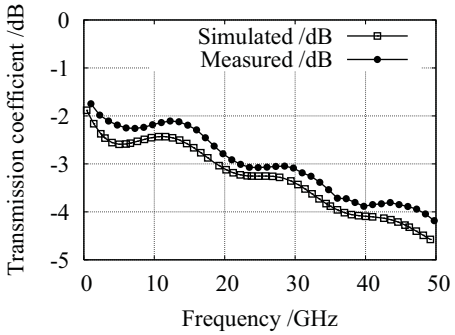

Fig. 4.8: Measured and simulated transmission coefficient of a 5000 μm long and 3 μm wide line

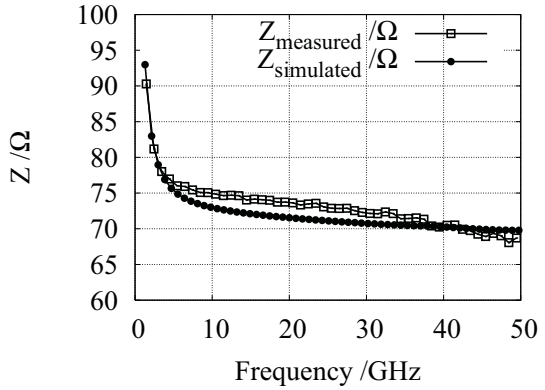

Fig. 4.9: Characteristic impedance extracted from the S-parameter measurements and simulation of a 1000 μm long and 3 μm wide TFMSL

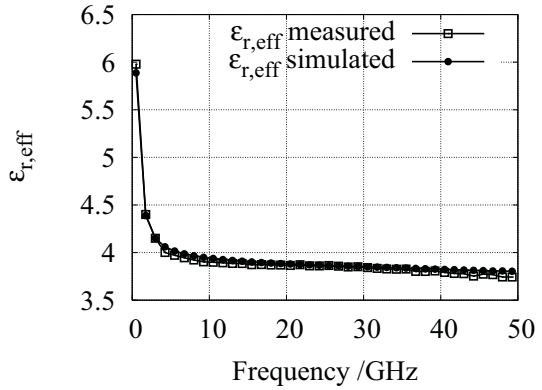

Fig. 4.10: Effective relative permittivity extracted from the S-parameter measurements and simulation of a 1000 μm long and 3 μm wide TFMSL

excitation presented in e.g. [31] and [32]. The measured and simulated extracted parameters on a 1000 μm long and 3 μm wide line are presented in Fig. 4.9, 4.10, 4.11 and 4.12. As expected, the extracted parameters from the simulated and measured S-parameters fit very well. It should be noted that the comparison between simulations and measurements was performed on all created TFMSLs in order to get a wide overview on the simulation accuracy. Similar performance was obtained for each designed geometry. This shows that $2\frac{1}{2}$ D EM tools can be relied on for future simulations. However, because during the IC design procedure a fine tuning of the line length is often required and because of the necessary computational time, it was mandatory to generate a scalable model to speed up the design procedure of the ICs. The created model and its accuracy are described in the following section.

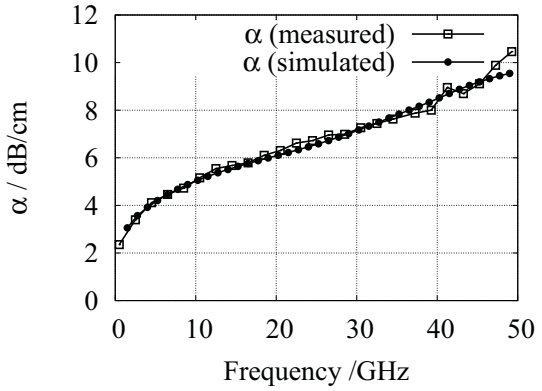

Fig. 4.11: Attenuation constant extracted from the S-parameter measurements and simulation of a 1000 μm long and 3 μm wide TFMSL

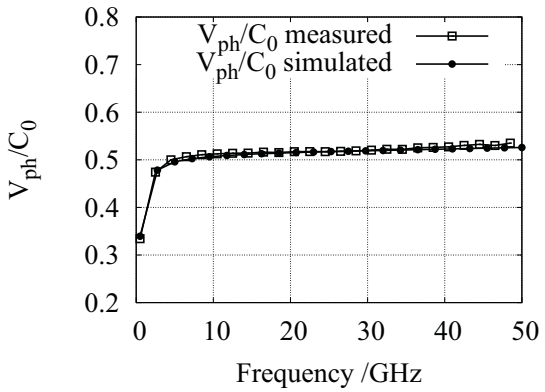

Fig. 4.12: V_{ph}/C_0 extracted from the S-parameter measurements and simulation of a 1000 μm long and 3 μm wide TFMSL

4.2.3 Modeling of the TFMSLs

A model only scalable in length was perfectly sufficient for this work. The equivalent circuit of the lines was based on a Π model. A schematic of the model is presented in Fig. 4.13. The impedance Z_S and admittance Y_P are calculated in the following way:

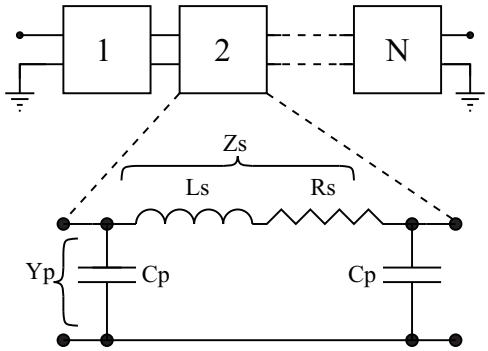

Fig. 4.13: Schematic of the TFMSL model

$$Z_S = \frac{R_s + j\omega L_s}{N}$$

$$Y_P = \frac{j\omega C_p}{N}$$

Where N (integer) is the amount of cascaded single cells necessary to simulate the distributed nature of the line (N=10 in this work). The different elements of the model are

then determined using the following equations.

$$R_S = R_0 \times \sqrt{1 + \frac{f}{f_c}} \times \ell$$

$$L_S = (L_0 - L'_v \times f) \times \ell$$

$$C_P = (C_0 + C'_v \times f) \times \ell$$

Where ℓ is the length of the TFMSL, f is the frequency, L_o and C_o are inductances and capacitances and L'$_v$ and C'$_v$ are inductances and capacitances normalized to frequency. The different parameters of the model components (R_0, f_c, L_0, L'_v, C_o and C'_v) are then determined using the procedure presented in Fig. 4.14.

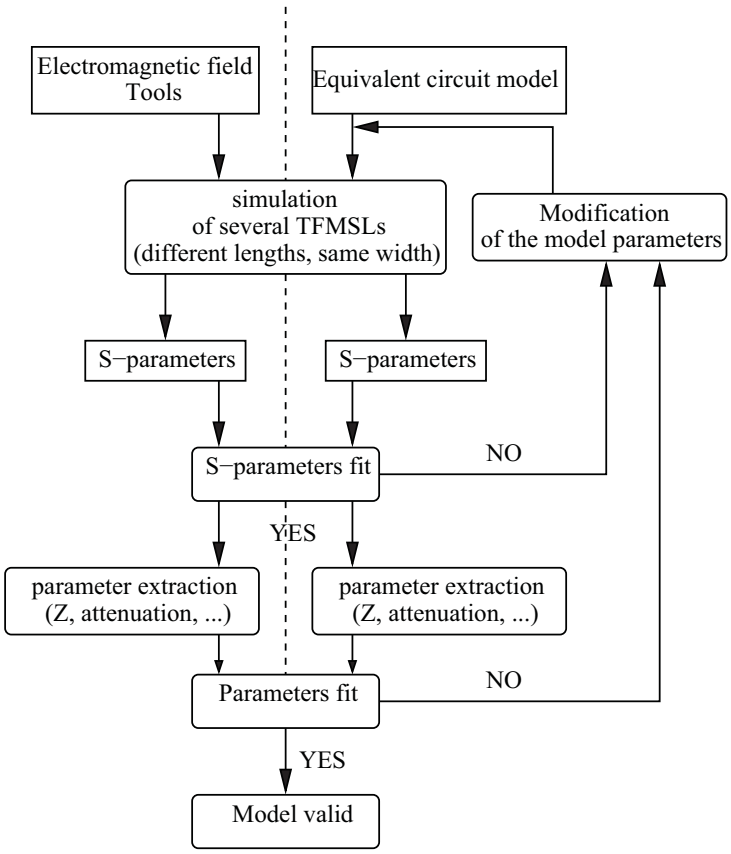

Fig. 4.14: Procedure used to determine the parameter values of the utilized model

A comparison of the simulated and measured TFMSL parameters is presented in Fig. 4.15, 4.16, 4.17 and 4.18. As can be seen, the model fits extremely well with the simulation results. Therefore, highly accurate simulations can be performed and the limits of the used technologies can be explored.

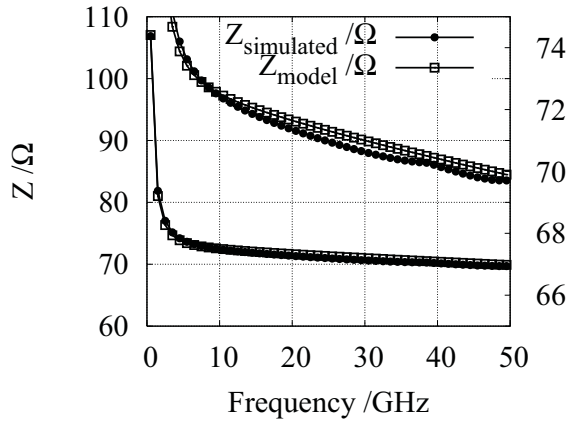

Fig. 4.15: Characteristic impedance extracted from the S-parameters (simulation and model) of a 1000 μm long and 3 μm wide TFMSL

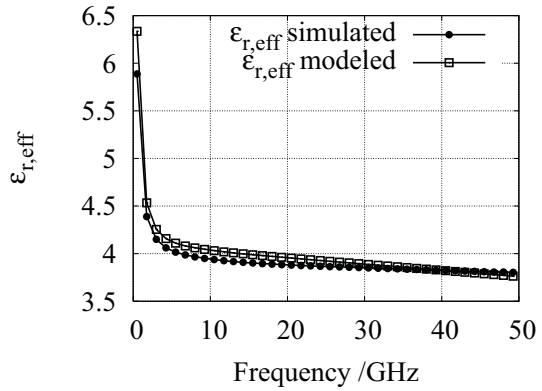

Fig. 4.16: Effective relative permittivity extracted from the S-parameters (simulation and model) of a 1000 μm long and 3 μm wide TFMSL

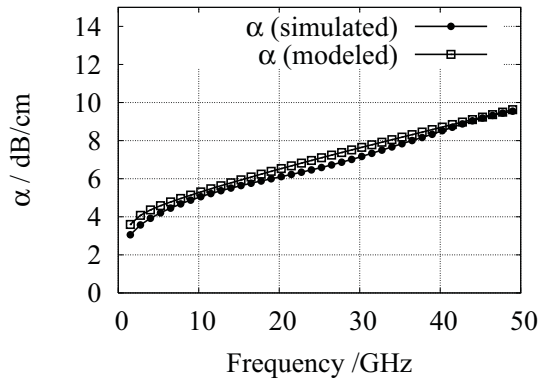

Fig. 4.17: Attenuation constant extracted from the S-parameters (simulation and model) of a 1000 μm long and 3 μm wide TFMSL

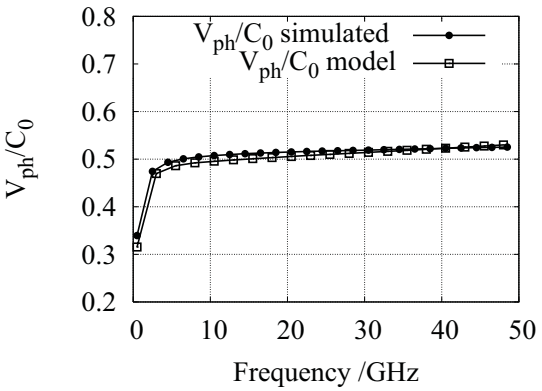

Fig. 4.18: V_{ph}/C_0 extracted from the S-parameters (simulation and model) of a 1000 μm long and 3 μm wide TFMSL

4.3 Lumped elements on lossy silicon substrate

Lumped elements on lossy silicon substrates have already been widely used and presented in e.g. [33], [34]. Designs using a lumped element approach achieve highly compact layouts, resulting in a low-cost IC. The most critical challenge of lumped inductive elements is to provide a scalable model. However, scalable models are only required when an extremely wide spectral region has to be covered. In this work, because of the low amount of required inductance values, it was possible to circumvent this problem. By layouting separate test structures of a small amount of spiral inductors as well as deembedding structures, it was possible to create a library of inductors based on measurements to drastically improve the simulation accuracy. A disadvantage of IC design based on a highly compact methodology is the challenge of the redesign. If larger elements are required during the redesign procedure, the available space on the layout might not be sufficient thus requiring a complete redesign of the IC and therefore significantly increasing the redesign time.

Chapter 5

Millimeter Wave Amplifier ICs

5.1 Introduction

The design of high performance mm-wave amplifiers operating beyond the $f_T/3$ limit is extremely challenging. Because of the low available gain when using the transistor in this region, appropriate topologies must be used, careful and accurate design simulations and optimizations have to be performed and precise layouting of the IC has to be accomplished. In this chapter, topologies capable of fulfilling such a task are described. In order to clearly demonstrate their capabilities and the possibility of design re-use, several versions were designed. In a first section, compact mm-wave amplifiers using lumped elements will be presented. Then, amplifiers using a thin-film microstrip line approach will be highlighted. For all these ICs, special emphasis has been placed on measures to substantially improve the isolation. The techniques which were necessary to reduce the cross-talk on the lossy silicon substrate are introduced in the following sections. Because all the presented ICs were designed to be implemented in a SHR or on the receiving side of a FMCW radar, they have a low noise approach in common. These topologies can easily be transposed to other amplifiers type such as e.g. preamplifier design.

5.2 Millimeter-wave amplifiers based on lumped elements

5.2.1 Millimeter-wave Low Noise Amplifier topology

In this section, the presented LNAs were realized using Atmel's SiGe2RF technology (see Section 3.1). To fully show the possibility of designing amplifiers beyond $f_T/3$ and to

demonstrate the design re-use approach, three versions were developed, operating above 30 GHz (at 35 GHz, 40 GHz and 50 GHz, respectively).
In order to obtain good gain/noise performance, two main topologies are used: the common-emitter and the cascode amplifier (an amplifier based on a single common-base stage is rarely used). However, since the operational frequency of the amplifier is approaching half of the transit frequency for the used technology, the first approach does not provide associated gain sufficient for acceptable performance. Therefore, the cascode topology is the most appropriate choice. In order to understand the essential advantages of the cascode amplifier, a simplified small-signal equivalent circuit of a bipolar transistor in common-emitter configuration is presented in Fig. 5.1.

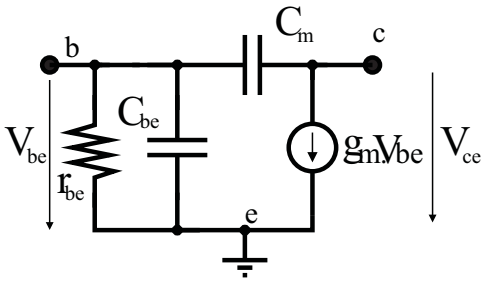

Fig. 5.1: Simplified small signal equivalent circuit of a transistor in common-emitter configuration

The capacitor C_m is called Miller capacitance. The input admittance of this circuit can be written:

$$Y_{in} = \frac{1}{r_{be}} + j\omega(C_{be} + C_m(1 - \frac{V_{ce}}{V_{be}})) \tag{5.1}$$

The equation 5.1 can then be written:

$$Y_{in} = \frac{1}{r_{be}} + j\omega(C_{be} + C_M) \tag{5.2}$$

where

$$C_M = C_m(1 - A_v) \tag{5.3}$$

This shows that the capacitor C_M will increase with higher magnitude of the voltage gain, therefore significantly decreasing the cut-off frequency of the amplifier. A simple solution consists in reducing the voltage gain of the transistor. Using a first order small signal model, it can be determined that:

$$A_v = -g_m R_L \tag{5.4}$$

where R_L is the load applied at the output of the common-emitter transistor. Hence, by using a low impedance load, the voltage gain can be strongly reduced. A common-base

transistor suffers less from the Miller effect and has a low input impedance (approximately $\frac{1}{g_m}$) and can therefore be cascaded to the common-emitter transistor. By using this technique and assuming that the two cascaded transistors have the same transconductance, the voltage gain becomes:

$$A_v = -g_m R_L = -g_m \frac{1}{g_m} = -1 \tag{5.5}$$

Hence, the influence of the Miller effect in a cascode amplifier configuration is strongly reduced, thus leading to a higher gain and bandwidth at high frequency. Another advantage of this topology is the provided higher isolation. The disadvantages of the cascode amplifier are the required higher supply voltage level as well as a slightly decreased noise performance. Because the provided gain of a single cascode stage is still not sufficient to reach acceptable performance (the targeted gain was in excess of 10 dB for all presented ICs), three stages are cascaded.

In order to obtain a wide input matching as well as higher linearity, a combination of emitter degeneration and series inductance at the input for simultaneous noise and 50 Ω matching is used. Above f_β (corner frequency of the current gain characteristic), the series inductive feedback (emitter degeneration) shows up as a real resistance at the input whereas the series inductance adjusts the imaginary part of the cascode input impedance by simultaneously moving the optimum source reflection coefficient Γs,opt. A simplified small signal equivalent circuit of the transistor with input matching network is presented in Fig. 5.2. Using this small signal circuit, the input impedance can be defined as follows:

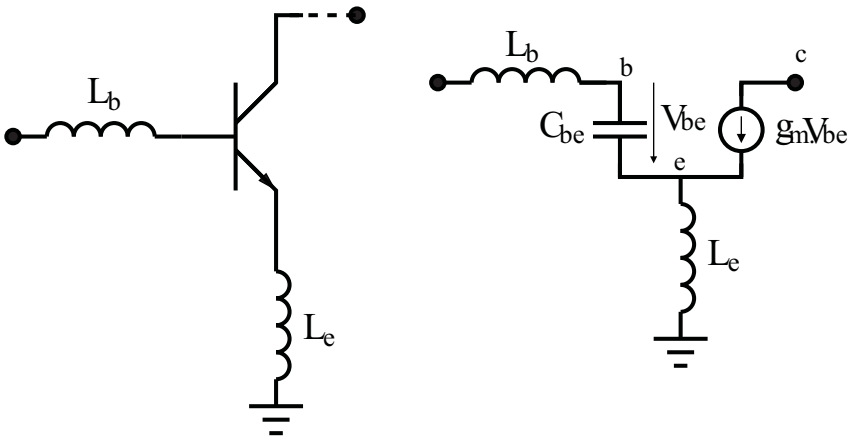

Fig. 5.2: Simplified small signal equivalent circuit of the transistor with input matching network

$$Z_{in} = \frac{g_m L_e}{C_{be}} + j(\omega(L_b + L_e) - \frac{1}{\omega C_{be}}) \tag{5.6}$$

Therefore using the previously stated relation, the value of L_e and L_b can be evaluated using the following equations:

$$L_e = \frac{50 C_{be}}{g_m} \tag{5.7}$$

$$L_b = \frac{1}{\omega^2 C_{be}} - L_e \tag{5.8}$$

The interstage as well as the output matching of the complete LNA were designed using LC matching networks. Such an approach allows DC biasing through the inductor as well as AC coupling between the stages by means of the capacitors. A schematic of the output matching network is presented in Fig. 5.3. Using this simple small signal circuit,

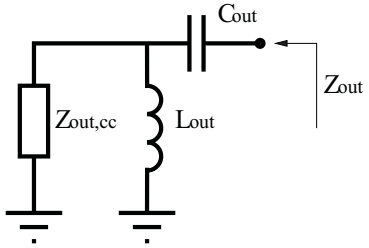

Fig. 5.3: Simplified small signal equivalent circuit of the cascode amplifier output impedance together with the output matching network. $Z_{out,cc}$ represents the output impedance of the cascode amplifier

the output impedance can be defined as:

$$Z_{out} = \frac{1}{j\omega C_{out}} + \frac{1}{\frac{1}{j\omega L_{out}} + \frac{1}{Z_{out,cc}}} \tag{5.9}$$

Even using this very simple small signal approach (the parasitics of the inductor and the capacitor are not included), a complex term would be obtained by separating the real and imaginary part of this equation. Therefore the smith chart was used to evaluate the necessary values of the matching elements. A schematic of a single-stage cascode LNA with inductive emitter-degeneration as well as series inductance is presented in Fig. 5.4 and a detailed chip photo of a single stage is depicted in Fig. 5.5.

5.2.2 Isolation techniques

The coupling or cross-talk is a critical issue on silicon substrate and has to be reduced using appropriate techniques [35].

Pad shielding The required large dimension of a signal pad makes it a very critical element when the improvement of the isolation is aimed for. In order to reduce the coupling

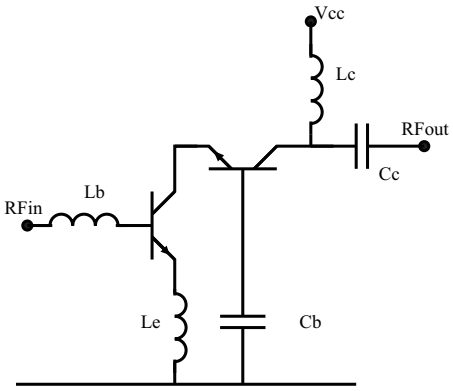

Fig. 5.4: Schematic of a single stage of the LNA based on lumped elements

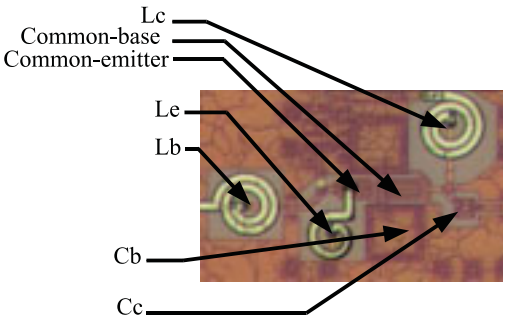

Fig. 5.5: Chip photo of a single stage of a designed LNA based on lumped elements using Atmel's SiGe2RF technology

from the core of the IC to its interface (bonding pads), the bottommost metalization layer is grounded and placed below the signal pad, therefore providing a shield from the lossy silicon substrate [36].

Inductor shielding As already reported, the amplifiers use a lumped elements topology, thus leading to a highly compact design. This high integration density however causes the inductors to be placed in close vicinity (see Fig. 5.6). Inductor to inductor coupling is then extremely predominant, difficult to model and critical because of the simulation inaccuracy they can engender. A simple approach to significantly reduce the inductor to inductor cross-talk is to shield the inductors using a grounded metal ring surrounding each element [37]. Due to these elements surrounding the inductor, a parasitic coupling of inductor-to-ground shield occurs and thus decreases the inductance as well as the quality factor of these reactive elements.

Substrate contacts In order to reduce cross-talk between the three stages of the designed LNAs, a ring of substrate contacts was placed around each stage of the IC. Therefore the substrate is grounded and neighboring stages are well isolated from each other [38].

Stage to stage filtering network In order to reduce significantly the amount of pads within the IC, the three stages of the millimeter-wave amplifiers are fed with a single supply voltage line. This solution decreases significantly the complexity of the characterization and leads to a simpler mounting structure. However, this single biasing line can also generate a path for cross-talk from one stage to another. To substantially reduce this parasitic effect, an RC low-pass filter [39] was placed at the biasing node of each stage of the IC (see Fig. 5.7). R_{filter} is an on-chip resistor of 10 Ω and C_{filter} is made of two nitride

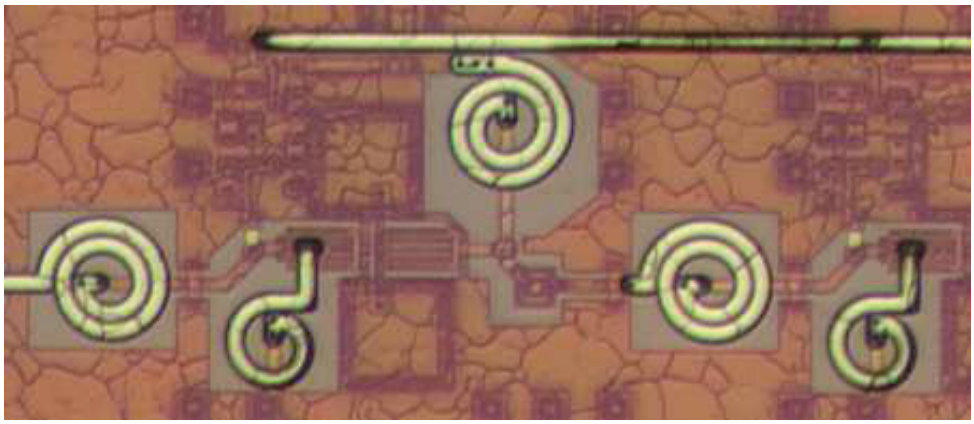

Fig. 5.6: Detail of a millimeter-wave amplifier using lumped elements. Five inductors are placed in a chip surface of 200 × 100 μm^2

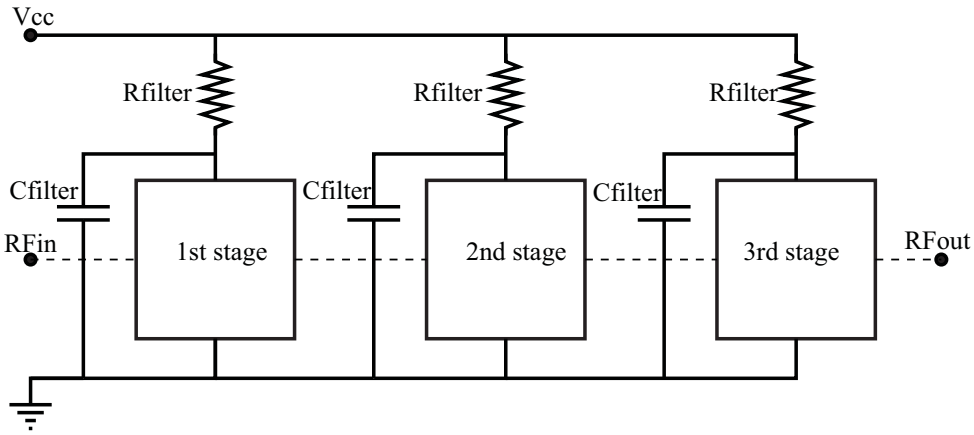

Fig. 5.7: Stage to stage RC low-pass filter

capacitors with an overall value of 3 pF. The choice of the value of R_{filter} is a compromise between efficiency of the low-pass filter and voltage drop across this element (a large value would result in a strong filtering but would also lead to a higher required supply voltage level). The choice of the value of C_{filter} is a compromise between efficiency of the filtering and integration density. The previously stated values were found to be perfectly sufficient for this study. Another possibility could have been to use an LC low-pass filter. However, because this filtering technique has to be applied at each stage and because of the necessary large dimension of the on-chip inductor, such topology would have led to a poor integration level.

5.2.3 Layout and characterization

The 35 GHz amplifier (first designed amplifier) was carefully laid out in order to reduce the length of the interconnects. Because of the lumped elements approach, the layout is extremely compact (only 823 × 380 μm^2). Once the layout was completed, all interconnects which were not initially included in the simulation environment were added to significantly improve the simulation accuracy. Due to the very short dimensions of these lines, a simple approximation (1 pH parasitic inductance assumed per 1 μm of on-chip interconnect) was used in order to speed-up the design. A detailed picture of the 35 GHz amplifier is depicted in Fig. 5.8. Once the 35 GHz LNA is characterized and measurements

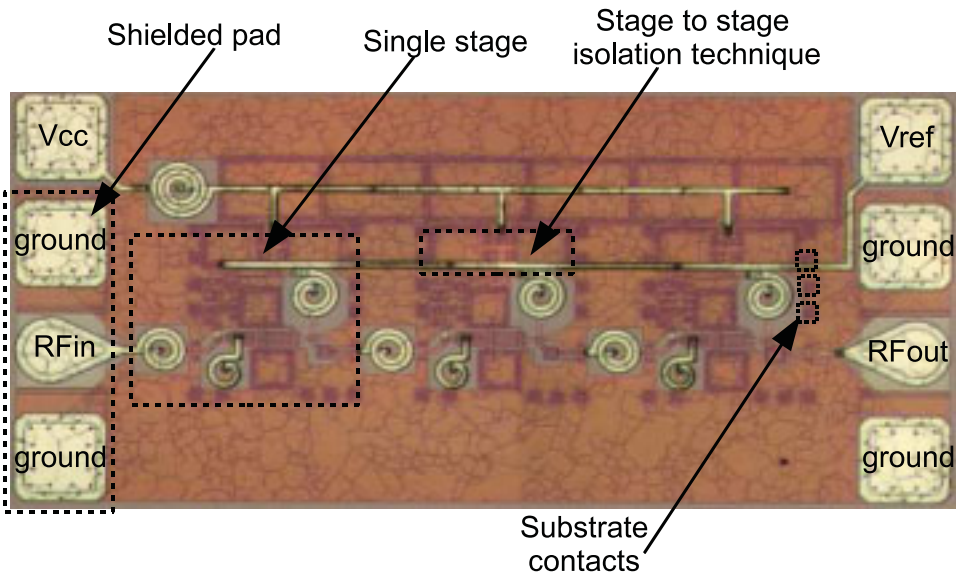

Fig. 5.8: Picture of the 35 GHz LNA using Atmel's SiGe2RF technology (823 × 380 μm^2)

are found to agree with the simulation, a re-use of the simulation environment and of the layout is possible to achieve similar performance at different frequency bands. Therefore the required time to design future ICs is tremendously reduced and chances to achieve the targeted performance in one design cycle (without redesign) are greatly improved. This leads to a drastically reduced overall cost.

Re-use of the topology

To prove this concept, the 40 GHz and 50 GHz amplifiers were designed using the layout configuration of the 35 GHz LNA (the lumped elements have simply smaller values

and dimensions in order to increase the operational frequency). Bias conditions, transistor sizes and elementary cells of the layout were kept unchanged. The pictures of the designed LNAs are depicted in Appendix A. The measurements of these ICs were performed on-chip in a 50 Ω test environment, using a Vector Network Analyzer (VNA) after Short Open Load Thru calibration (SOLT). A picture describing the setup is presented in Fig. 5.9. The small signal measurements of the three amplifiers are shown in Fig. 5.10,

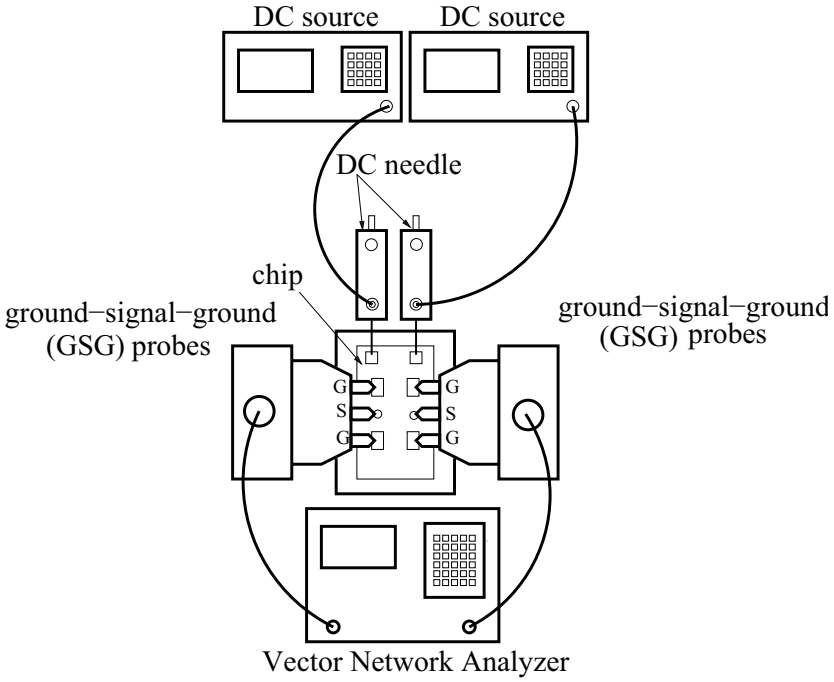

Fig. 5.9: Setup used to characterize the small signal operation of the LNA (after SOLT calibration)

5.11 and 5.12, respectively. The ICs consume 135 mW at a supply voltage level of 3 V, which is a reasonable power consumption for three stage cascode LNAs operating at these frequencies. The noise figure measurement of these circuits could not be performed because of the frequency limitation of the available test set (2-26 GHz). The simulated noise performance is therefore presented instead. As can be seen, by using the previously described isolation techniques, the reverse isolation of the ICs is very good (always higher than 50 dB over the complete measured spectrum). The large signal measurements were performed on-chip using the signal source Agilent E8254A and a power meter. The setup was taken perfectly symmetrical in order to easily separate the losses at the input of the DUTs from the losses at their output. A schematic describing the used setup to accurately calculate the losses is presented in Fig. 5.13. The setup used to perform the large signal measurement of the LNAs is presented in Fig. 5.14. The performance of the 35 GHz and 40 GHz LNAs under large signal conditions are presented in Fig. 5.15 and

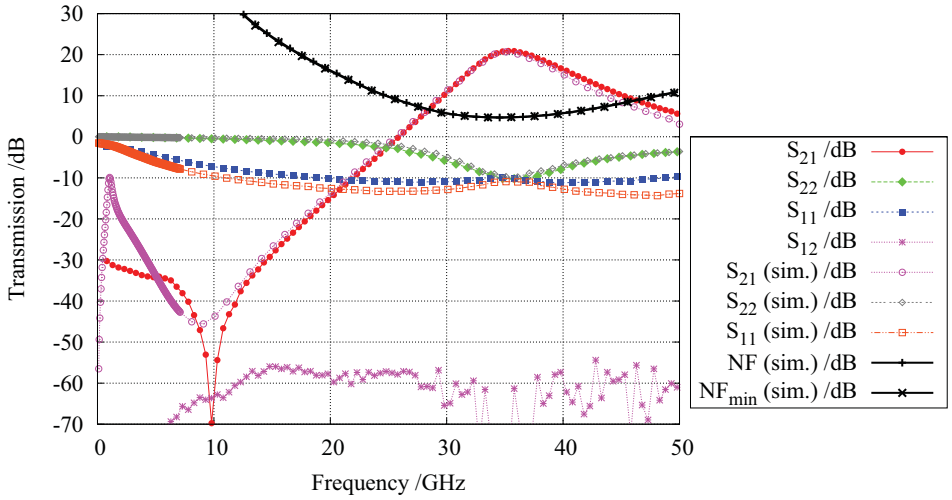

Fig. 5.10: Simulation and on-wafer small signal measurements of the **35 GHz** amplifier under 50 Ω test environment with a supply voltage level of 3 V (drawn current is 45 mA)

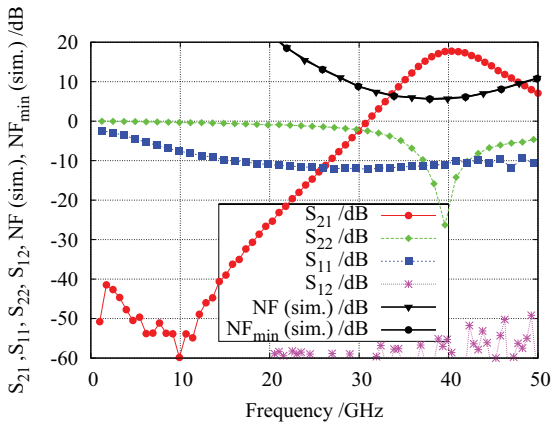

Fig. 5.11: On-wafer small signal measurements of the **40 GHz** amplifier under 50 Ω test environment with a supply voltage level of 3 V (drawn current is 45 mA)

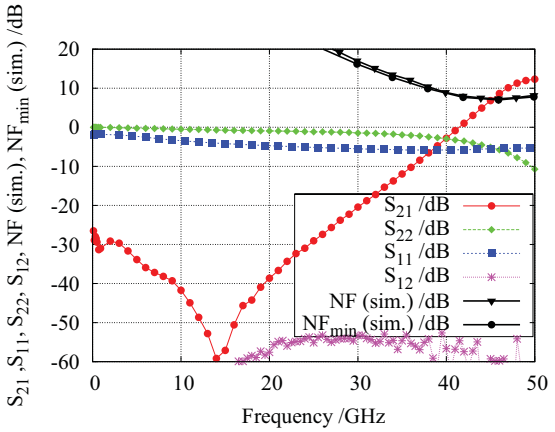

Fig. 5.12: On-wafer small signal measurements of the **50 GHz** amplifier under 50 Ω test environment with a supply voltage level of 3 V (drawn current is 45 mA)

5.16. The linearity of the 50 GHz could not be measured. As can be seen, the 1 dB input compression points of the designed LNAs are good (higher than - 15 dBm for both measured LNAs) mostly because of the chosen bias point for each stage of the LNAs and the use of emitter degeneration. Because the system architecture presented in Section 2.2 is differential, two single-ended LNAs can be juxtaposed. This technique was used e.g. in [40]. However, this technique is not optimal because the problem of the packaging is still not solved in contrary to a fully balanced approach. Therefore, the following sections describe fully differential topologies to drastically reduce the influence of the packaging.

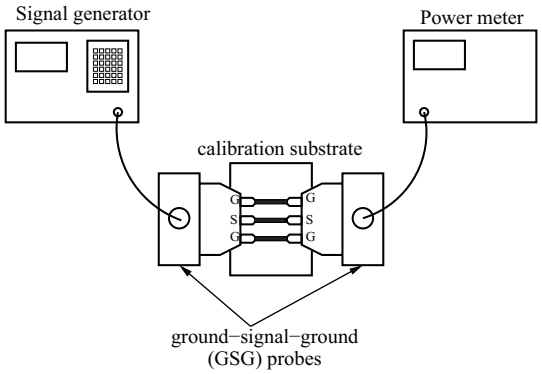

Fig. 5.13: Schematic describing the used setup to accurately calculate the losses

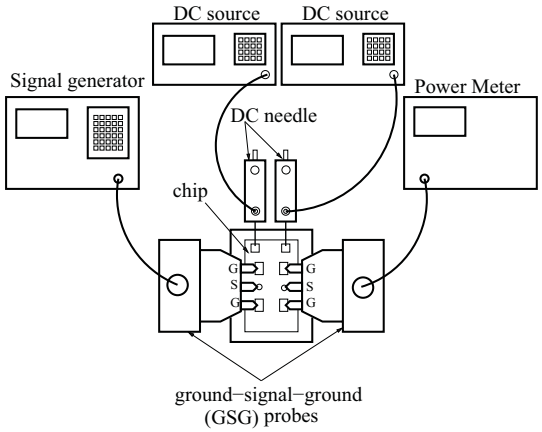

Fig. 5.14: Setup used to perform the large signal measurement of the LNAs

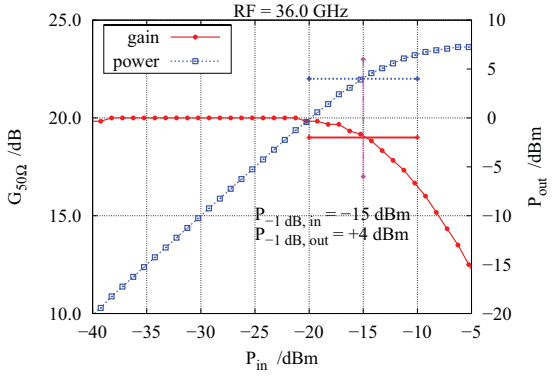

Fig. 5.15: On-wafer large signal measurements of the **35 GHz** amplifier in a 50 Ω test environment with a supply voltage level of 3 V (drawn current is 45 mA)

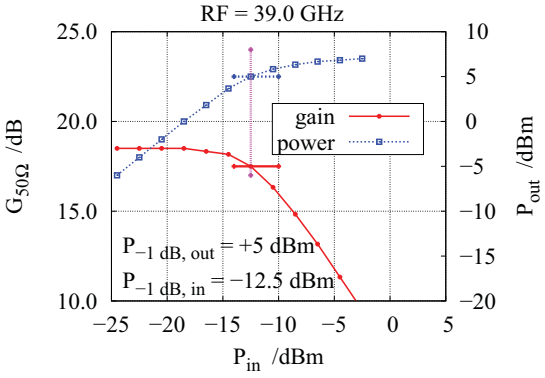

Fig. 5.16: On-wafer large signal measurements of the **40 GHz** amplifier in a 50 Ω test environment with a supply voltage level of 3 V (drawn current is 45 mA)

5.3 Millimeter-wave amplifiers using TFMSLs

5.3.1 Millimeter-wave amplifiers based on thin-film microstrip lines using Atmel's SiGe HBT Technology

Amplifiers based on lumped elements lead to a highly compact design and therefore to a higher monolithic integration of the complete system. However, it is difficult to achieve an acceptable accuracy of the spiral inductors behavior using EM simulations. Furthermore, if a redesign needs to be performed, due to the high integration density, the replacement of an inductor by another might lead to the complete redesign of the IC. Another issue of the previously described topology is its single-ended architecture which leads to critical

packaging. Therefore, the use of thin-film microstrip lines in a fully integrated fully differential amplifier was investigated.

Description of the topology

As previously explained (see Section 5.2.1), the chosen technology does not have a sufficient f_T to use single-stage and common-emitter topology. Therefore, to achieve competitive amplification level, three stages using a cascode topology were used. As a current source at the emitters of the common-emitter transistor pair, a typical technique is to use a current mirror [41] or a resistor [42, 43]. However, this leads to a significant voltage drop and therefore necessitates a higher supply voltage. It is possible to overcome this problem by using a reactive element. This was done in this work by using a high value inductor as e.g. in [44].
In order to obtain a good input matching, an emitter degeneration was used (already highlighted in Section 5.2.1). The output matching uses an LC combination. A schematic of a single stage of the fully differential LNA is depicted in Fig. 5.17. Differential designs

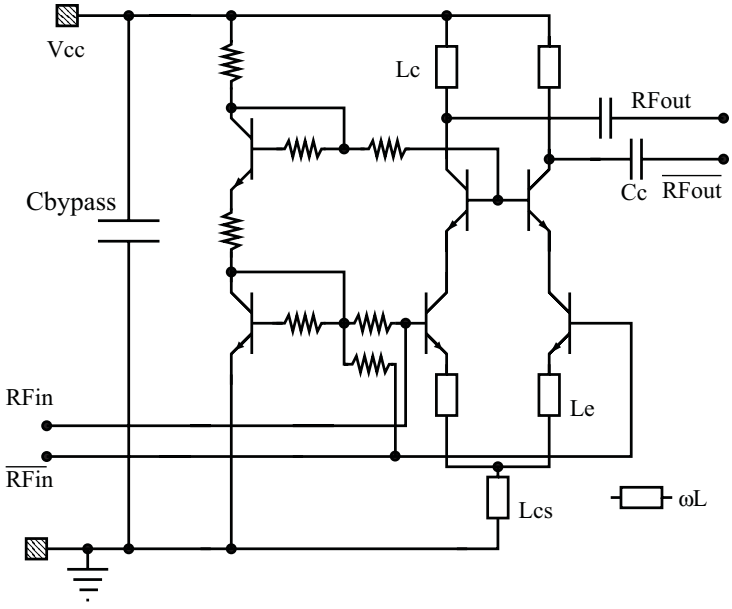

Fig. 5.17: Schematic of a single stage of the differential LNA

suffer from a higher power dissipation. Because the linearity was not a strong criterion for this design, a smaller transistor was used in order to significantly reduce the drawn current of the circuit. Thereby, reasonable power consumption could be reached. The thin-film microstrip elements were simulated using two EM field simulation tools (Momentum and Sonnet).

Layout and measurements of the fully differential low noise amplifier using Atmel's SiGe HBT technology

Like for the single-ended LNA presented previously, the layout of the differential amplifier was carefully performed in order to reduce the length of the interconnects. This leads to an IC with very compact dimensions (680 × 840 μm^2). The size of this IC is therefore only slightly larger than the two juxtaposed single-ended LNAs, which proves that highly compact ICs can also be reached by using a transmission line approach. Because of the unavailability of baluns beyond 26 GHz, the differential amplifier was measured single-endedly. A typical technique to characterize such IC is to provide 50 Ω terminations at the input and output of half of the circuit. In this work, to further ease the measurement procedure, an on-chip resistor with a value of 50 Ω was placed behind the input and output signal pads of the lower half of the LNA. Thereby, only 100 μm GSG probes were necessary to characterize the IC. Therefore the setup used to perform the small signal and large signal measurements of this amplifier remain the same as for the previously presented single-ended LNAs. After on-chip characterization, the resistor can be easily removed to allow the mounting of the chip. For the same reason, the three stages of the LNA are fed through a single bias line. Hence, only a single DC needle is necessary for on-chip characterization and a single bondwire is necessary to connect the on-chip supply voltage line to the test fixture. A chip photo of the differential LNA based on TFMSL using Atmel's SiGe2RF technology is presented in Fig. 5.18. The small signal and large signal

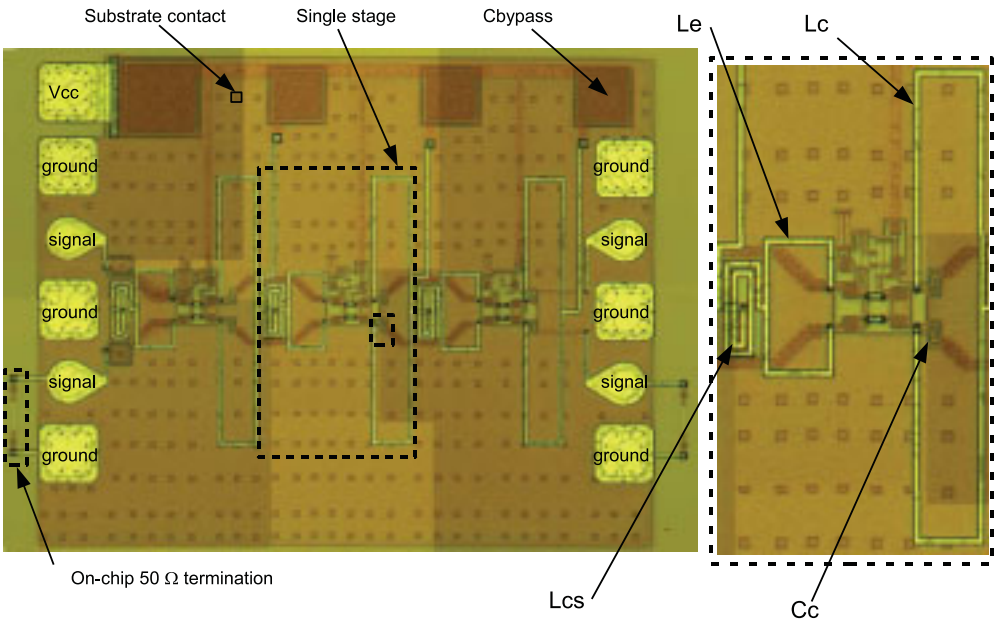

Fig. 5.18: Chip photo of the differential LNA using TFMSL (700 × 850 μm^2)

measurements of the IC are presented in Fig. 5.19 and 5.20. These measurements were performed at a supply voltage level of 4 V (corresponding to a drawn current of 40.9 mA). In order to obtain the differential gain of the IC, 6 dB should be added to the gain of the amplifier measured single-endedly (this procedure was also explained e.g. in [45]). The determination of the 1 dB input and output compression point of the differential amplifier based on single-ended measurements is more difficult. However, according to simulations, removal of 3 dB to $P_{1\ dB,in}$ and addition of 3 dB to $P_{1\ dB,out}$ brings a very reasonable approximation and was therefore used here.

Like the 35, 40 and 50 GHz LNAs previously described, this fully differential amplifier was designed in order to allow an easy re-use. The TFMSLs are placed within the layout in a way that allows an easy shortening of their lengths to reach higher frequencies. The potential of such an approach is described in the following section.

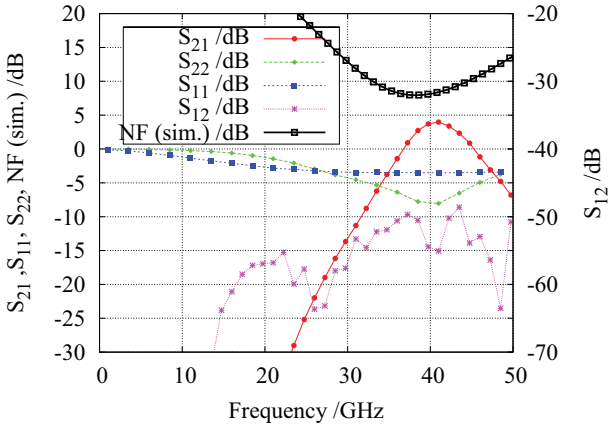

Fig. 5.19: On-wafer small signal measurements of the 40 GHz amplifier in a 50 Ω test environment with a supply voltage level of 4 V and drawn current of 41 mA (6 dB should be added to the gain of the amplifier driven single-endedly in order to obtain the differential gain)

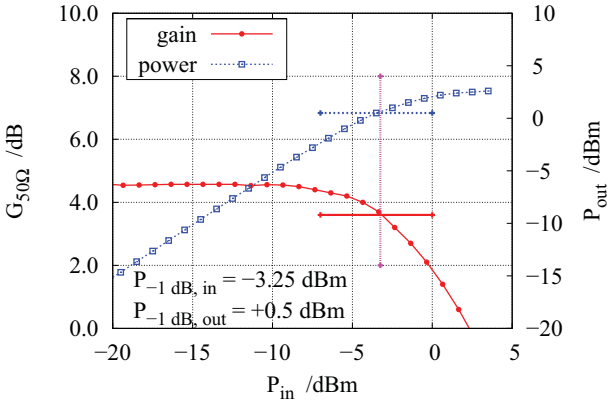

Fig. 5.20: On-wafer large signal measurements of the 40 GHz amplifier in a 50 Ω test environment with a supply voltage level of 4 V (drawn current is 41 mA). 3 dB should be removed from the $P_{1dB,in}$ and 3 dB should be added to the $P_{1dB,out}$ of the amplifier driven single-endedly in order to obtain the compression points of the amplifier driven differentially

5.3.2 77-81 GHz low noise amplifier based on thin-film microstrip lines using IHP's SiGe BiCMOS Technology

Just as the LNAs hitherto reported, the 77-81 GHz low noise amplifier uses three AC coupled cascaded differential cascode stages. The previously described noise matching techniques (emitter degeneration) were not used for this IC. It was simulated that the gain performance of the LNA using emitter degeneration was too low because of the generated feedback. Hence, the input of the whole IC was simply matched for optimum noise performance using a simple shunted TFMSL, similarly [46]. The simulated input reflexion coefficient was below 10 dB over the whole SRR bandwidth. The schematic of a single stage is presented in Fig. 5.21. Because of the narrow frequency band of operation, the current source at the emitter of the common-emitter transistor pair uses a resonant circuit by means of an LC network [47]. This topology provides a very good common-mode suppression and allows a low supply voltage level as explained in section 5.3.1. One critical disadvantage of this approach is that above resonance, the LC network is seen as a capacitance by the common-mode signal. This capacitive series feedback leads to a negative real part of the impedance seen into the bases of the differential amplifier which can generate spurious common-mode oscillation (the circuit has then a configuration of capacitively degenerated oscillator). Therefore, the stability of the LNA under common-mode excitation required to be carefully verified. In order to decrease the noise figure of the LNA, all transistors of the IC are biased at a low current density. This also leads to a very low power consumption (only 90 mW at a supply voltage of 3 V). A chip photo of

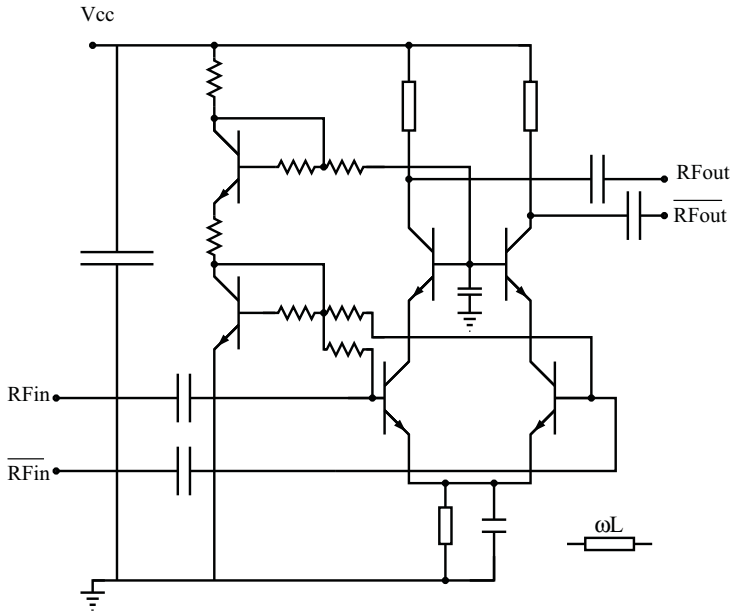

Fig. 5.21: Simplified schematic of a single stage of the 77-81GHz LNA

the IC is presented in Fig. 5.22.

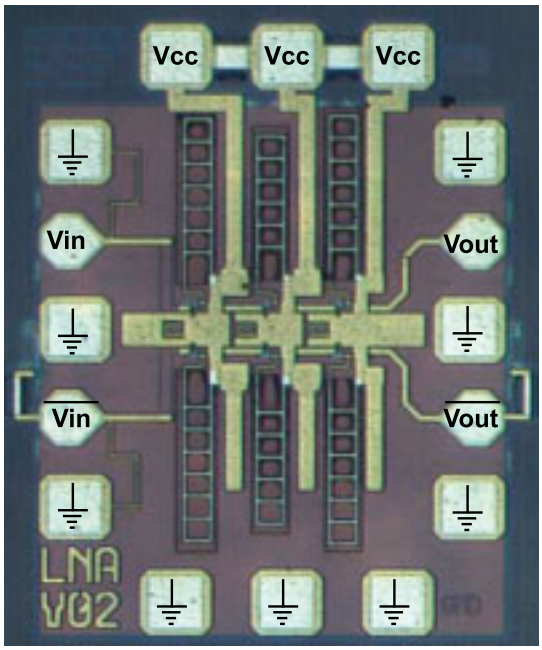

Fig. 5.22: Chip photo of the 77-81 GHz LNA (530 × 690 μm^2)

Measurements of the 77-81 GHz low noise amplifier

Like for the fully differential amplifier previously presented in Section 5.3.1, the IC was characterized on-chip and single-endedly. On-chip 50 Ω resistors were placed behind the input and output signal pads of the lower half of the LNA. Contrary to the previously presented LNA, this technique was mandatory due to the lack of 100 μm GSGSG probes operating at these frequencies.
The small signal performance was measured in a first step (same setup than for the previously described amplifiers). The S-parameters are depicted in Fig. 5.23. The large signal measurements were performed single-endedly as well, the performance of the LNA is presented in Fig. 5.24. The characterization of the losses was much more challenging due to the non-symmetrical setup. The losses of each element of the setup were characterized individually. However, the accuracy of the measurements remains acceptable. As can be seen, the LNA shows very good gain performance (like in the previous section, 6 dB should be added to obtain the gain of the LNA if driven differential), as well as good linearity. Using the previously mentioned isolation techniques (filtering network, substrate contact

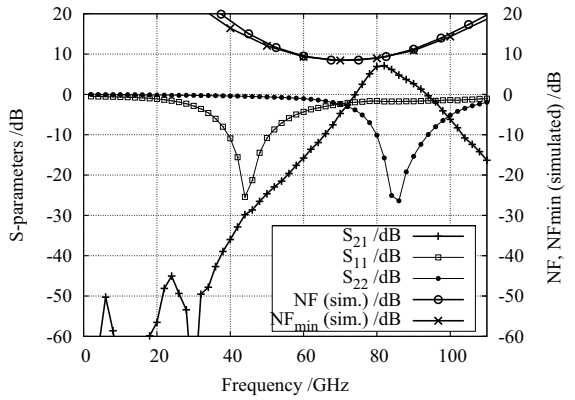

Fig. 5.23: S-parameter measurements of the differential 77-81 GHz LNA driven single-endedly supplied with 3 V (with a corresponding drawn current of 30 mA). (6 dB should be added to the gain of the amplifier driven single-endedly in order to obtain the differential gain)

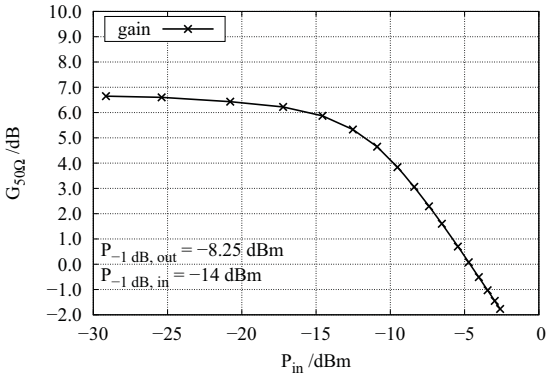

Fig. 5.24: Large signal measurements of the differential 77-81 GHz LNA driven single-endedly supplied with 3 V (with a corresponding drawn current of 30 mA). 3 dB should be removed from $P_{1dB,in}$ and 3 dB should be added to $P_{1dB,out}$ of the amplifier driven single-endedly in order to obtain the compression points of the amplifier driven differentially

at the frame of each stage, pad shielding, cascode topology) the reverse isolation is very good for an IC operating at this frequency range and fabricated on a low-resistivity Si substrate. The only problem appearing during measurements is the input matching which was shifted to a lower frequency range. This was explained by the wrong modeling of the bond pads. The capacitance of the pad (most critical parasitic) was calculated using a simple parallel plate capacitance equation. A slight inaccuracy of the TFMSL model was also partly responsible for this deviation. It should be noted that the same problems occurred at the output, however because the length of the TFMSL used within the output matching network of the third stage is adjustable, this problem could be solved. The matching could be improved by reducing the pad dimensions or by implementing an integrated antenna on the chip. This 77-81 GHz LNA is the first published differential LNA operating at this frequency range in any existing technology [48].

Re-use of the topology

In order to demonstrate reliable operation in a wide frequency range and to avoid re-designs if the amplifier will be used for different applications (different frequency ranges), the effective lengths of the lines are adjustable within a wide range. This can easily be

realized by cutting shorting bars in the top metallization layer between the two complementary signal lines of a differential microstrip line. Adjustable line technique has already been used in several publications such as e.g. in [49]. However, as depicted in Fig. 5.25, as opposed to previous publications, the shorting bars were not placed in the virtual ground of the differential microstrip line. This solution allows to save a large chip area and to decrease the interstage interconnects. However, a higher number of cuts is necessary. Several techniques can be used to cut the shorting bars placed within the IC (ultrasonic manipulator, focused ion beam, laser or needle). In this work, although a simple needle was successfully used to perform several cuts, the focused ion beam technique was often chosen due to its higher accuracy. It should be noted that if mass-market applications are targeted, a redesign of the mask corresponding to the upper metalization level might be useful. However, because a modification is necessary only on a single mask, the overall redesign cost is considerably reduced. Using a single IC and various line length

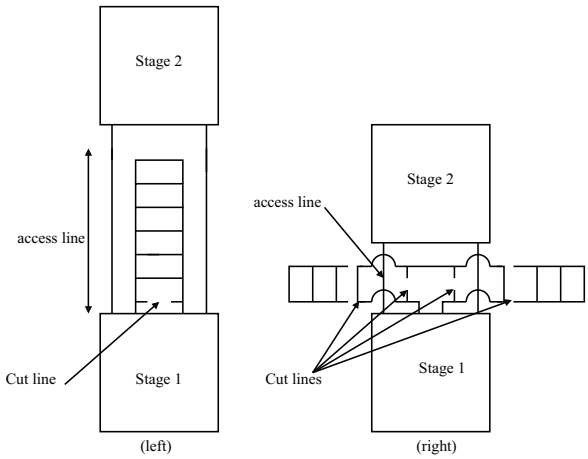

Fig. 5.25: Necessary cuts in [49] (left) and with the used topology (right). As can be seen, the used topology decreased significantly the length of the interconnect

configurations, several frequency ranges were reached with very good performance. The small signal and large signal measurements of the three differential LNAs measured single-endedly are depicted in Fig. 5.26 and Fig. 5.27, respectively. As can be seen, the measured amplifiers show high gain and good linearity with low power consumption, therefore proving the suitability of this topology not only for the UWB 77-81 GHz automotive radar applications but also for a wide range of consumer electronics operating beyond 60 GHz.

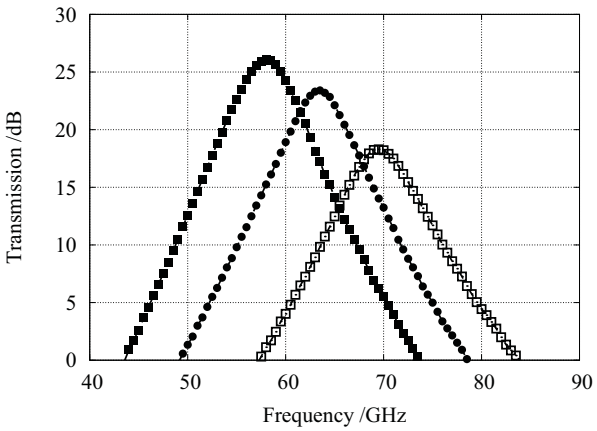

Fig. 5.26: On-wafer small signal measurements of the millimeter-wave LNAs at 3 V supply voltage (the corresponding drawn current is 30 mA)

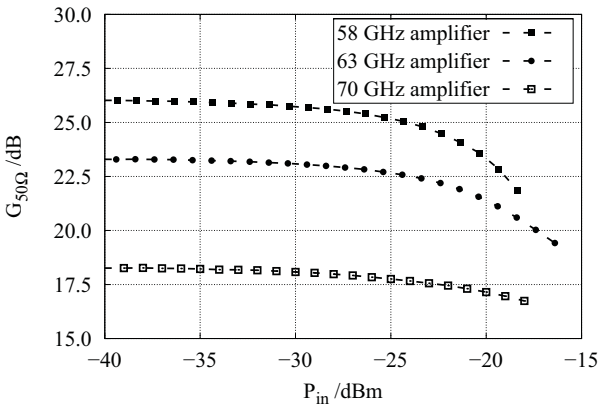

Fig. 5.27: On-wafer large signal measurements of the millimeter-wave LNAs at 3 V supply voltage (the corresponding drawn current is 30 mA)

5.4 Summary of the millimeter-wave amplifiers performance

In this chapter, several amplifier topologies were presented. These topologies allow the ICs to reach very good performance beyond $f_T/3$ and allow an easy design re-use, both leading to a substantial cost reduction. The described ICs use several techniques that once combined together, allow to achieve very good results, such as e.g. high gain, compact IC, good matching. In order to reach competitive gain (in excess of 10 dB), three cascaded stages were necessary. Each stage is based on a cascode topology with reactive input and output matching network. In order to achieve good noise and gain performance, a simultaneous noise and 50 Ω matching was performed using an emitter degeneration technique (the narrow band LNAs using IHP technology do not use this approach due to the fact that a narrow band noise and 50 Ω matching could be obtained without this topology). In order to improve the isolation, several techniques such as pad shielding, efficient DC filtering network and inductor shielding were implemented. The use of lumped elements or folded TFMSLs leads to a compact die area. These ICs were designed in such a way that layout modifications on the reactive elements can easily be performed. This allows to shift the center frequency over a very wide range. Several versions using a common layout structure were designed in order to prove this aspect. In the following tables, the main results of the designed amplifiers are presented. The values and parameters of several of the designed mm-wave amplifiers are shown in Appendix B.

parameter				
S.E./Diff.	S.E.	S.E.	S.E.	Diff.
L.E./TFMSL	L.E.	L.E.	L.E.	TFMSL
P_{DC} /mW	135	135	135	164
f_{op} /GHz	35	40	50	40
S_{21} /dB	21	18	13	4.75*
NF /dB	4.7 (sim.)	5.7 (sim.)	8.2 (sim.)	8 (sim.)
S_{11},S_{22} /dB	-10, -10	-10, -20	-10, -15	-6, -8
$P_{1dB,in}$ /dBm	-15	-12.5	n.a.	-3.25*
Chip area /μm^2	823 × 380	735 × 380	680 × 380	700 × 850
comments				measured S.E.

Tab. 5.1: Detailed amplifier performance overview using the Atmel 0.8 μm SiGe HBT process. S.E.: Single-ended, Diff.: Differential, L.E.: Lumped elements, sim.: simulated, *:Measured single-endedly

parameter				
S.E./Diff.	Diff.	Diff.	Diff.	Diff.
L.E./TFMSL	TFMSL	TFMSL	TFMSL	TFMSL
P_{DC} /mW	90	90	90	90
f_{op} /GHz	58	63	70	79
S_{21} /dB*	26	23	18	14
NF /dB	not sim.	not sim.	not sim.	8 (sim.)
S_{11},S_{22} /dB	-5, -18	-5, -15	-5, -11	-3, -10
$P_{1dB,in}$ /dBm*	-25	-22.5	-20	-14
Chip area /μm^2	530 × 690	530 × 690	530 × 690	530 × 690

Tab. 5.2: Detailed amplifier performance overview using the IHP 0.25 μm SiGe BiCMOS process. S.E.: Single-ended, Diff.: Differential, L.E.: Lumped elements, sim.: simulated, *:Measured single-endedly

5.5 Comparison with previously published amplifiers

The following table gives an overview of previously published amplifiers on Si substrate. As it can be seen, the amplifiers presented in this work exhibit similar or better performance, even if they are using a technology with lower f_T.

	P_{DC} /mW	f_{op} /GHz f_{op}/f_T	S_{21} /dB	NF /dB	$P_{1dB,in}$ /dBm	Technology
this work	135	35, 0.44	21	4.7	-15	0.8 μm SiGe HBT (f_T=80 GHz)
this work	135	40, 0.5	18	5.7	-12.5	0.8 μm SiGe HBT (f_T=80 GHz)
this work	135	50, 0.63	13	8.2	n.a.	0.8 μm SiGe HBT (f_T=80 GHz)
this work	164	40, 0.5 (diff.)	4.75	8	-3.25	0.8 μm SiGe HBT (f_T=80 GHz)
this work	90	58, 0.3 (diff.)	26	n.a.	-25	0.25 μm SiGe HBT (f_T=190 GHz)
this work	90	63, 0.33 (diff.)	23	n.a.	-22.5	0.25 μm SiGe HBT (f_T=190 GHz)
this work	90	70, 0.37 (diff.)	18	n.a.	-20	0.25 μm SiGe HBT (f_T=190 GHz)
this work	90	79, 0.42 (diff.)	14	8	-14	0.25 μm SiGe HBT (f_T=190 GHz)
[50]	18	44, 0.25	13.3	4.5	-17.5	0.12 μm SiGe HBT (f_T=208 GHz)
[51]	51	30, 0.25	16.8	6	-19.8	0.2 μm SiGe HBT (f_T=120 GHz)
[52]	20	40, 0.2	23	3.7	-12	0.13 μm SiGe:C BiCMOS (f_T=205 GHz)
[53]	11	61.5, 0.31	15	4.2	-20	0.12 μm SiGe HBT (f_T=200 GHz)
[54]	54	60, 0.44	11	n.a.	n.a.	130 nm CMOS (f_T=135 GHz)
[55]	41	40, 0.27	9.5	4	-7	90 nm CMOS (f_T=149 GHz)

Tab. 5.3: Comparison between the designed amplifiers and previously published millimeter-wave amplifiers

Chapter 6

Millimeter Wave Voltage Controlled Oscillators

6.1 Introduction

The function of an oscillator is to create a stable periodic time-varying output waveform. In the most general case, output signals can be e.g. sinusoidal, square, triangle or pulse. In this work, only sinusoidal waveforms are of interest and will be investigated.
Oscillators are essential blocks of an RF front-end and are used in applications such as carrier generation and clock signal. In order to allow the IC to achieve good performance, several aspects of the oscillator (voltage controlled oscillator in this work) have to be taken into account. This section highlights the theory of the oscillator and describes the chosen topologies. To fully demonstrate the potential of the chosen approaches, several versions were designed, measured and are presented here.

6.2 Theory of oscillators

6.2.1 Negative resistance type oscillators

There is a wide variety of oscillator topologies (RC oscillator, LC oscillator, ring oscillator, etc.). For this study, an oscillator of the negative-resistance type represents a good choice because of its capability to achieve high operation frequency, good output power and low phase noise.
Such circuits contain three main parts: a resonator, an active circuit and an output load, as described in Fig. 6.1. The oscillation condition is fulfilled if:

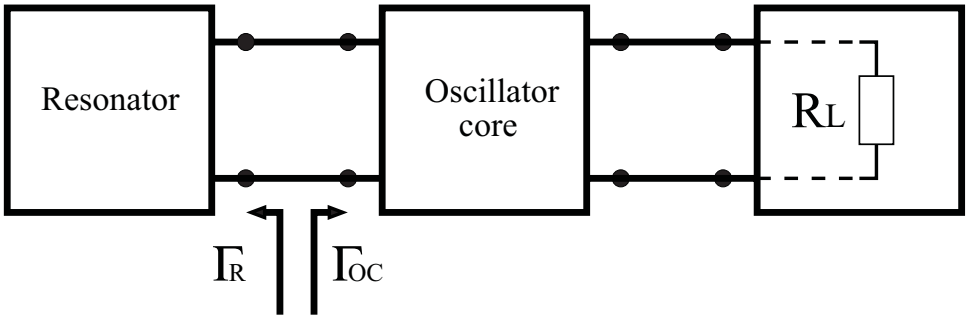

Fig. 6.1: Basic block-diagram of the negative resistance type oscillator

$$\Gamma_R.\Gamma_{OC} > 1 \tag{6.1}$$

This relation can also be divided into magnitude and phase requirements:

$$|\Gamma_R|.|\Gamma_{OC}| > 1 \tag{6.2}$$

$$\theta(\Gamma_R) = -\theta(\Gamma_{OC}) \tag{6.3}$$

In other words, at the interface between resonator and oscillator core, the product of magnitude of the resonator reflection coefficient and the oscillator core reflection coefficient must be higher than one and the phases must add up to zero.

6.2.2 Oscillator phase noise

Once the previously stated relations are fulfilled, several other aspects of the design have to be carefully studied. One of the most important figure of merit for an oscillator is its noise performance. In general, circuit elements (such as e.g. the resonator network) and device noise can perturb both the amplitude and phase of an oscillator output. However, all practical oscillators operate in saturation, therefore noise generated amplitude variations are compressed and that drastically decreases their influence on the circuit's noise performance. Therefore, the phase noise generally dominates. Such a study was performed in [56]. Another reason for the unimportance of the amplitude noise is that the VCO will be connected to the switching quad of the mixer (see chapter 7), where the transistors are operated in the switching regime. Thus, the focus of this work will be placed on strongly decreasing the phase noise of the IC.
Phase noise in LC oscillators (this work) is usually expressed by Leeson's relation:

$$\pounds(\Delta f) = \frac{FkT}{2P_{osc}} \left[1 + \left(\frac{f_{osc}}{2Q_L\Delta f}\right)^2\right] \left(1 + \frac{f_c}{|\Delta f|}\right) \tag{6.4}$$

Where f_{osc} is the oscillation frequency, Δf is the offset frequency, P_{osc} is the power of the carrier, Q_L is the loaded Q of the resonator, f_c is the corner frequency of the 1/f noise and F is a noise factor.
The major problem of this semi-empirical relation is that F is not specified for the given topology. Therefore the Leeson's relation was used here only for first approach and the phase noise optimization was performed through adequate simulations.
The phase noise of a VCO is depending on the quality factor of the resonator but also on the utilized devices. In bipolar devices, the phase noise strongly increases with increased collector current [57] and worsens with increased source impedance as well. Therefore, in order to obtain high output power as well as low phase noise, large devices biased at low current density were used. However, because the transistors are no more biased at the optimum current density $J_{c,opt}$, the f_T of the device decreases and this has critical repercussions on the loop gain of the oscillator. Hence, a compromise has to be found between necessary loop gain and phase noise performance and precise simulations using accurate models need to be performed.

6.3 Description of the topology

One of the first versions of the studied VCO type was presented in [58]. To obtain the oscillation condition, the transistor emitter is capacitively degenerated. A simplified schematic of the topology as well as a simplified small signal equivalent circuit (used for a similar calculation in [58]) is shown in Fig. 6.2. Using the presented equivalent circuit,

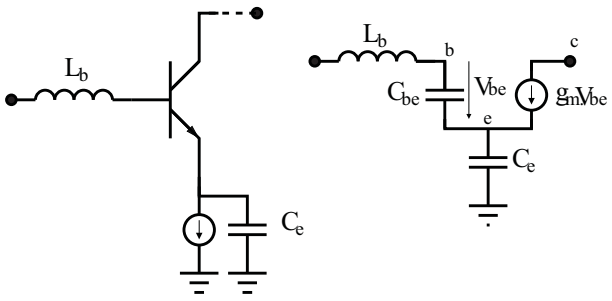

Fig. 6.2: Simplified schematic of the studied topology

the available negative resistance and the VCO oscillation frequency can be written:

$$Negative\ Resistance = -\frac{g_m}{\omega^2 C_{be} C_e} \tag{6.5}$$

$$\omega L_b - \frac{1}{\omega C_{be}} - \frac{1}{\omega C_e} \approx 0 \tag{6.6}$$

Li *et al.* in [59] proposed a topology based on the previously described design. The schematic of the oscillator is presented in Fig. 6.3. As can be seen, a differential topology

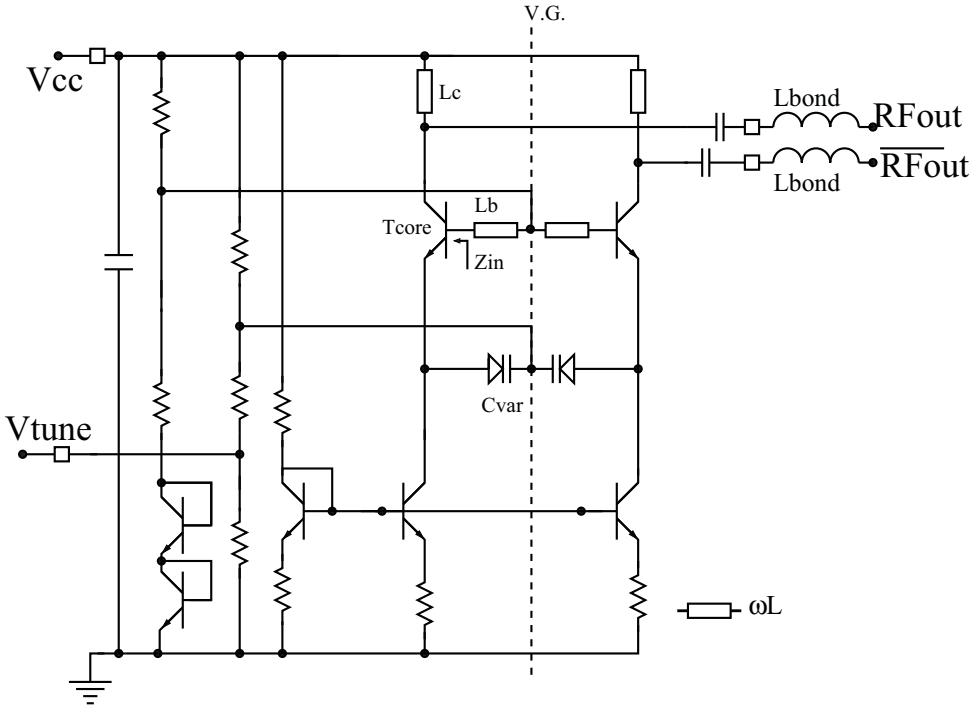

Fig. 6.3: Basic topology of the designed oscillator presented in [59]

was used. As previously explained, the impedance Z_{in} between the transistor T_{core} and the component L_b has a negative real part and a capacitive component that depends on the capacitor C_{var} provided by a varactor diode formed by either a reverse-biased emitter-base or collector-base region. The inductive elements such as L_b are made by short TFMSLs. Short transmission lines ($l \leq \lambda/4$) with short-circuit at one end have an effective inductance calculated as follows:

$$L_{eff} = \frac{Zo}{2\pi f} \tan(2\pi \frac{l}{\lambda}) \tag{6.7}$$

where l is the length, λ the wavelength on-chip, Zo the characteristic impedance and f the frequency. For $l << \frac{\lambda}{2\pi}$, L_{eff} is independent of frequency and proportional to l. A high value of Zo will lead to a shorter microstrip line, therefore the achieved integration level of the IC is very good even by using TFMSLs. The microstrip line L_c is used for matching. The output impedance is formed by the $50\,\Omega$ load (for half of the symmetrical circuit), the capacitance of the bond pad and the bond wire connecting the IC to the mounting structure. In opposition to the topology presented in [60] where the topology forces the signals across the transistors to be equal in magnitude but with opposite signs, here the common-mode oscillation is avoided using a current source. Therefore, a topology providing a high impedance over a wide bandwidth needs to be used. Hence, an LC

resonator (as presented in Section 5.3.2) or another type of narrow-band current source could not be used and a current mirror was preferred.
This topology has good advantages as previously explained, however it contains critical flaws as well. The first and most important aspect that had to be improved is the strong dependency of the oscillation frequency on the load impedance, therefore leading to a highly critical mounting. Another problem of this design is that no technique is provided to reduce the noise generated by the current sources (as it will be seen later, a large amount of phase noise is generated by these elements). Therefore an improved version was designed in order to solve these critical issues.
A second VCO topology was published by Li *et al.* [61]. A schematic of the circuit is presented in Fig. 6.4. In order to correctly describe the topology, a simplified schematic

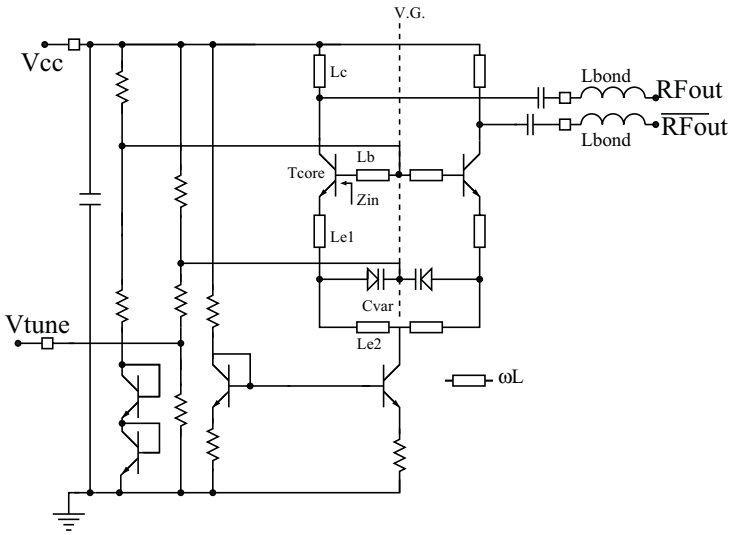

Fig. 6.4: Schematic of the improved topology

containing the most important elements of the IC is shown in Fig. 6.5. The principle of the circuit remains the same. L_{e1}, L_{e2} and C_{var} provide together a capacitive reactance. In opposition to the circuit presented in Fig. 6.3, the inductor L_{e2} places the current source in a virtual ground. Hence, the capacitance C_{tot} of the transistor current source is no more connected to the element C_{var} and therefore does not influence the potential tuning range of the VCO. Another crucial advantage of the component L_{e2} is that together with the capacitance C_{tot} of the current source transistor, L_{e2} provides a low-pass filter that strongly attenuates high frequency noise coming from the current source. In particular, the noise appearing around twice the operation frequency is down-converted into the carrier frequency [62]. Therefore, using this technique substantially improves the noise performance of the oscillator.
In this circuit, L_{e1} is used (together with L_{e2} as well) to improve the loaded quality factor

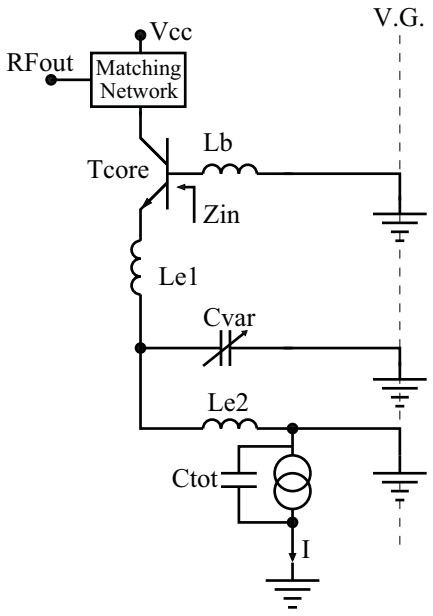

Fig. 6.5: Simplified schematic of the presented topology

of the resonant network thus leading to a further decrease of phase noise. It is essential to choose the values of L_{e1}, L_{e2} and C_{var} in a way that the equivalent circuit of these elements still acts capacitively.

In order to strongly attenuate the current source noise, L_{e2} and C_{var} were chosen in a way that the corner frequency of the filter lies far below the oscillation frequency. The resonant frequency of the network made by L_{e1} and C_{var} was chosen higher than the operation frequency of the circuit.

The equivalent capacitance made by L_{e1}, L_{e2} and C_{var} increases substantially with frequency without any variation of C_{var}. This leads to a higher tuning range.

The previously highlighted techniques allow to reach a very good phase noise performance. However, the presented topology still remains sensitive to a variation of the load impedance if the VCO is intended for multichip system and will be bonded to another IC or, if the oscillator is bonded to an imperfectly terminated transmission line. To solve this problem, a differential common-base transistor pair was added to the previously described configuration. Due to this cascode topology, a slight increase of supply voltage is necessary in order to correctly bias the circuit. This addition to the VCO topology drastically improves the isolation between the oscillator core and the output load. Furthermore, higher output power can be obtained. However, because of the additional active devices, the phase noise performance is slightly degraded.

This topology was chosen for this work. A schematic of the VCO with cascode topology is presented in Fig. 6.6. In order to improve the previously described topology, additional microstrip lines were implemented between the common-emitter and common-base tran-

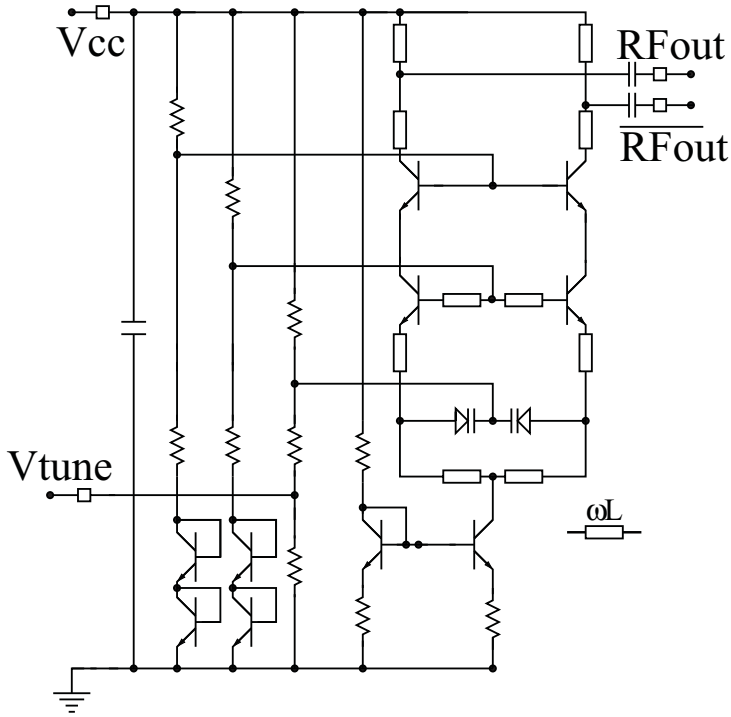

Fig. 6.6: VCO with cascaded differential common-base transistor pair

sistor pairs. These elements improve the interstage matching between the VCO core and the common-base output buffer. Because the designed oscillator is intended to drive a mixer and a frequency divider, a second differential output was added to the standard topology. In this way, the IC can drive differentially the subsequent circuits, resulting in a significant performance improvement. A schematic of the designed version is presented in Fig. 6.7.

Re-use of the topology

The oscillator presented in [61] uses trimmable microstrip lines to allow a wide range of carrier frequencies using a single IC, and also allows rapid correction in case of slight inaccuracies of the simulation. This technique was also used in this study and leads to the possibility of a design re-use. As for the amplifiers described in 5.3.2, a redesign of the mask corresponding to the upper metal layer would allow to obtain an IC suited for mass-market applications. The preparation necessary to obtain the correct line length for each TFMSL is time consuming and, in the absence of FIB, remains a very complex procedure due to the dimensions that need to be dealt with (down to 20μm). Therefore, two versions of the designed VCO were prepared in which no cut was necessary, leading to an immediately possible characterization. The chip photograph of the first version of the

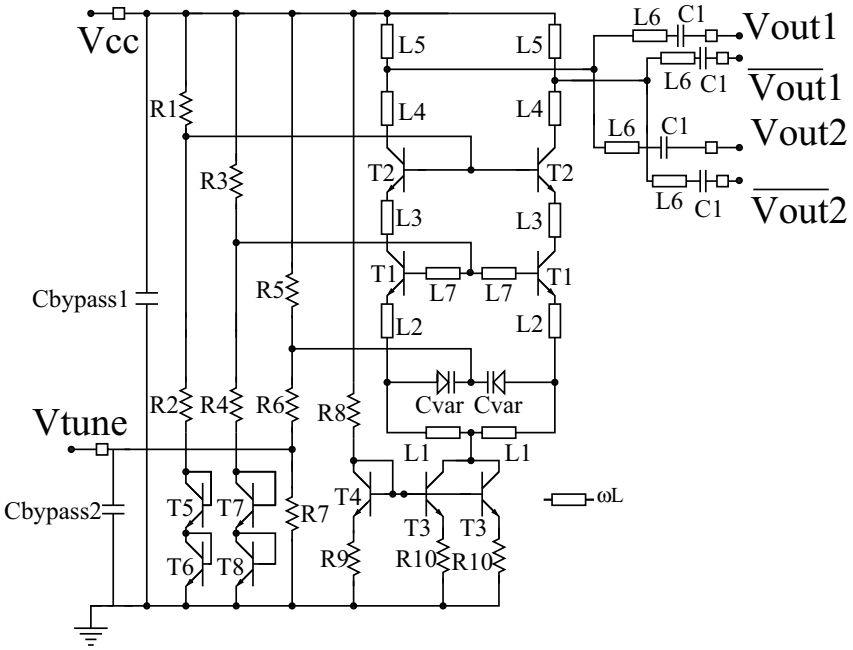

Fig. 6.7: Improved version of the VCO with cascaded differential common-base transistor pair

designed VCOs is presented in Fig. 6.8 (due to the similarity between the different versions, the other chip photos are displayed in Appendix C). This also proves that an easy design re-use is possible by using very simple layout modifications (these changes in the layout were first simulated in order to check the basic VCO operation). The microstrip line elements, which are the most space-consuming elements of the layout, were folded in order to obtain a compact IC, especially the line L_{e2} (see Fig. 6.4) which is the longest line of the whole circuit. Hence, as can be seen, the presented VCOs remain highly compact. Because the designed oscillators are fully differential, the mounting of the circuits and especially the path between the ground of the chip and the ground of the test fixture is in theory uncritical. However, because of layout issues, a perfectly symmetrical IC is very difficult to achieve. Therefore, especially at high operation frequency, it is preferable to use multiple bondwires for the grounding of the chip. Hence, several ground pads were placed around the periphery of the circuit to allow an easier mounting of the VCO. These three ICs have a die area of only $865 \times 565\,\mu\text{m}^2$ including bond pads.

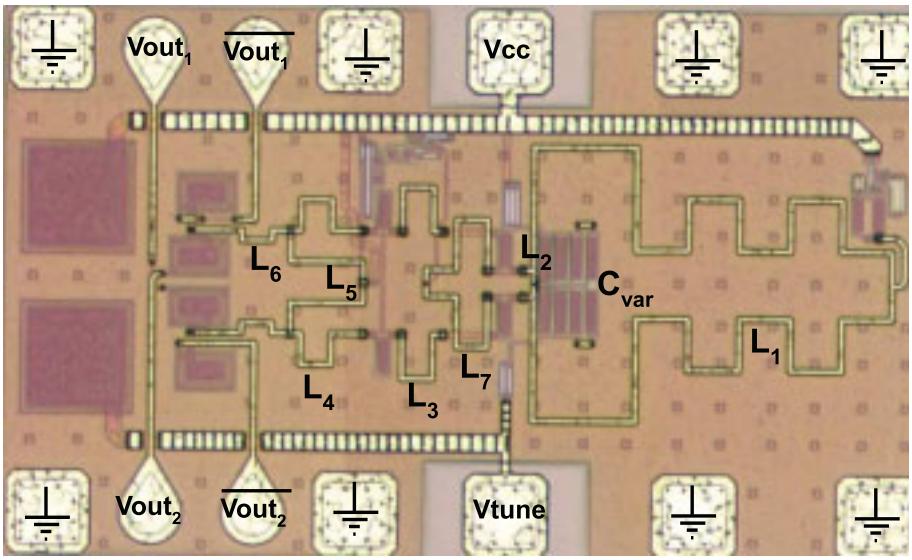

Fig. 6.8: Picture of the 1^{st} version of the VCO with common-base output buffer ($865 \times 565\ \mu m^2$)

6.4 Characterization of the VCOs with common-base buffer

The oscillators were characterized using a spectrum analyzer to determine the frequency tuning range and phase noise, and a power meter to measure the power performance. Because the VCOs have two differential outputs, three of the four signal pads were connected to external $50\,\Omega$ terminations. However, it was carefully checked that all outputs provide the same output power. The circuits were supplied with a DC needle connected to a voltage source. The VCO consumes 52 mA at a supply voltage level of 5 V. A schematic describing the used setup is presented in Fig. 6.9. The losses of the setup were calculated like in Section 8.3.3. The frequency tuning range, the phase noise and output power of the first version are depicted in Fig. 6.10 and 6.11 for a supply voltage level of 5 V. The frequency tuning range, the phase noise and output power of the second version are depicted in Fig. 6.12 and 6.13 (at a supply voltage level of 5 V as well). The frequency tuning range is reasonable and perfectly sufficient for most wireless applications. The delivered power at each differential output of the VCO is perfectly suited to drive a mixer and a frequency divider. As can be seen, the phase noise starts, at low V_{tune}, with acceptable values (below - 70 dBc/Hz at 1 MHz from the carrier) and rapidly de-

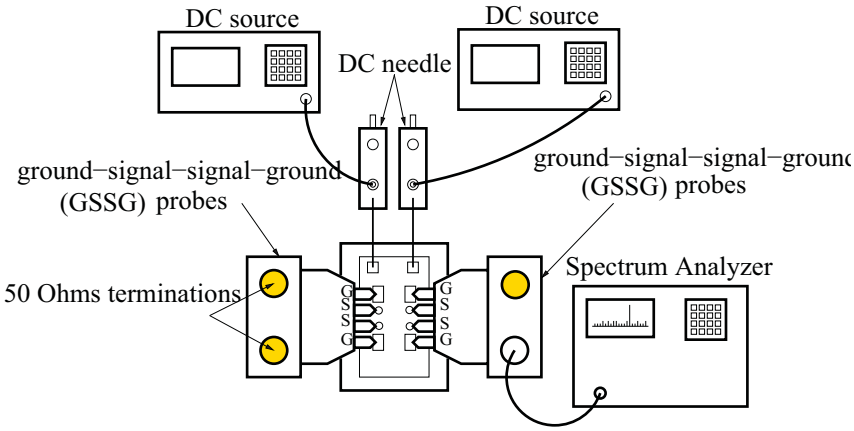

Fig. 6.9: Setup used to characterize the operation frequency and phase noise of the VCOs (to measure the power, the spectrum analyzer was replaced by a power meter)

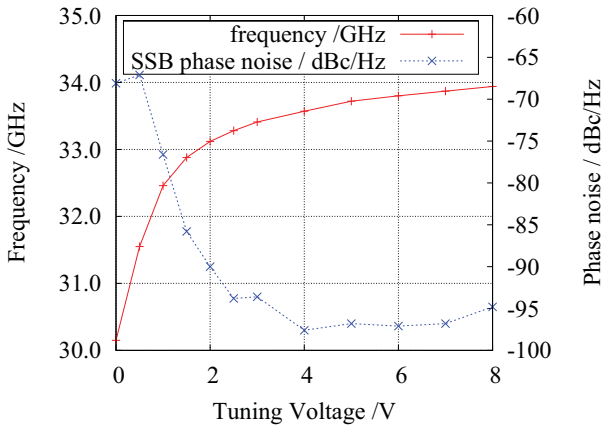

Fig. 6.10: Frequency tuning range and phase noise performance at 1 MHz offset of the 1^{st} version of the VCO with differential common-base output buffer (Vcc = 5 V, I = 52 mA)

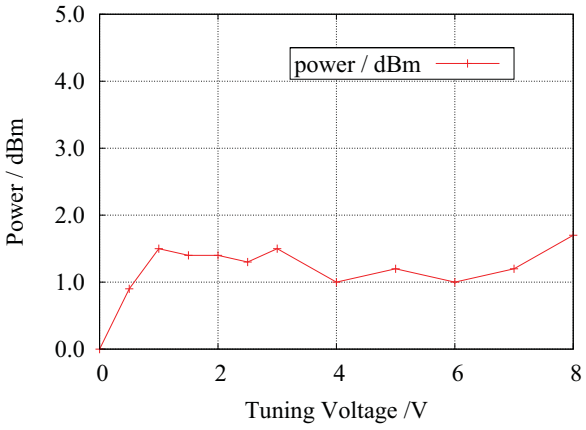

Fig. 6.11: Output power of the 1^{st} version of the VCO with differential common-base output buffer (measurements were performed at one single-ended output of the two differential outputs)

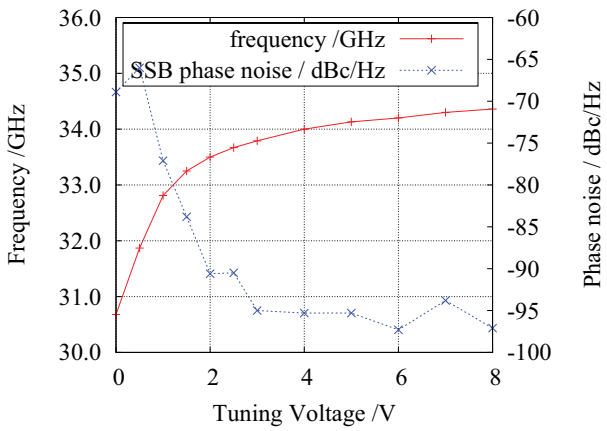

Fig. 6.12: Measured frequency tuning range and phase noise (at 1 MHz offset) of the second version of the oscillator with cascode topology

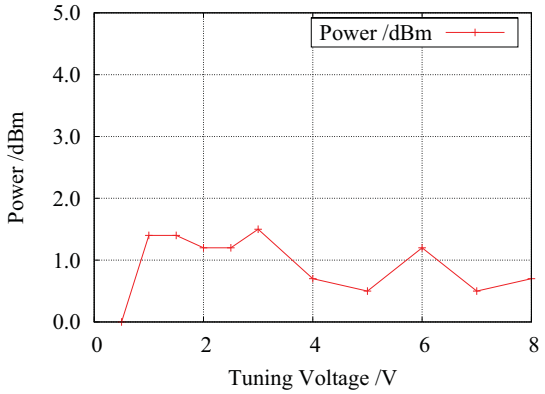

Fig. 6.13: Measured power of the second version of the VCO with cascode topology at one single-ended output of the two differential outputs

creases to reach very good performance for higher V_{tune} (around - 95 dBc/Hz at 1 MHz offset). The deteriorated phase noise for low tuning voltages is due to a slight deviation of the biasing network. As can be seen in Fig. 6.14, the current flowing through V_{tune} is negative for applied voltages below 2.5 V. Because the biasing network was designed in a way that the VCO could be used from $V_{tune} \in$ [0-5 V] with I_{tune} positive, it shows that the varactor diode is forward biased, therefore leading to a higher phase noise. Therefore, the VCOs performance were measured for higher V_{tune} than in the simulation. It should be noted that the V_{tune} pad was connected to a non-ideal voltage source through a DC needle. Therefore, it can be assumed that the biasing of the control voltage has a slight influence on the phase noise performance (noise pickup). A possible improvement could be to use a GSG probe cascaded with a bias-tee or once mounted, to use on-board capacitors to reduce this effect. The advantage of such a topology is the high flexibility regarding layout variation. In order to verify the potential of the realized topology, the varactor made by four parallel transistors had its overall capacitance reduced. This was performed by placing an interconnect on the highest available metal layer. Hence, this interconnect can be easily removed and the equivalent capacitance of the varactor can be significantly reduced. The picture of the varactors with the removable interconnect is presented in Fig. 6.15. The interconnects (one per side) were removed using the FIB technique and the two previously described versions were remeasured with the previously described setup. The measurements (frequency tuning range and phase noise) of the first version with this modification is presented in Fig. 6.16. The power performance is very similar to the previous version and is therefore not presented here. A photo of the spec-

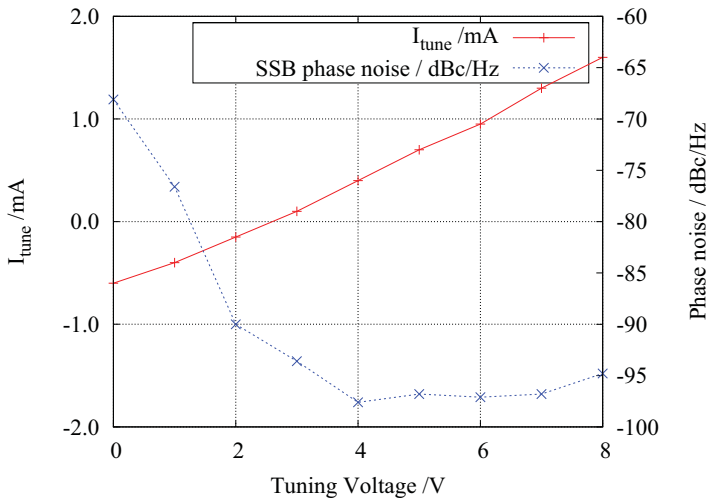

Fig. 6.14: Phase noise and current through the V_{tune} path as a function of the applied tuning voltage (1^{st} version of the VCO with differential common-base output buffer)

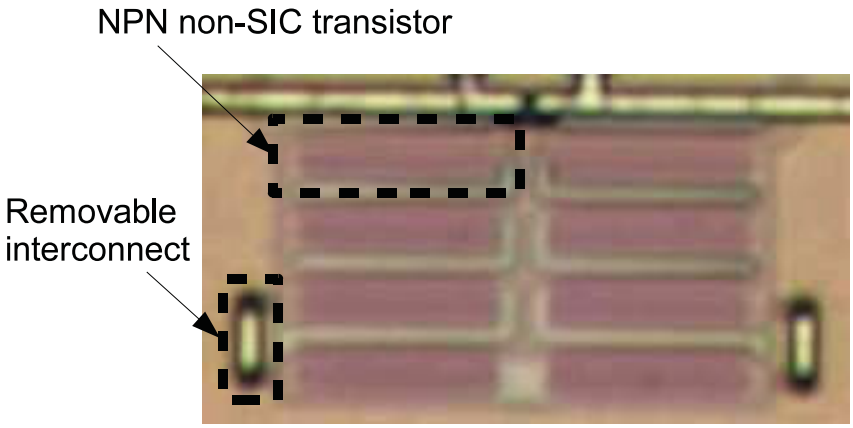

Fig. 6.15: Picture of the varactor used in the VCO with common-base output buffer. The removable interconnect is framed

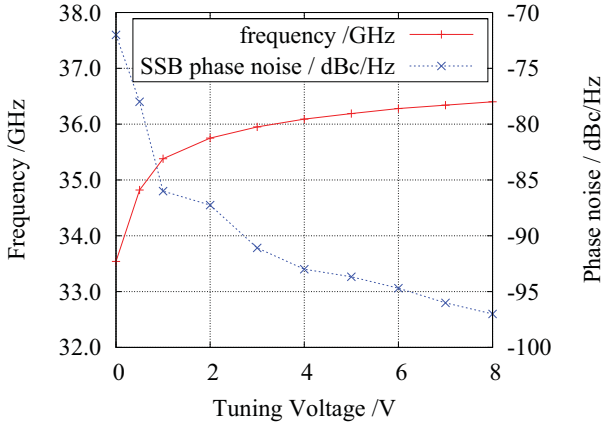

Fig. 6.16: Measured frequency tuning range and phase noise (at 1 MHz offset from the carrier) of the first version of the VCO with differential common-base output buffer (for this measurement the removable interconnect at the varactor was cut)

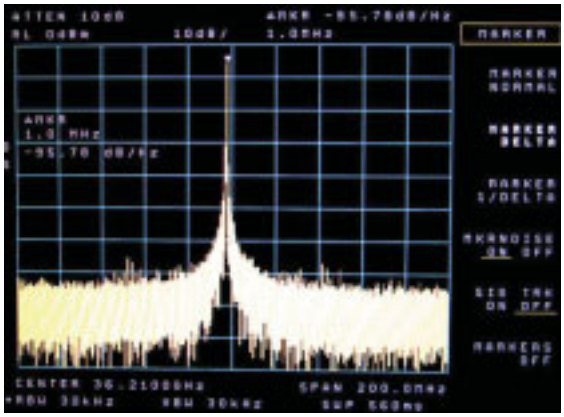

Fig. 6.17: Photo of the measured spectrum (display of the spectrum analyzer). The measurement was performed with Vcc = 5 V corresponding to a drawn current of 52 mA and a tuning voltage of 7 V

trum analyzer display window during measurement is presented in Fig. 6.17. A similar procedure (removal of a varactor by means of FIB technique) was used for the second version as well. The frequency tuning range and phase noise measurements are presented in Fig. 6.18. Again, the power performance is not displayed due to its similarity with the previous measurements. The two previously described measurements were obtained by

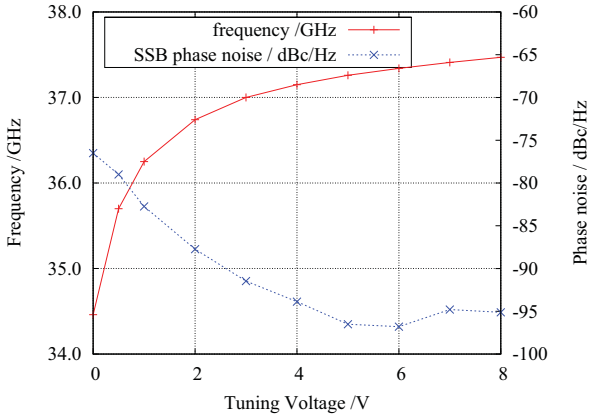

Fig. 6.18: Frequency tuning range and measured phase noise (at 1 MHz offset) of the second version of the VCO with cascode topology (interconnect of the varactor removed)

modifying the varactor configuration. However, it was possible to reach a higher degree

of freedom by working on the TFMSL length. This was performed using the trimmable line technique in the layout of the VCO. By FIB, the electrical length of the lines was chosen slightly shorter than the simulated length while the varactor remained untouched. The characterization of the resulting IC is presented in Fig. 6.19. The power is approx-

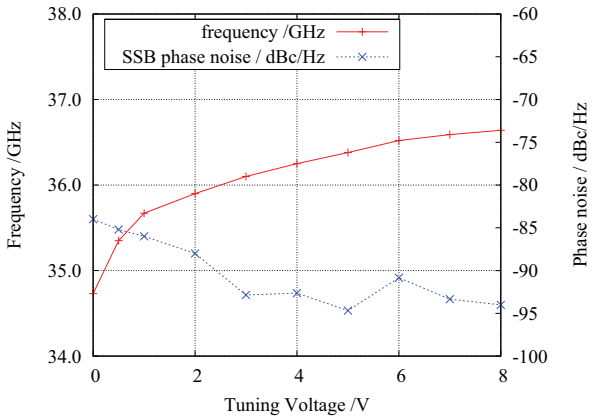

Fig. 6.19: Frequency tuning range and phase noise performance at 1 MHz offset of the VCO with differential common-base output buffer after FIB on the trimmable TFMSLs (Vcc = 5 V, I = 52 mA)

imately 5 dB below the power measured for the previously described VCOs. This can be easily explained by the coupling occurring between the lines and the additional lines necessary to allow the trimmable line technique. It should also be noticed that the FIB procedure is a time-consuming technique (even if the time required between a "FAB-in" and "FAB-out" is drastically higher). However, for first studies, crucial informations can be gathered, therefore leading to a substantial improvement of time.
The previously described topologies were obtained by modifying first the varactor configuration and second the TFMSL length. These two procedures were performed separately, therefore in the future, by combining these two techniques, the 38 GHz region will be reached (which is almost the case here) and this oscillator topology will be used for applications such as LMDS.

6.5 VCO with cascode output buffer

The previously described topology provides wide frequency tuning range, low phase noise and decoupling from a non-ideal loading. However, if higher output voltage swing is required, a different design might be preferred. In this section, a VCO with a different

output buffer is presented. This topology provides higher output power at the cost of a higher power consumption and was previously presented in [63], [64] and [65]. The VCO core is based on the topology presented in Fig. 6.4 in Section 6.5. However, instead of a common-base configuration, an emitter follower pair followed by a cascode amplifier stage was placed at the output of the VCO core. This different topology provides a potential higher output power and a further improved isolation from a non-ideal loading. A simplified schematic is presented in Fig. 6.20. However in this work the authors used

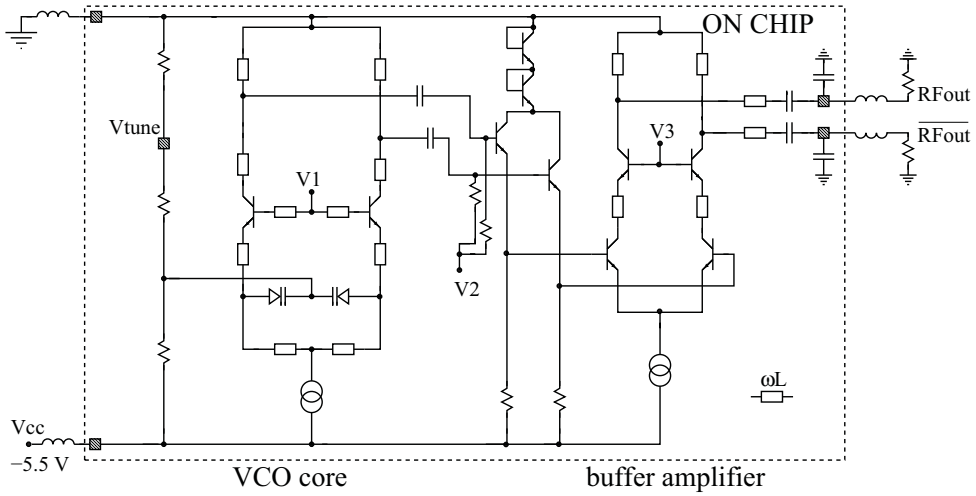

Fig. 6.20: Simplified schematic of the VCO core published in [63]

this oscillator to drive a Tx antenna and thus, the necessary output power was very high (in excess of 16 dBm) leading to a very large DC consumption of 1.2 W. Here, because the output power requirements were not so extreme, the topology was simplified in order to decrease the power dissipation. However, as opposed to [63], a second output buffer was added for the same purpose as in Section 6.5. In order to drastically decrease the dissipated power, the differential emitter follower was omitted. It was simulated that the quality of the matching between the oscillator core and the buffer was acceptable and would lead to a good performance even by using this simplified topology. The complete and detailed schematic of the voltage controlled oscillator with output cascode stage is presented in Fig. 6.21 (only one output buffer is depicted). Because of the more complex design, one of the major issues is the potential parasitic oscillation that might occur within the whole IC. A first technique to verify this was to place probes capable of checking for negative resistances within the schematic (existing tool within ADS). A second technique was to deactivate the oscillator core and run a transient simulation. Within the layout, the interconnects were made as short as possible as well as the ground, power-supply, and bias lines. It should be noted that all parasitic lines must be taken into account in the simulation procedure. In [63], small damping resistors were placed in series within the

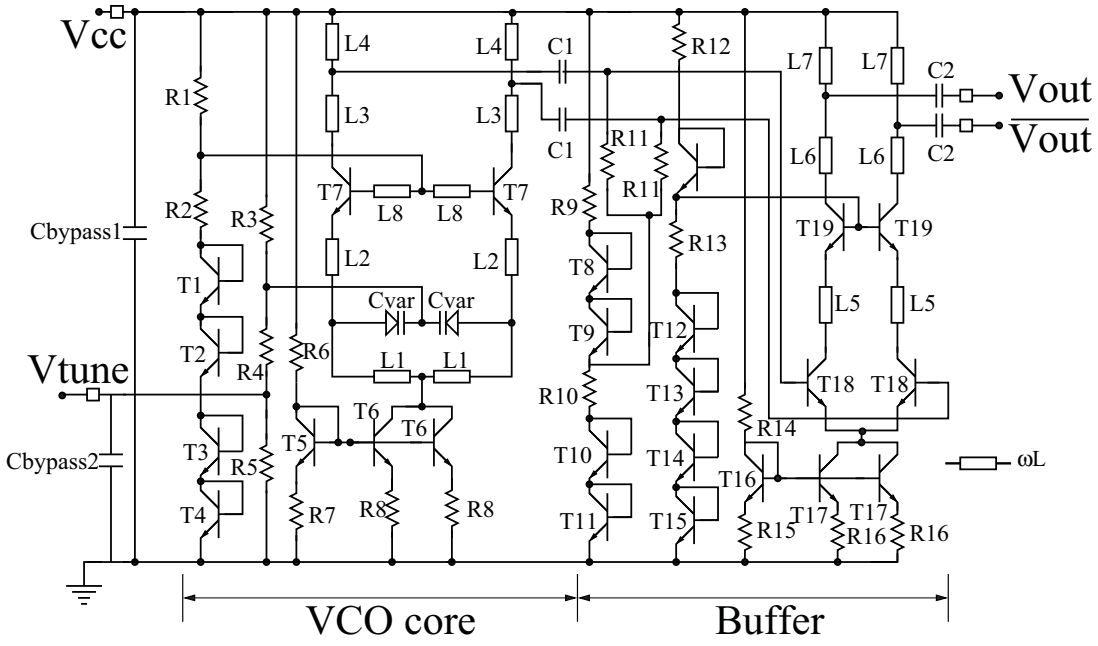

Fig. 6.21: Detailed schematic of the voltage controlled oscillator with output cascode stage

buffer in order to avoid parasitic oscillations. This technique was not used here because of the generated noise that strongly affects the performance of the VCO and lowers the potential output power.

Like for the topology presented in Section 6.5, three versions of the VCO were designed. Two oscillators were layouted with fixed line lengths and with a varactor made with five NPN non-SiC HBTs where one of the transistors can be separated from the varactor, thus leading to a lower overall capacitance and therefore higher operation frequency. The picture of the first version of the designed VCOs is presented in Fig. 6.22 (due to the similarity of the other designed VCOs, they are presented in Appendix C). The die area of these ICs is 890×1000 μm^2.

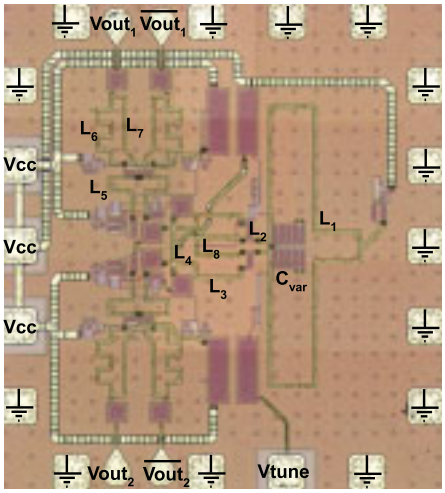

Fig. 6.22: Picture of the voltage controlled oscillator with cascode output buffer (1^{st}version). The IC has a size of 890 × 1000 μm^2

6.6 Characterization of the VCOs with cascode buffer

The measurement procedure was the same as for the previous topology. The measurements of the first topology are presented in Fig. 6.23 and 6.24. The IC was measured at a supply voltage of 5 V. The corresponding current consumption is 126 mA. Because the high output power delivered at each differential output might not be necessary (for instance, the dynamic frequency divider presented in chapter 8 does not need such a high power level to correctly operate), this reasonable power dissipation can be limited by reducing the current consumption on one half of the IC while the other half could for instance drive a Tx antenna. The overall power consumption can also be reduced by using a lower supply voltage level. The VCO operates very well at 4 V supply voltage (with a corresponding current of 75 mA), but with an output power approximately 3 dB lower. The lower phase noise and power performance at low tuning voltage level occur for the same reason than in Section 6.5 and can easily be corrected. The performance of the second version is presented in Fig. 6.25 and 6.26. A picture of the displayed spectrum is shown in Fig. 6.27. Like for the description presented in Section 6.5, one of the transistors used within the varactor could be removed in order to decrease its overall capacitance, resulting in an increase of carrier frequency. The results of this modification on the first version of the VCO are presented in Fig. 6.28 for frequency tuning range and phase noise and in Fig. 6.29 for power. The same procedure was then applied to the second version. Frequency tuning range and phase noise are depicted in Fig. 6.30 and power performance

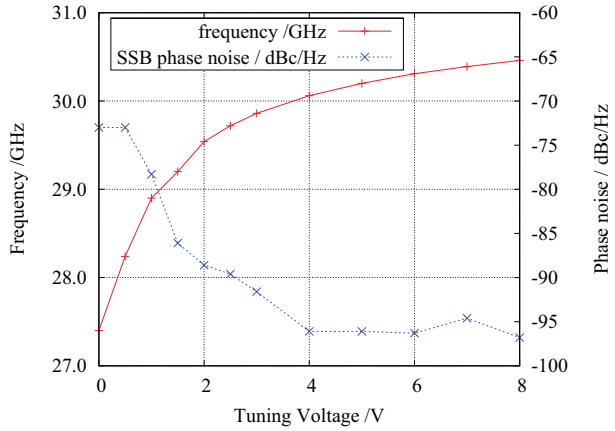

Fig. 6.23: Frequency tuning range and phase noise at 1 MHz offset of the first version of the VCO with differential cascode output buffer (Vcc = 5 V with a drawn current of 126 mA)

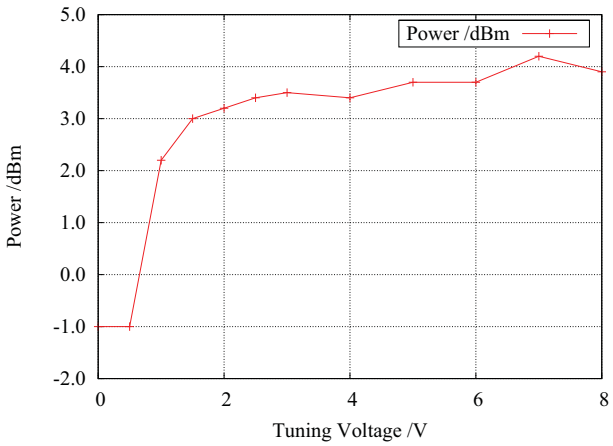

Fig. 6.24: Measured power of the first version of the VCO with differential cascode output buffer

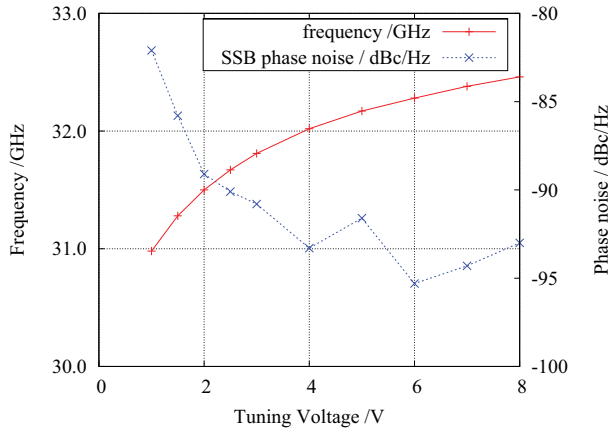

Fig. 6.25: Characterized frequency tuning range and phase noise at 1 MHz offset of the second version of the VCO with differential cascode output buffer (Vcc = 5 V with a drawn current of 126 mA)

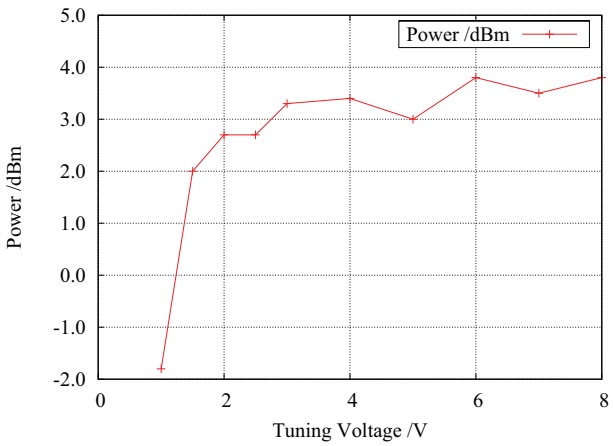

Fig. 6.26: Measured output power of the second version of the VCO with differential cascode output buffer

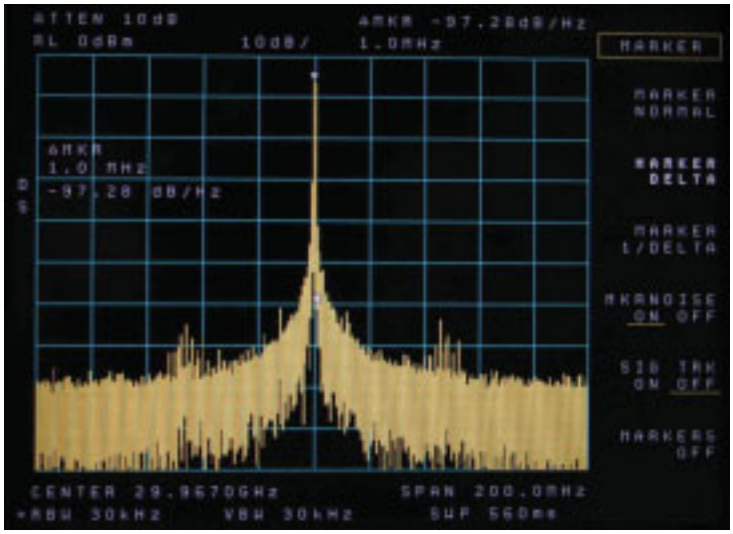

Fig. 6.27: Displayed spectrum of the first version of the VCO with cascode output buffer (Vcc = 5 V, I = 126 mA, tuning voltage is 4 V)

is depicted in Fig. 6.31. All together, the results presented here for this topology demonstrate that the use of a VCO core (presented in Fig. 6.4) with differential cascode amplifier as buffer allows to reach very good performance in terms of frequency tuning range, output power and phase noise.

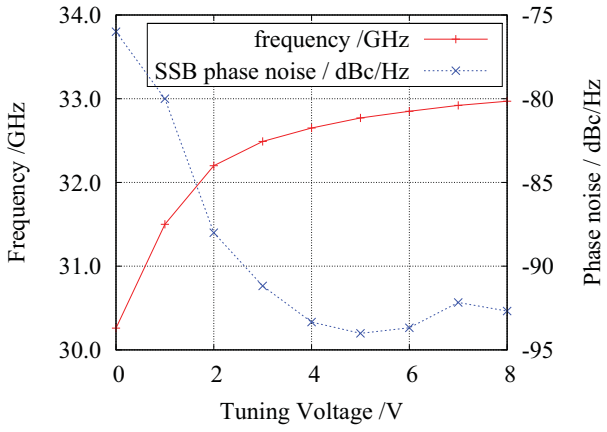

Fig. 6.28: Frequency tuning range and phase noise performance at 1 MHz offset of the first version of the VCO with differential cascode output buffer (interconnect removed, Vcc = 5 V, I = 126 mA)

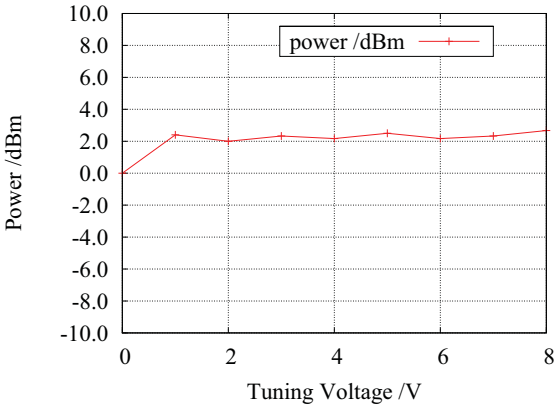

Fig. 6.29: Measured power of the first version of the VCO with differential cascode output buffer (one interconnect of the varactor was removed to decrease its capacitance)

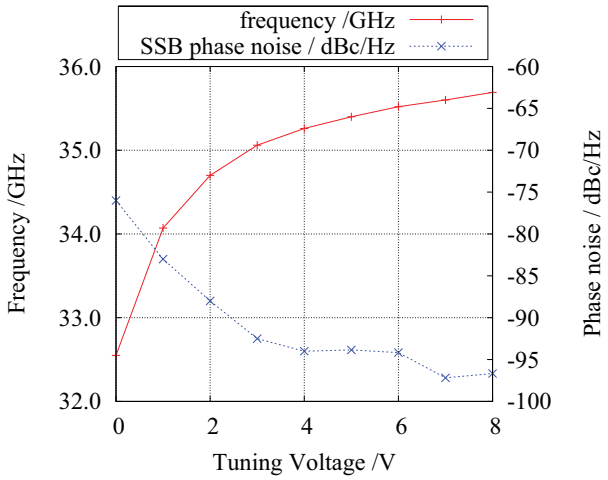

Fig. 6.30: Frequency tuning range and phase noise performance at 1 MHz offset of the second designed VCO with differential cascode output buffer with modified varactor (interconnect removed)

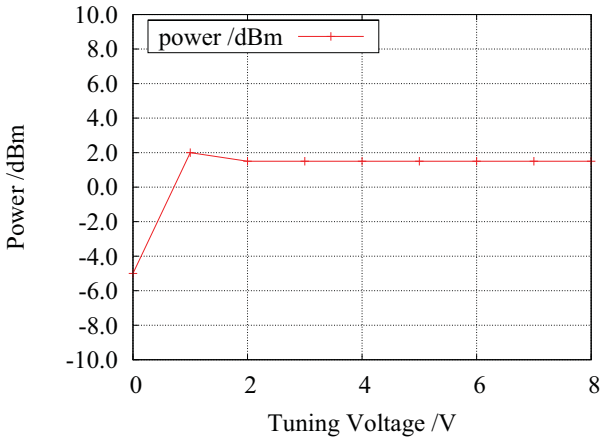

Fig. 6.31: Measured output power of the second version of the VCO with differential cascode output buffer with modified varactor

6.7 Conclusion

In this chapter, two major oscillator topologies were presented. The VCO core uses the negative resistance type oscillator. This negative resistance is created by capacitive degeneration at the emitter. In order to facilitate the mounting of the IC, the VCO is fully differential and provides two differential outputs. This also allows to drive directly e.g. a down-converter mixer and a frequency divider. Because the VCO should be connected to the following ICs using ultrasonic bonding, a buffer has to be provided. Two different types of buffer architectures were investigated.

The first topology consists of a differential common-base transistor technique placed above the VCO core. This allows a reasonable supply voltage level, a low power consumption, good frequency tuning range, very low phase noise and good output power. Because of this simple topology, the layout of this VCO is very compact. By using this addition to the VCO core, the decoupling between the VCO and the output load is significantly improved and therefore the VCO pulling is theoretically inexistent.

The first VCO design provides very high performance, however if higher output power is required, this topology might not be sufficient. Therefore, a second design was investigated. The VCO core remains unchanged, however, the buffer consists here of a differential cascode amplifier cascaded to the VCO. The performance in terms of phase noise and frequency tuning range remains similar to the first architecture. However, the delivered output power is 3 dB higher at the cost of a higher power consumption and

larger die area.
All the previously mentioned topologies were designed with a varactor in which one of the diodes could be removed resulting in a carrier frequency increase. Another technique to verify the potential of the topologies was to use a trimmable line technique. Hence, the electrical length of the thin film microstrip line could be modified leading to an additional degree of freedom. Using these two mentioned techniques, the center frequency was significantly elevated (up to 15 %) without lowered performance.
All these measurements prove that very good RF sources can be generated far beyond one third of the f_T. An overview of the measured performance of the VCOs is presented in Tables 6.1, 6.2 and 6.3. The values and parameters of several of the designed VCOs are presented in Appendix D.

Version	1^{st} version	2^{nd} version	1^{st} version *	2^{nd} version *
Icc /mA	52	52	52	52
Vcc /V	5	5	5	5
(f_{min}-f_{max})/GHz	30.15-33.94	30.51-34.36	33.54;36.4	34.46;37.47
Phase noise (1 MHz offset) /dBc/Hz	-67.1 (worst) -97.1 (best)	-66 (worst) -97.3 (best)	-72 (worst) -97 (best)	-76.5 (worst) -96.8 (best)
Output power /dBm**	1 +/- 1	1 +/- 1	1 +/- 1	1 +/- 1
Layout size /μm^2	865 × 565	865 × 565	865 × 565	865 × 565

Tab. 6.1: Performance overview of the measured VCOs with common-base output buffer (*: In this version, the overall capacitance of the varactor was decreased by removing one of the transistors used as diode. **: At one single-ended output of the two differential outputs.)

Version	Version with adjustable line technique
Icc /mA	52
Vcc /V	5
[f_{min}-f_{max}]/GHz	34.73-36.64
Phase noise (1 MHz offset) /dBc/Hz	-84 (worst) -94.68 (best)
Output power /dBm	-4 +/- 1
Layout size /μm^2	865 × 565

Tab. 6.2: Performance overview of the measured VCO with common-base output buffer (version with adjustable line technique)

Version	1^{st} version	2^{nd} version	1^{st} version *	2^{nd} version *
Icc /mA	126	126	126	126
Vcc /V	5	5	5	5
(f_{min}-f_{max})/GHz	27.4-30.46	30.98-32.46	30.26;32.97	32.55;35.69
Phase noise (1 MHz offset) /dBc/Hz	-73 (worst) -96.8 (best)	-82.1 (worst) -95.3 (best)	-76 (worst) -94 (best)	-76 (worst) -97.18 (best)
Output power /dBm**	3 +/- 1	3 +/- 1	2 +/- 1	2 +/- 1
Layout size /μm^2	890 × 1100	890 × 1100	890 × 1100	890 × 1100

Tab. 6.3: Performance overview of the measured VCOs with cascode output buffer(*: In this version, the overall capacitance of the varactor was decreased by removing one of the transistors used as diode. **: At one single-ended output of the two differential outputs.)

6.8 Comparison with previously published oscillators

The following table gives an overview of previously published oscillators fabricated on various technologies for comparison. Like in chapter 5, the designed VCOs achieve very good performance using a low-cost technology.

	P_{DC} /mW	f_{min}-f_{max} /GHz	Phase noise (1 MHz offset) /dBc/Hz	Output power /dBm	Technology
this work	260	34.46-37.47	-76.5 (worst) -96.8 (best)	1 +/- 1	Atmel SiGe2RF 0.8 μm SiGe HBT
this work	630	30.98-32.46	-82.1 (worst) -95.3 (best)	3 +/- 1	Atmel SiGe2RF 0.8 μm SiGe HBT
[66]	303	44.4-47.1	-93 (worst) -104 (best)	0	0.14 μm SiGe HBT
[67]	12.8	40	-90	1	0.13 μm SiGe BiCMOS
[68]	11.25	36.3-40.5	-90.03	-7.9	0.13 μm SOI CMOS
[69]	105.6	18.5-25	-85	-15	0.12 μm SiGe BiCMOS
[70]	105.6	35.2-37.6	-105 (2MHz offset)	≈ -14	0.25 μm SiGe BiCMOS

Tab. 6.4: Overview of previously published VCOs

Chapter 7

Fully Balanced Down-Converter Mixer

7.1 Introduction

Down-converter mixers are frequency translation circuits which allow the conversion of signals from a high frequency (RF signal) to a lower intermediate frequency (IF signal) in a receiver chain. The opposite is also possible (up-conversion of an IF signal to an RF signal), however this design aspect is out of scope here. Several well-known architectures can be used to realize mixing. However, due to the low-resistivity silicon substrate or the high frequency, several topologies, such as e.g. the rat race mixer [71] due to the high losses, had to be excluded.
In this chapter, the fundamentals of mixers are shown, then the simulation and characterization of a fully differential millimeter-wave down-converter mixer are presented.

7.2 Fundamentals of mixers

A mixer is a nonlinear circuit that combines two signals in order to produce the sum and difference of the two input frequencies at its output. Such effect can be described by means of a mathematical approach. To analyze a mixer, the circuit is expanded as in the block diagram presented in Fig. 7.1. g(t) can be written:

$$g(t) = f_1(t) + f_2(t) \tag{7.1}$$

and by means of the taylor series,

$$h(t) = H_1 \cdot [f_1(t) + f_2(t)] + H_2 \cdot [f_1(t) + f_2(t)]^2 + ... \tag{7.2}$$

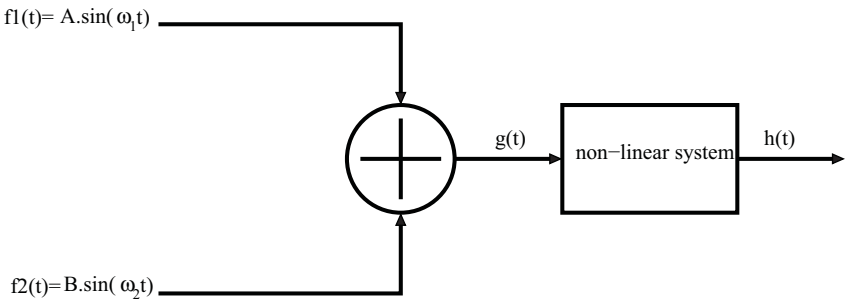

Fig. 7.1: Block diagram of a mixer

The equation (7.2) can be rewritten:

$$h(t) = H_1 \cdot [A.sin(\omega_1 t) + B(\omega_2 t)] + H_2 \cdot [A.sin(\omega_1 t) + B \cdot sin(\omega_2 t)]^2 + ... \tag{7.3}$$

$H_2 \cdot [A \cdot sin(\omega_1 t) + B \cdot sin(\omega_2 t)]^2$ can be expanded:

$$H_2 \cdot [A \cdot sin(\omega_1 t) + B \cdot sin(\omega_2 t)]^2 = H_2 \cdot \left[A^2 \cdot sin^2(\omega_1 t) + B^2 \cdot sin^2(\omega_2 t) + 2 \cdot A.B.sin(\omega_1 t) \cdot sin(\omega_2 t)\right] \tag{7.4}$$

$2 \cdot A \cdot B \cdot sin(\omega_1 t) \cdot sin(\omega_2 t)$ becomes:

$$A \cdot B \cdot [cos(\omega_1 + \omega_2)t + cos(\omega_1 - \omega_2)t)] \tag{7.5}$$

Therefore the sum and difference of the input waves are obtained through non-linearity.

7.3 Double balanced mixer

As previously explained, several design topologies can be chosen in order to generate a frequency translation. Using FET or Si CMOS technologies, a widely used architecture is the passive mixer [72–74]. Passive mixers are usually defined as mixers having a power gain below one between the RF and IF ports and do not consume power. In this approach, if e.g a FET transistor is used to design the mixer (passive mixer can also be designed using diodes [71]), it is not biased in the active region but at $V_{DS} \approx 0$ and acts as a voltage controlled resistor. This leads to a low-noise and a high linearity, however such topologies show high loss and high LO power is often required which makes it not suitable for highly integrated or low power systems.

For microwave and millimeter-wave ICs based on Si bipolar technologies, the active mixer is a good topology. Active mixers typically are mixers having a power gain greater than unity and therefore require active devices biased in the active region. Once again, several approaches exist. There are two widely used types of mixers: balanced and unbalanced mixers. Unbalanced mixers do not reject RF-IF and LO-IF, nor LO-RF feed-through

[75, 76]. Therefore the port-to-port isolation is very poor. Single-balanced active mixers [77] have good RF-IF and LO-RF isolation, but do not avoid LO-IF feed-through [76]. Because of its symmetrical topology, the fully differential (or double-balanced) mixer overcomes very well this issue [76] and was therefore the investigated topology in this work.

A fully balanced active mixer using bipolar devices is designed using a Gilbert cell mixer topology. The block diagram presented in Fig. 7.2 gives an overview of the operation principle of the mixer. The RF signal is applied to the lower transistors which form a

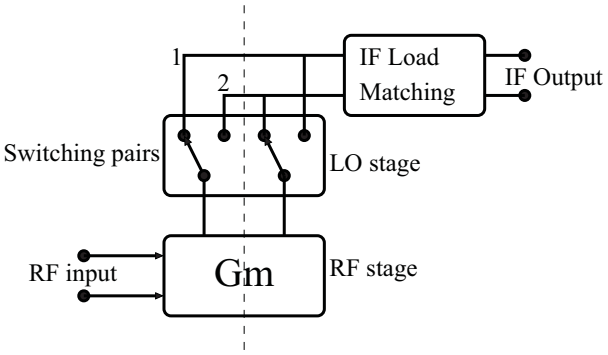

Fig. 7.2: Operation principle of a Gilbert cell mixer

differential amplifier. The LO signal is applied to the upper transistors, which act as switches (as in a diode ring mixer). The sampled current is then converted to voltage through the IF load (usually performed with high value resistors in the case of a down-converter).

At microwave and millimeter-wave frequencies, the aforementioned blocks of the Gilbert cell mixer can be very easily monolithically integrated, resulting in a compact IC. The RF stage is designed using an emitter-coupled pair (even if several publications show that a common-base transistor pair might be a potential solution in the case of required high linearity [78]). In this work, because of the low available gain, the common-emitter transistors are biased in class-A, however, for mixers where the power consumption is highly critical, the RF transistor pair can be biased at e.g. class-AB or even class-B [79]. The upper transistor block of the mixer is realized using four common-emitter transistors driven with high input voltage swing (LO side). As previously mentioned, the loading is realized using on-chip resistors. A schematic of a standard Gilbert cell mixer is presented in Fig. 7.3. At the output of the mixer core, a differential common-collector stage (emitter follower) is implemented. The high input impedance of the buffer stage allows to convert the switched output current into high output voltage.

As previously described, the fully balanced Gilbert cell mixer has an excellent port-to-port isolation. A good LO suppression at the IF port is very important because a high

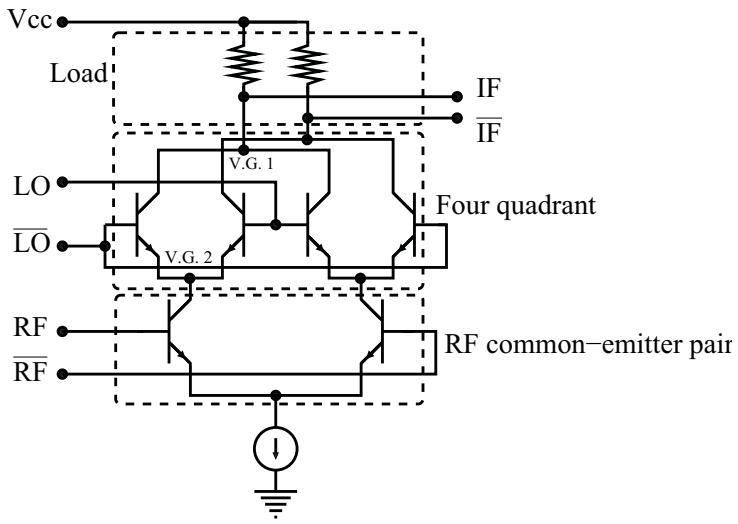

Fig. 7.3: Schematic of a standard Gilbert cell mixer

LO power at the IF output might lead to the saturation of the following stage. In e.g. a radiometer system, a LO leakage through the RF port might be sent through the Rx antenna and be reflected back to the same antenna and would lead to misleading informations. The RF-IF isolation is usually less important because of the much lower power of the RF signal compared with P_{LO}. The isolation is realized by using the 180° phase shift which generates a virtual ground (see in Fig. 7.3: $V.G._1$ and $V.G._2$). Therefore out-of-phase signals are filtered out. However, perfect port-to-port isolation will only occur if the signals are perfectly 180° phase shifted. Therefore special emphasis has to be placed on keeping the layout as symmetrical as possible in order to mitigate any leakage. Additionally, because of the large spectral separation between LO/RF and IF, a simple shunt capacitor pair placed between the Gilbert cell core and its output buffer stage is implemented to act, together with the load resistors, as a low-pass filter and strongly attenuate the high frequency components. A block diagram of the corresponding Gilbert cell mixer and its complete schematic are depicted in Fig. 7.4 and 7.5, respectively. For AC coupling, the RF and LO differential inputs are connected to 300 fF nitride capacitors. Therefore, no SMD elements will be necessary at the input for the mounted chip. Because of the large required value of the blocking capacitors at the IF output, these elements will be provided on-board. The usual technique to provide a current source at the RF emitter-coupled pair is to use a resistor with high value or a current mirror. However, these two topologies create a voltage drop leading to a higher necessary supply voltage. Therefore, an inductive RF current source was implemented in this design. This reactive element provides a high impedance and therefore allows a very good common-mode rejection. Because of the very low resistance across the spiral coil, the voltage drop is negligible. To

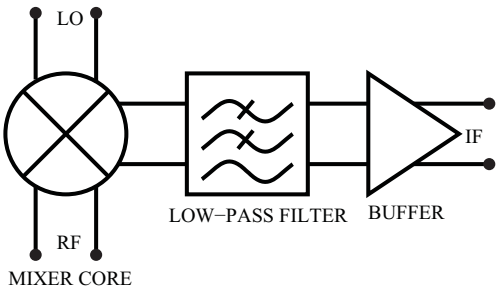

Fig. 7.4: Block diagram of the Gilbert cell mixer

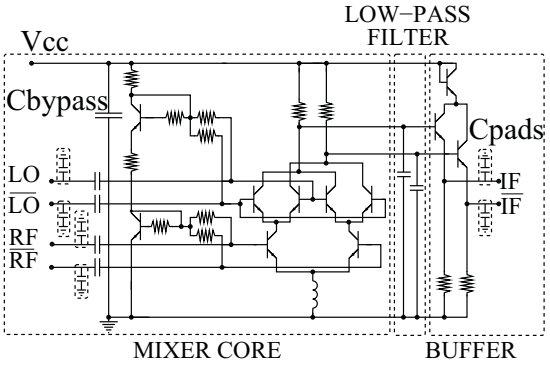

Fig. 7.5: Complete schematic of the fully balanced mixer based on the Gilbert cell topology

provide good RF filtering along the supply voltage path, a large on-chip shunt capacitor (C_{bypass})was provided. The biasing of the IC was provided by means of a current mirror. Due to the fact that the mixer is fully differential, the IF output signal is decoupled from the DC path and does not necessitate any additional filtering along the biasing line. However, because of potential asymmetric layout, an off-chip shunted capacitor might be additionally implemented to the test fixture.

Re-use of the topology

Because the purpose of this mixer was to be implemented in various types of applications operating at different frequencies (between 24 GHz and 40 GHz), a narrow band matching using reactive elements was not performed (such approach is very often used for Gilbert cell mixer [80–82]). However, it was simulated that the VCOs presented in Chapter 6, if connected to the fully differential mixer, had perfectly sufficient output power to drive the LO input of this IC. Because the VCO core is very well decoupled, the impedance of the mixer will have no influence on the oscillation frequency. Within the layout, the transistors will be placed in close vicinity, therefore parasitic coupling will occur. However, because the modeling of this effect is an extremely challenging task for such a complex structure, it was not performed for this design.

7.4 Layout and measurements

The circuit topology comprises only one single inductive element used as current source, therefore the layout of the designed Gilbert cell mixer is extremely dense (only $530 \times 450\ \mu m^2$).

Because of the high frequency and the lossy interconnect, the RF and LO paths were designed as compact as possible. In order to limit leakage (or feed-through) which would result in mediocre port-to-port isolation, the layout was also kept as symmetrical as possible. This drastically decreases the phase and amplitude shift at the IF output. A chip photo of the IC is presented in Fig. 7.6. The necessary measurement setup used to char-

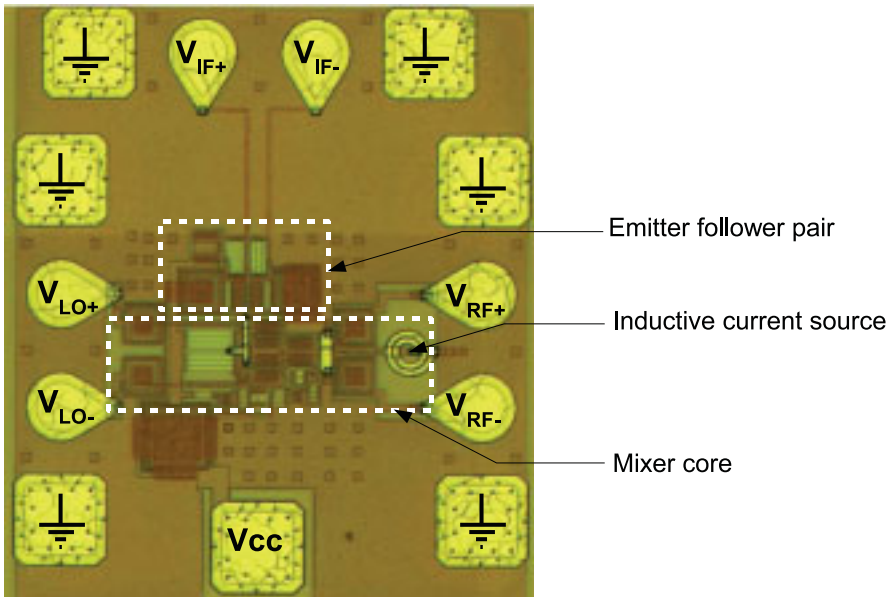

Fig. 7.6: Chip photo of the fully differential down-converter mixer (530 × 450 μm^2)

acterize the Gilbert cell mixer is complex because of the significant number of probes and the extreme compactness of the IC leading to RF probes positioned in close vicinity. Like for the previously presented differential ICs, the mixer was characterized single-endedly. Since only one signal source was available during the measurement of the circuit, a vector network analyzer was used in continuous wave mode. However, because of the poor power capability of this measurement equipment, the LO and RF compression points of the mixer could not be characterized. The LO input was connected to the signal source because of the higher required power, while the IF output was detected with a spectrum analyzer and with an oscilloscope afterward. The simulation of the mixer was repeated, reproducing the measurement conditions. The picture in Fig. 7.7 and the schematic in Fig. 7.8 provide an overview of the measurement setup. The measurements were performed in two steps. First the delivered output power at the LO input was kept constant at 1 dBm while the RF power was swept up to the maximum available output power of the network analyzer. Then, the power at the RF side was kept constant (-13.3 dBm) while the LO power was swept. All these procedures were performed for a supply voltage level of 4 V and for frequencies from 30 GHz up to 40 GHz (frequency limit of the used signal

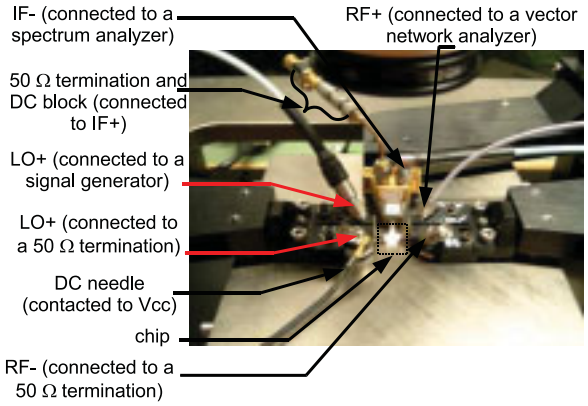

Fig. 7.7: Photo of the mixer measurement setup

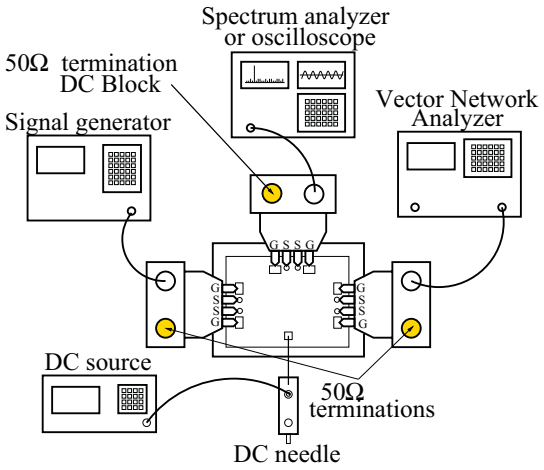

Fig. 7.8: Description of the measurement setup

source). The RF and LO frequency were always adjusted as to obtain an IF frequency of 100 MHz. The conversion gain of the mixer driven single-endedly at a 4 V supply voltage (corresponding to a drawn current of 51.5 mA) and constant LO power (1 dBm) is presented in Fig. 7.9. The conversion gain of the Gilbert cell mixer driven single-endedly at a 4 V supply voltage and constant RF power (-13.3 dBm) is presented in Fig. 7.10. For both graphs, the simulated conversion gain of the IC when driven differentially and single-endedly is presented. As previously explained, due to the power limitation of the available measurement setup, the 1 dB compression point could not be characterized. Measurements are approximately 4 dB lower than the simulation, which can be explained by e.g. substrate coupling between transistors due to the extreme compactness of the layout. However, by removing 4 dB from the simulated performance of the mixer driven differentially, a conversion gain is still obtained, which was the main target during the design procedure of this very broadband mixer. The simulated linearity shows a $P_{1dB,in}$ at the RF side of 2.5 dBm, which is perfectly sufficient when compared to the $P_{1dB,out}$ of the LNAs described in Chapter 5. The differential output voltage was also measured with an oscilloscope in order to detect potential phase and amplitude shifts. A photo of the oscilloscope display is presented in Fig. 7.11. As can be seen, the two output signals are well out-of-phase and the amplitude shift is of approximately 1.1 dB.

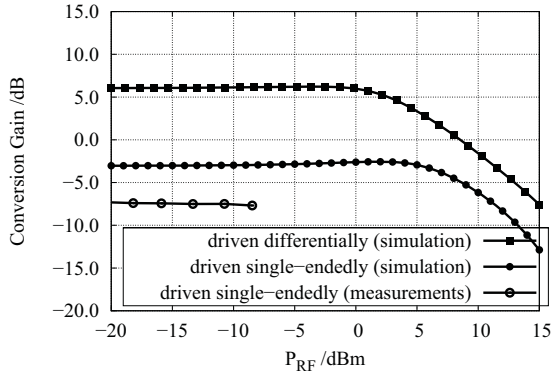

Fig. 7.9: Conversion gain of the mixer at constant LO power (1 dBm) with f_{RF}=30 GHz and f_{LO}=30.1 GHz (Vcc=4 V)

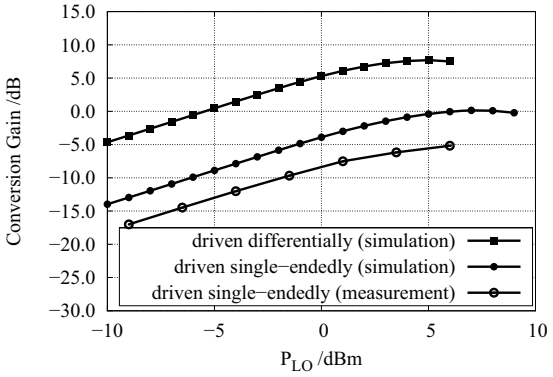

Fig. 7.10: Conversion gain of the mixer at constant RF power (-13.3 dBm) with f_{RF}=30 GHz and f_{LO}=30.1 GHz (Vcc=4 V)

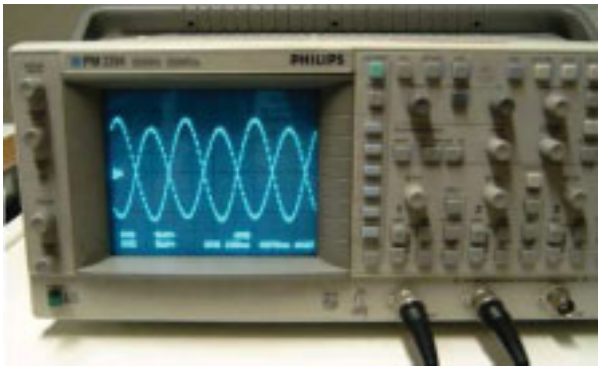

Fig. 7.11: Display of the differential output voltage of the mixer

7.5 Conclusion

In this chapter, a fully differential down-converter mixer was presented. Due to the fact that the design is based on bipolar devices, the most appropriate topology is the Gilbert cell mixer. Because of the wide spectral range for which this IC was conceived, no specific narrow band matching was provided. However, like previously emphasized (see page 69), this approach is not problematic and allows sufficient performance for the targeted purpose. After successful simulation, the circuit was carefully laid out in order to generate a highly compact IC (530 x 450 μm^2). The circuit was characterized single-endedly at different frequency ranges. A moderate inaccuracy between simulation and measurement was found, which can be explained by the use of a lossy substrate and its unavoidable parasitic coupling generation between active devices. However, the overall performance including expected conversion gain, power consumption, compactness remains very good. The summarized performance of the mixer is presented in Table 7.1. The values and parameters of this IC are presented in Appendix E.

	Power consumption	Gain (P_{LO}=1 dBm)	$P_{1dB,in}$ (P_{LO}=1 dBm)	Chip size
Simulation differentially	208 mW	6 dB	2.5 dBm	-
Simulation single-endedly	208 mW	- 3.1 dB	7 dBm	-
Measurement single-endedly	206 mW	- 7.3 dB	n.a.	530 $\times$ 450 μm^2

Tab. 7.1: Summarized performance of the mixer

Chapter 8

High Performance Frequency Dividers

8.1 Introduction

Frequency division is an essential function in today's RFIC systems such as wireless transceivers and FMCW radar systems, and is an integral part of PLLs. In standard PLLs, the output signal of the VCO is divided down in order to enable comparison with a reference stable source operating at much lower frequency. A critical issue of frequency dividers is the power dissipation. In order to obtain a reasonably low output frequency, dividers need a high divide ratio when connected to millimeter wave VCOs, which leads to a drastic increase of power consumption that degrades the overall performance of the designed system. Two main topologies are chosen to perform a frequency division: The dynamic topology (also called analog or regenerative frequency divider) and the static, also called digital. This chapter deals with efficient design topologies used in this work. The first section will describe the dynamic frequency divider, then the static divider topology will be briefly presented and finally the measurement results of a 32:1 frequency divider will be illustrated.

8.2 Divider using second-order regenerative modulator

The major advantages of the regenerative frequency divider (RFD) compared to the static topology are a higher maximum frequency of operation and a theoretically lower power consumption (due to a lower amount of transistors). The main drawback is a narrower

operation bandwidth. Even if the dynamic frequency divider is a widely used approach to achieve frequency division, its operation principle is often not well understood. Therefore, in this chapter, the fundamental theory of the dynamic frequency divider will be presented. At first, the operation of the analog frequency divider may seem straight forward. As described in the block diagram shown in Fig. 8.1, the complete divider consists of a mixer (or modulator), a low-pass filter and an amplifier. If we consider the most general case

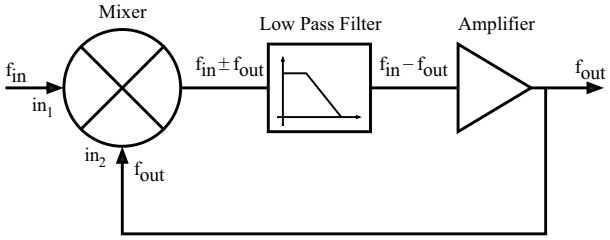

Fig. 8.1: Block diagram of the regenerative frequency divider

for such a circuit configuration, we obtain

$$nf_{in} - mf_{out} = f_{out} \quad (nf_{in} > mf_{out}) \tag{8.1}$$

or

$$mf_{out} - nf_{in} = f_{out} \quad (nf_{in} < mf_{out}) \tag{8.2}$$

Where f_{in} is the frequency of the signal applied at the input of the complete RFD, f_{out} the frequency of the signal fed back to the balanced or conjugate input of the mixer and m,n are integer describing the modulation order (defined as the sum of m and n).
By simplifying the two previously stated relations, we have:

$$f_{out} = \frac{n}{m \pm 1} f_{in} \tag{8.3}$$

However, the previously stated equations are only valid if the feedback path does not create nonlinearity. As explained in [83], if harmonics of f_{out} are generated in the feedback circuit (see Fig. 8.2), the equation 8.3 has to be rewritten the following way:

$$f_{out} = \frac{n}{rm \pm 1} f_{in} \tag{8.4}$$

Where r is an integer describing the harmonics created in the feedback circuit. This general case shows that greater submultiple ratios than n/(m±1) can be generated by using a given modulator and a harmonic generator (e.g. frequency multiplier). In this work, a second-order modulator (n=m=1) will be used and it will be assumed that no nonlinearity is created through the feedback path. Therefore the equation 8.4 becomes:

$$f_{out} = \frac{1}{2} f_{in} \tag{8.5}$$

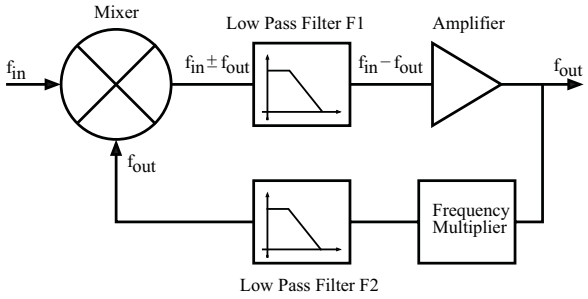

Fig. 8.2: Block diagram of the regenerative frequency divider with an added nonlinear circuit

However, in the Fig. 8.1, a very important assumption is used to obtain the previously stated general relations: from the beginning we assumed that the frequency f_{out} was already present in the feedback path. A very obvious question is now: where does the frequency f_{out} come from in the first place?. To answer this important question, the input wave will be written as follows:

$$e_{in} = E_{in}cos(wt) \tag{8.6}$$

and the frequency at the mixer second input in_2

$$e_{out} = E_{out}cos(\frac{\omega t}{2} + \varphi). \tag{8.7}$$

Consequently, the sideband outputs can be written

$$e_{sb} = A_{mod}E_{in}E_{out}[cos(\frac{\omega t}{2} - \varphi) + cos(\frac{3\omega t}{2} + \varphi)] \tag{8.8}$$

Because of the low pass filter present in the feedback path, the component $3\omega/2$ is strongly attenuated and can be omitted, therefore we obtain:

$$e_{sb} = A_{mod}E_{in}E_{out}[cos(\frac{\omega t}{2} - \varphi)]. \tag{8.9}$$

For a given signal e_{in} and therefore a given amplitude E_{in}, the product A_{mod} E_{in} is constant. If the gain of the amplifier is greater than the losses of the modulator and the low pass filter, the wave with frequency component $\omega/2$ will be reapplied to the input in_2 with a greater amplitude than the original component. Thus, no matter how small E_{out} is, the division will be sustained. Consequently, whether the origin e_{out} is based on thermal noise, transient produced by the signal e_{in}, etc., the division will be obtained.
The starting condition previously stated is actually very similar to an oscillator. However, if the input signal is not present or is too small, the losses of the system will not be compensated and the starting condition will not be fulfilled. Therefore, a minimum signal amplitude (also called input sensitivity) is necessary and is the most fundamental figure

of merit for frequency dividers.
In order to pursue this study, it is important to establish the relation between the wave contained in the feedback (8.7) and the produced lower sideband (8.8). This relation can be written:

$$E_{out}cos(\frac{\omega t}{2} + \varphi) = A_{amp}A_{mod}E_{in}E_{out}cos(\frac{\omega t}{2} - \varphi + \theta) \tag{8.10}$$

where A_{amp} is the gain of the amplifier in the feedback path and θ the phase shift of the amplifier and the filter (the latest being usually a part of the amplifier).
We can take separately phase and amplitude components from 8.10. This will be:

$$A_{amp} = \frac{1}{A_{mod}E_{in}} \tag{8.11}$$

and

$$\varphi = \frac{\theta}{2} \tag{8.12}$$

Because as explained previously, the operation of an RFD is analogous to the operation of an oscillator, remains the question of the phase relation between the output of the modulator and the feedback input. If we look at the relation (8.12), it can be seen that the phase shift in the feedback circuit will always adjust itself with respect to the input signal.
As mentioned, the circuit will operate if $A_{amp}A_{mod}E_{in}$ is greater than one. For the system to reach equilibrium, at constant E_{in}, either A_{amp} or A_{mod} must decrease. This behavior can be obtained through saturation (due to device physical limitation).

8.3 Divider using a fully differential Gilbert cell topology

8.3.1 Design philosophy

To design an RFD, a first approach would consist of designing the mixer, low pass filter and amplifier separately as shown in Section 8.1. Actually, this was the way it was performed in the very first designs of this topology. However, it is possible by means of adequate design architecture to reproduce each separate block of the RFD using a single and compact topology. In this work, an RFD using a Gilbert cell topology was studied. One of the first implementations of this architecture appeared in [84]. The standard topology (see Fig. 8.3) consists of a Gilbert cell mixer (T1-T6) and two emitter follower pairs (T9, T10 and T15, T16). In this architecture, the input signal is applied to the upper transistors ((T3-T6) while the feedback is applied to the lower transistor pair (T1-T2). The Gilbert

cell provides both modulation and amplification. The output is directly loaded with the load resistor R_L. The emitter follower stages provide level shifting, allowing the signal at the mixer output to be fed back to the input. Because of the inherent low-pass filter characteristic of the loop (the amplifier can be seen as an ideal amplifier cascaded with a low-pass filter), no additional filter is required . Therefore the monolithic integration level can be drastically improved. The design of an RFD was performed using the two available technologies (Atmel's SiGe2RF and IHP SG25H1, see Chapter 3). In order to reach optimum speed of operation, all transistors were biased at the optimum current density. However, like mentioned in [85], by using a different transistor size and biasing level, lower frequency of operation can be reached.

The main advantages of the dynamic frequency divider compared to the static architecture (see Section 8.5) are its lower power consumption (less transistors are required in the RFD) and its higher speed of operation. Indeed, the maximum operational frequency of the RFD is mostly limited by the cut-off frequency of the loop gain rather than the loop delay. The key figures of merit for RFD are $\frac{f_{max,op}}{P_{DC}}$ (where $f_{max,op}$ is the maximum frequency

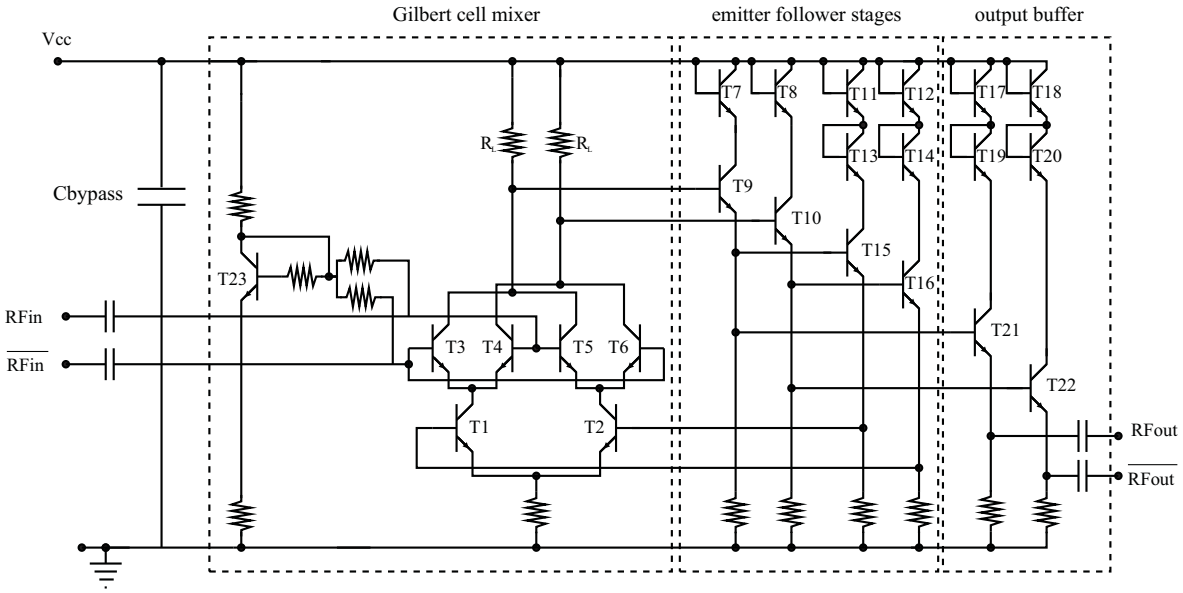

Fig. 8.3: Complete schematic of a regenerative frequency divider using bipolar transistors

of operation and P_{DC} the power dissipation), bandwidth of operation, sensitivity and integration level (die area). The main drawback of the dynamic frequency divider is its low operational bandwidth. The divider operates between cut-off frequency of the loop gain (for $f_{max,op}$) and the low-pass filter corner frequency (for $f_{min,op}$, where $f_{min,op}$ is the maximum frequency of operation) because once $3f_{in,op}/2$ is no longer filtered out, division is no more generated. Therefore, for standard dynamic frequency divider topology based on

the Gilbert cell mixer topology, the bandwidth is approximately $[\frac{f_{max,op}}{3};f_{max,op}]$. However, drastic improvement of the broadband performance as well as sensitivity can be obtained by adding a transimpedance amplifier (TIA) stage. In [86], it was demonstrated that the addition of the TIA decreases significantly time constants generated by the Miller capacitance and the collector response time and consequently increases the operation bandwidth of the IC (see [87], [88]). Moreover, because of the additional amplification, the sensitivity is further improved. The main drawback of the dynamic frequency divider with transimpedance topology is the necessary higher supply voltage (due to the added TIA stage) leading to a slightly higher power dissipation. The schematic of the dynamic frequency divider with transimpedance topology is depicted in Fig. 8.4. The complete

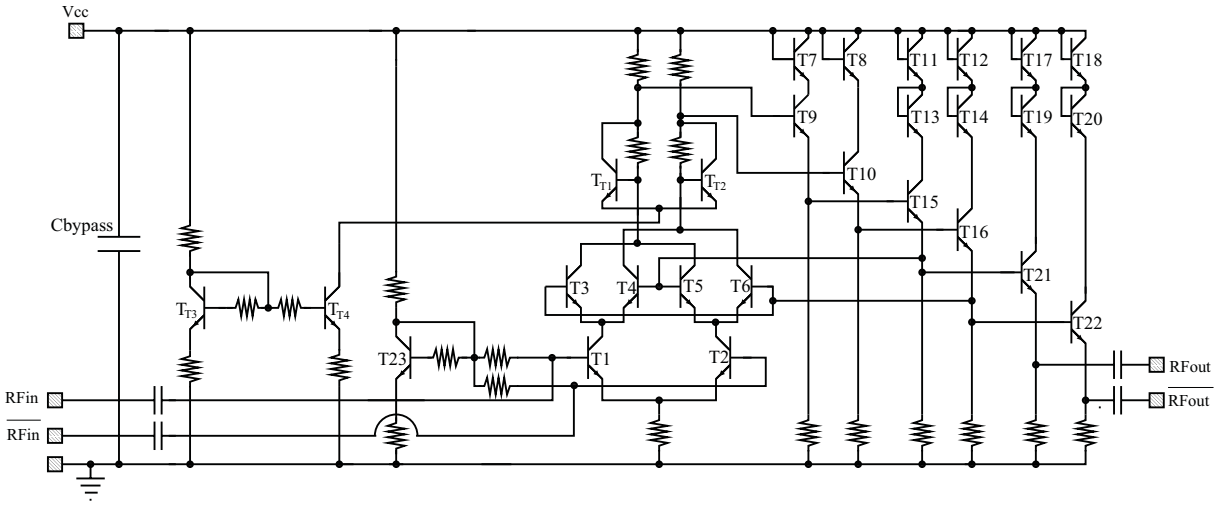

Fig. 8.4: Complete schematic of a regenerative frequency divider using bipolar transistors with transimpedance amplifier stage

dynamic frequency divider was simulated under Advanced Design System (ADS) from Agilent. As previously pointed out, each transistor was biased for optimum speed purpose (difficult procedure because of the complexity of the topology). After correct biasing of each element of the RFD, a time domain analysis was performed using the transient analysis tool.

8.3.2 Layout of the dynamic frequency dividers with transimpedance stage

The layout of ICs on a lossy silicon substrate is always a challenge. In the dynamic frequency divider design, the most critical elements are the interconnect of the feedback path. Because of its architecture, a long access line between the last emitter follower stage

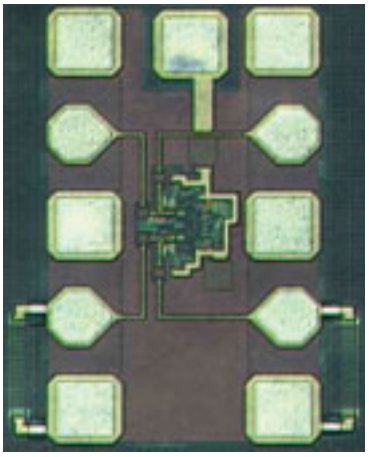

Fig. 8.5: Picture of the dynamic frequency divider with transimpedance topology using IHP's SiGe BiCMOS Technology (the size of this IC is 295 × 475 μm^2)

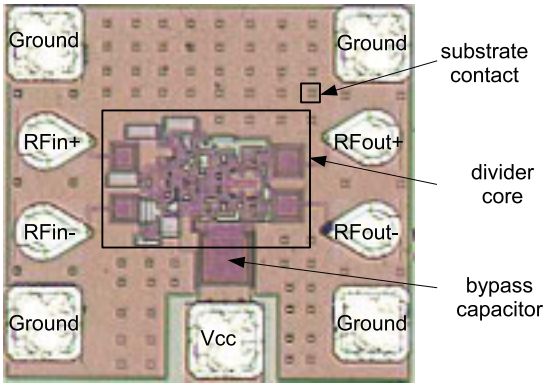

Fig. 8.6: Picture of the dynamic frequency divider with transimpedance topology using Atmel's SiGe2RF SiGe HBT Technology (435 × 400 μm^2)

(T_{15} and T_{16}) and the switching quad (T_3, T_4, T_5, T_6) is hardly avoidable. This leads to higher losses, lower loop gain and therefore lower sensitivity and bandwidth. Thus, it is essential to optimize the layout and reduce the interconnect length. The layouts of the dynamic frequency dividers with transimpedance stage are presented in Fig. 8.5 and Fig. 8.6. The ICs consume an area of 295 × 475 and 435 × 400 μm^2, respectively.

8.3.3 Characterization of the dynamic frequency dividers with transimpedance topology

Measurement of the dynamic frequency divider with transimpedance topology using Atmel's SiGe HBT technology

To measure differential ICs, the most usual technique is to connect half of the IC to 50 Ω terminations. A simulation has to be performed in order to reproduce the measurement conditions. The first step for the characterization of the RFD using Atmel's SiGe HBT technology is to measure the setup losses. Because the setup is symmetrical (see schematic shown in Fig. 8.7), it is reasonably assumed that each half of the measurement equipment contributes the same losses. Therefore, the overall losses are characterized and divided by two. An overview of the setup used to characterize the losses and the RFD is presented in Fig. 8.7 and Fig. 8.8, respectively. The Fig. 8.9 presents the measured sensitivity of the RFD, as well as the simulation of the IC when driven single-endedly and differentially. As can be seen, the RFD shows very good performance in term of sensitivity and bandwidth.

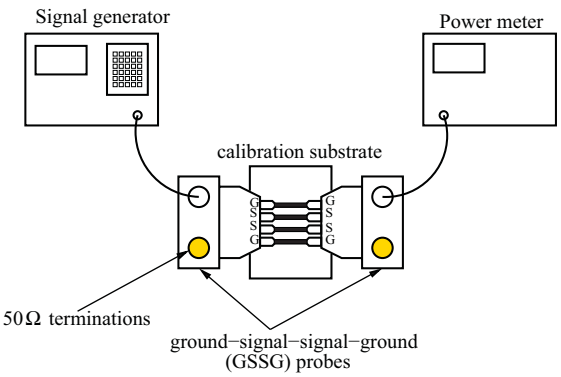

Fig. 8.7: Measurement of the setup losses for the characterization of the regenerative frequency divider using Atmel's SiGe HBT technology

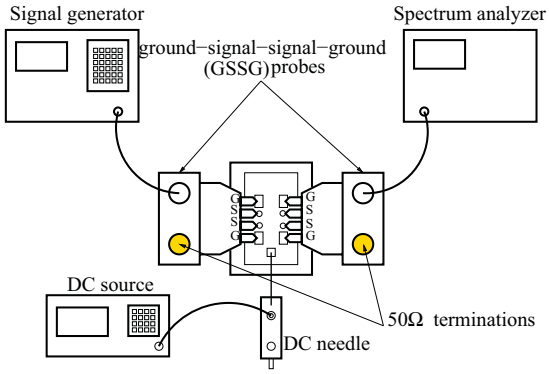

Fig. 8.8: On-chip characterization of the regenerative frequency divider using Atmel's SiGe HBT technology

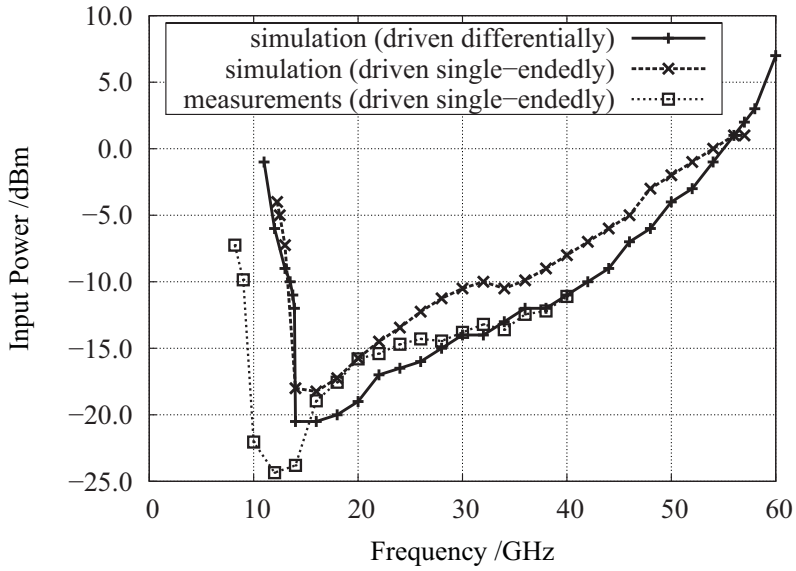

Fig. 8.9: Characterization of the regenerative frequency divider using Atmel's SiGe HBT technology

The measurements could only be performed up to 40 GHz. However, due to the good sensitivity of the IC at this frequency, the divider is expected to still operate beyond this point. The behavior of the IC in the time domain was also analyzed using a sampling oscilloscope. The output waveform of the RFD driven with a 40 GHz input signal is depicted in Fig. 8.10.

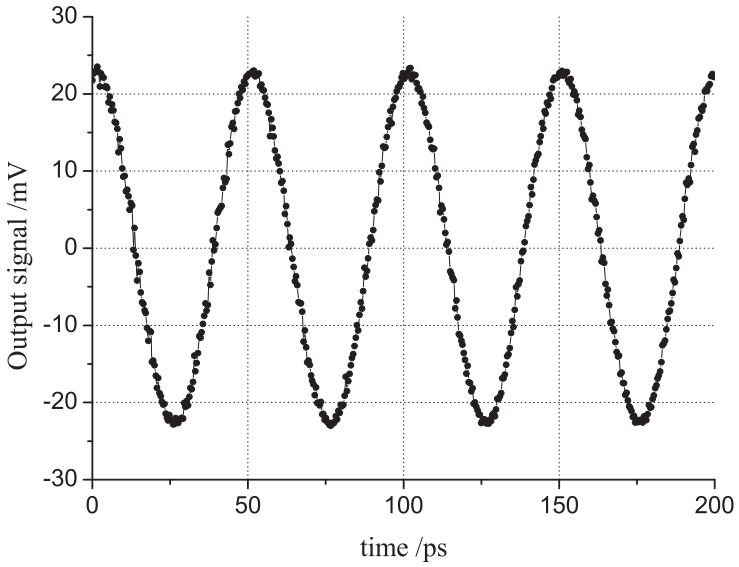

Fig. 8.10: Output waveform of the regenerative frequency divider in steady operation using Atmel's SiGe HBT technology. The applied input signal has a frequency of 40 GHz and a power of -4 dBm

Characterization of the mounted dynamic frequency divider with transimpedance topology using Atmel's SiGe HBT technology

To evaluate the performance of the divider once mounted, a test fixture was designed to characterize the regenerative frequency divider with transimpedance topology using Atmel's SiGe HBT technology. The measuring socket consists of a 254 μm thick RO4350B laminate with low permittivity (ε_r=3.48) fixed on a brass block. The chip is glued into a recess on this socket and then ultrasonically bonded. By this measure the chip surface is roughly at the same level as the access lines so that the bond wires are kept as short as possible. A photograph of the mounted IC and its test fixture is depicted in Fig. 8.11 and the resulting sensitivity for various bias points is presented in Fig. 8.12.

Measurement of the dynamic frequency divider with transimpedance topology using IHP's SiGe:C BiCMOS technology

One of the main issue of measurements beyond 50 GHz is the cost of the equipement. In order to facilitate the measurement of the RFD using IHP's SiGe:C BiCMOS technology, on-chip 50 Ω terminations were used. These elements were placed behind the bonding

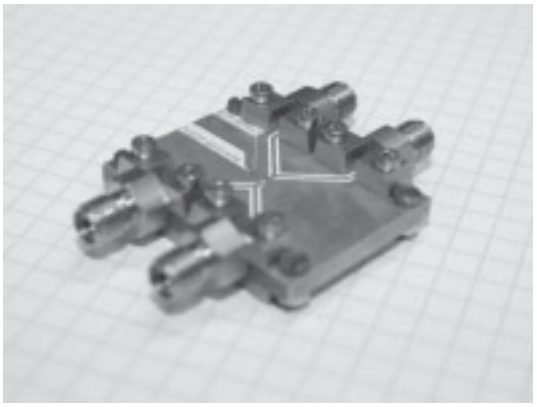

Fig. 8.11: Picture of the mounted frequency divider

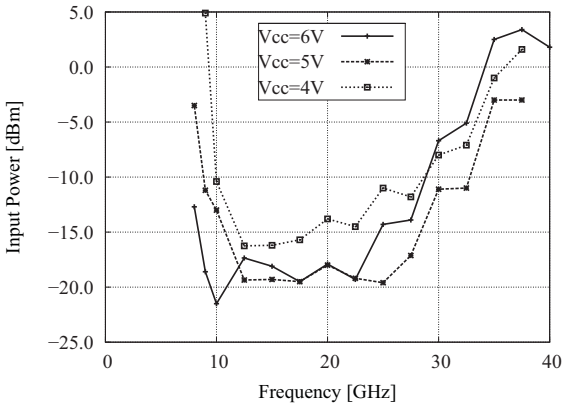

Fig. 8.12: Measured sensitivity of the mounted dynamic frequency divider with additional transimpedance amplifier stage for various biasing points

pads. Hence, they can easily be removed using focused ion beam (FIB), laser or ultrasonic manipulator to allow packaging of the ICs on an appropriate substrate after on-chip characterization. The influence of the implementation of the polysilicon resistors instead of external terminations was first simulated in order to anticipate possible problems engendered by the resistor parasitics. However, it was seen that the use of on-chip polysilicon resistors as 50 Ω terminations is uncritical. A passivation window was opened on the top of the interconnect lines to ease the separation of the on-chip termination from the bonding pads if mounting of the IC is required. The measurement procedure was divided into two steps:

- The dynamic frequency divider was measured in a first step up to 70 GHz. The signal is generated by the Agilent E8257D signal generator. This element is then connected to a 110 GHz GS 100 μm Picoprobe probe. The output signal was detected using the Agilent E2448A spectrum analyzer. As previously explained, using on-chip 50 Ω polysilicon resistors, single-ended probes can be used instead of differential ones. A description of the measurement setup of the frequency divider for up-to-V-band characterization is presented in Fig. 8.13.

- The measurements of the divider in the W band were performed using the Agilent E8257D signal source and the Millimeter Wave Source Module S10MS-AG to reach the 75 GHz-110 GHz region. A description of the measurement setup of the frequency divider for W-band characterization is presented in Fig. 8.14.

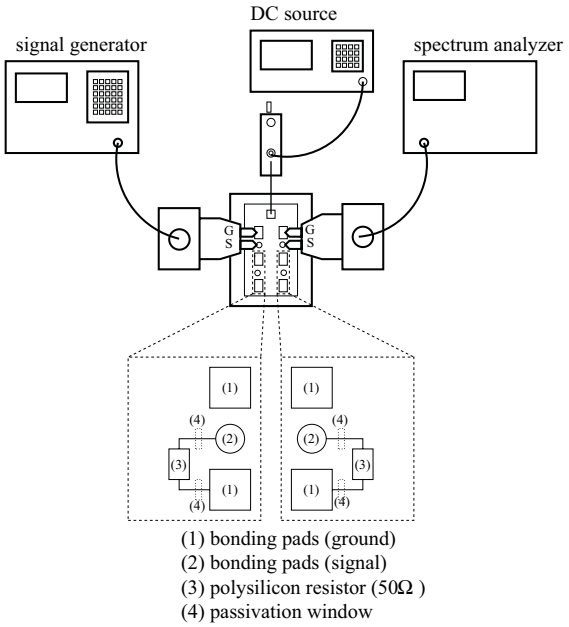

Fig. 8.13: Characterization of the regenerative frequency divider up to V-band using IHP's SiGe:C BiCMOS technology

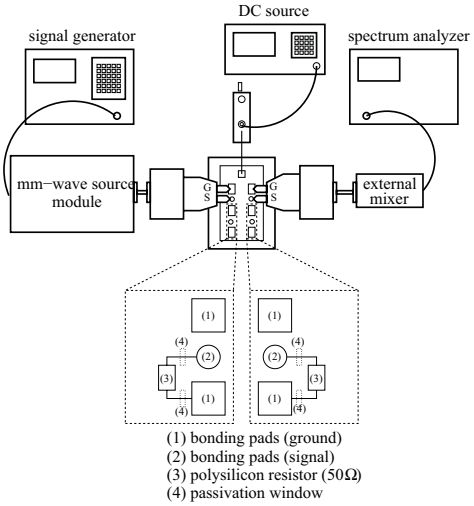

Fig. 8.14: W-band characterization of the regenerative frequency divider using IHP's SiGe:C BiCMOS technology

The most challenging step was the characterization of the losses of the setup. This is due to the fact that the setup could not be kept symmetrical. Therefore, the loss of each individual element used to characterize the IC was estimated individually. However, the resulting accuracy is acceptable and allows a good overview of the RFD performance. The resulting sensitivity is described in Fig. 8.15 for a supply voltage of 5 V (corresponding to a drawn current of 35 mA). Because this IC was designed for automotive applications, an interesting data is the sensitivity variation in a high temperature environment. This measurement was performed on-chip using a heatable chuck. The resulting performance of the IC is depicted in Fig. 8.16. Due to the complexity of the setup, this measurement was only performed in the W band. As seen, the frequency divider still operates in the full SRR/LRR bandwidth (76-81 GHz) also in such a critical environment.

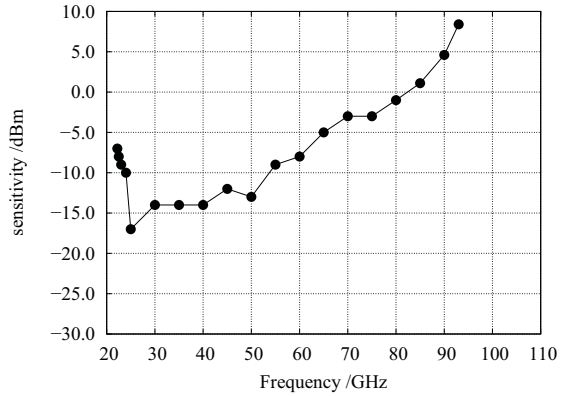

Fig. 8.15: Measured sensitivity of the dynamic frequency divider with additional transimpedance amplifier stage (SG25H1 technology)

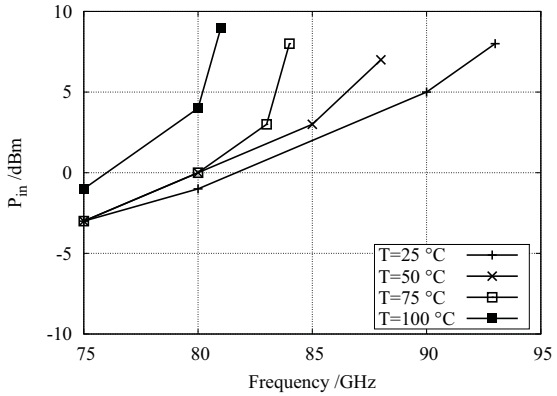

Fig. 8.16: Measured sensitivity over temperature of the dynamic frequency divider with additional transimpedance amplifier stage (SG25H1 technology)

8.4 Regenerative frequency divider design: Conclusion

In this section, two dynamic frequency dividers were presented. The first IC uses Atmel's SiGe HBT technology, the second was designed using IHP's SiGe:C BiCMOS technology. Both ICs use, as an addition to the standard topology, a transimpedance stage that significantly improves the sensitivity and broadband performance. A comparison with previously published dynamic frequency dividers is presented in Table 8.1.

	technology/f_T /GHz	[$f_{min,op}$-$f_{max,op}$] /GHz	P_{DC} /mW	$\frac{f_{max}}{P_{DC}}$	size /μm^2
[89]	0.12 μm SiGe bipolar	n.a.-100	285	0.35	n.a.
[90]	0.8 μm Si bipolar/40	n.a.-28	190	0.15	n.a.
[91]	0.25 μm SiGe bipolar/75	8-63	470	0.13	900×900
[92]	0.2 μm SiGe HBT/122	32-82.4	303	0.27	n.a.
[93]	0.25 μm SiGe HBT/80	26.6-79.2	1072.5	0.07	550×450
[94]	0.1 μm HEMT/220	86-108	360	0.29	1000×750
[95]	0.8 μm InP/InGaAs DHBT/245	n.a.-150	357	0.42	1500×1500
Atmel	0.8 μm SiGe HBT/80	8->40	175	> 0.22	435×400
IHP [96]	0.25 μm SiGe HBT/190	22-93	180	0.53	550×450

Tab. 8.1: Comparison between several published dynamic frequency dividers

8.5 Low power static frequency divider

The presented static frequency divider was not realized within the frame of this work. However, because it was integrated in a larger circuit, a small chapter is dedicated to this MMIC (a complete description of the designed static frequency divider can be found in [97]).

8.5.1 Theoretical approach

The analog frequency divider topology has theoretically a very high operational frequency. However, in order to divide the lower frequency range, the static frequency divider is often preferred due to its very good performance in terms of bandwidth. One possible topology is the Master-Slave Toggle Flip-Flop (MS-TFF) circuit, which has been used here. The MS-TFF presented here uses Atmel's SiGe2RF technology and consists of two D-latches, implemented in standard Emitter-Coupled-Logic (ECL). Instead of using two or more emitter follower stages between the two D-latches like widely used in the literature, only one emitter follower pair was used in order to reduce the supply voltage level. The smallest available transistor is optimal for high speed operation, for making up the upper-level current switching pairs. Therefore, a transistor with an emitter length of 1.4 μm has been chosen, resulting in low overall power consumption. A schematic describing the static frequency divider topology is presented in Fig. 8.17.

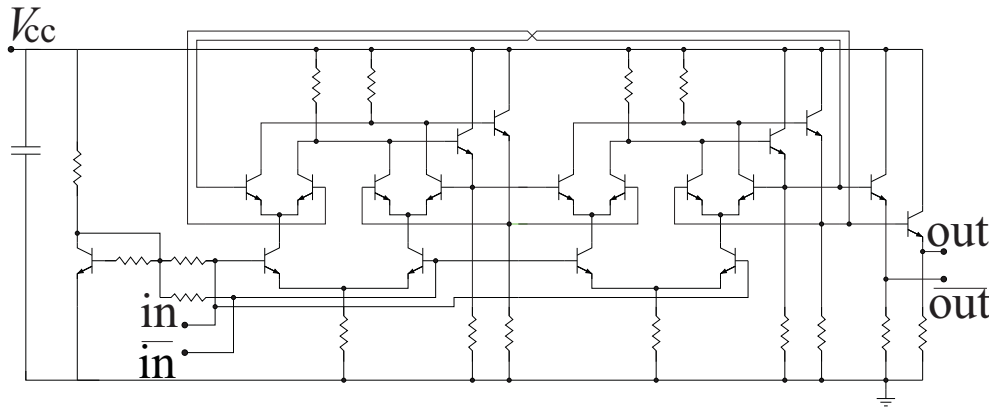

Fig. 8.17: Schematic of the static frequency divider using Atmel's SiGe2RF technology

8.5.2 Layout and characterization

A photograph of the static frequency divider chip is depicted in 8.18. The IC was measured

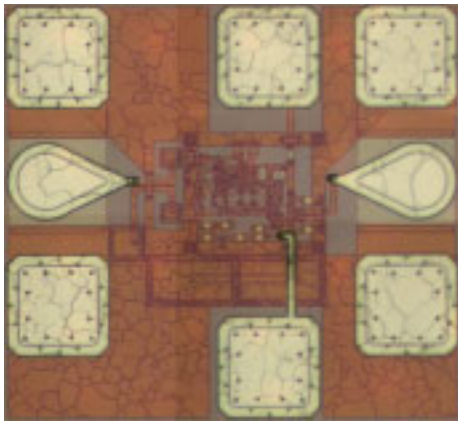

Fig. 8.18: Picture of the static frequency divider using Atmel's SiGe2RF technology (the chip size is 360 × 330 μm^2)

single-endedly in order to ease the characterization of the IC. This was mediated in the layout by connecting the complementary input port (RFin-) to ground via a capacitor. The inverted output port (RFout-) was left floating. The divider core itself has a chip-area of only 95 × 73 μm^2. The overall chip size is 360 × 330 μm^2, including the bonding pads. In [97], the divider was characterized at a supply voltage of 4 V. However, because the 32:1 frequency divider is intended to operate at 5 V, the sensitivity measurements of the static divider were performed with this given supply voltage level (which corresponds to a drawn current of 26 mA). The results are presented in Fig. 8.19.

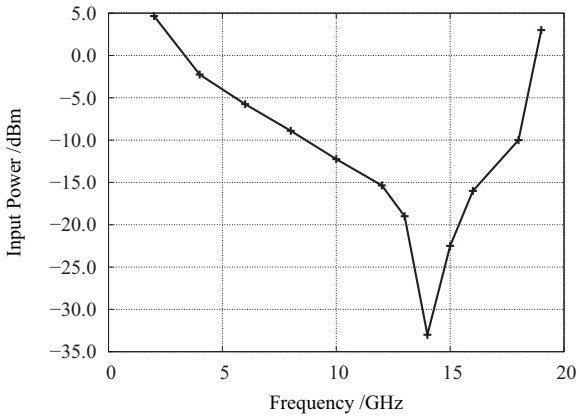

Fig. 8.19: Sensitivity measurements of the static frequency divider using Atmel's SiGe2RF technology at a supply voltage level of 5 V

8.6 32:1 frequency divider

8.6.1 Topology description

In order to obtain a frequency divider with high divide ratio, several dynamic and static frequency dividers were cascaded. The regenerative frequency divider was chosen for the first stages because of its higher frequency of operation. The static was used to divide the lower frequency domain.
Because fast phase/frequency detectors with maximum input frequencies up to 2 GHz are available products in the market, it was decided that an IC with a divide ratio of 32 was sufficient. This also allows a lower power consumption, which later could lead to an higher monolithic integration level.
Using Atmel's SiGe HBT technology (SiGe2RF), the topology was chosen as follows: The first two stages are using the previously described regenerative frequency divider while the remaining three stages use a static architecture [98]. A block diagram of the 32:1 frequency divider is depicted in Fig. 8.20. The chip photograph of the 32:1 frequency

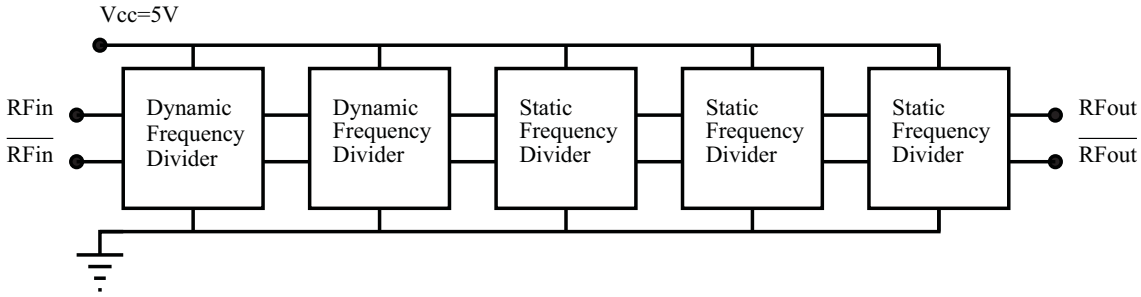

Fig. 8.20: Block diagram of the 32:1 frequency divider using Atmel's SiGe2RF technology

divider is presented in Fig. 8.21. The chip size is 1130 × 460 μm^2. The DC decoupling between each stage was performed using nitride capacitors. Their values are increasing with decreasing frequency in order to avoid influencing the RF performance of the IC.

8.6.2 Measurements of the 32:1 frequency divider

The measurements were performed on-chip using 100 μm GSSG probes. The IC consumes 150 mA at 5 V suppply voltage. As previously highlighted in 8.3.3, half of the circuit was connected to 50 Ω terminations in order to ease the measurement setup. The sensitivity of the differential frequency divider driven single-endedly is depicted in Fig. 8.22. The 32:1 frequency divider was also measured at a lower supply voltage in order to significantly reduce the power consumption of the divider. The circuit consumes 110 mA at 4 V supply

voltage. As can be seen, the IC operates at least over an octave (measurements beyond 40 GHz could not be performed) with very good sensitivity performance. The output of the divider was also measured by using a sampling oscilloscope. The measurements are presented in Fig.8.23.

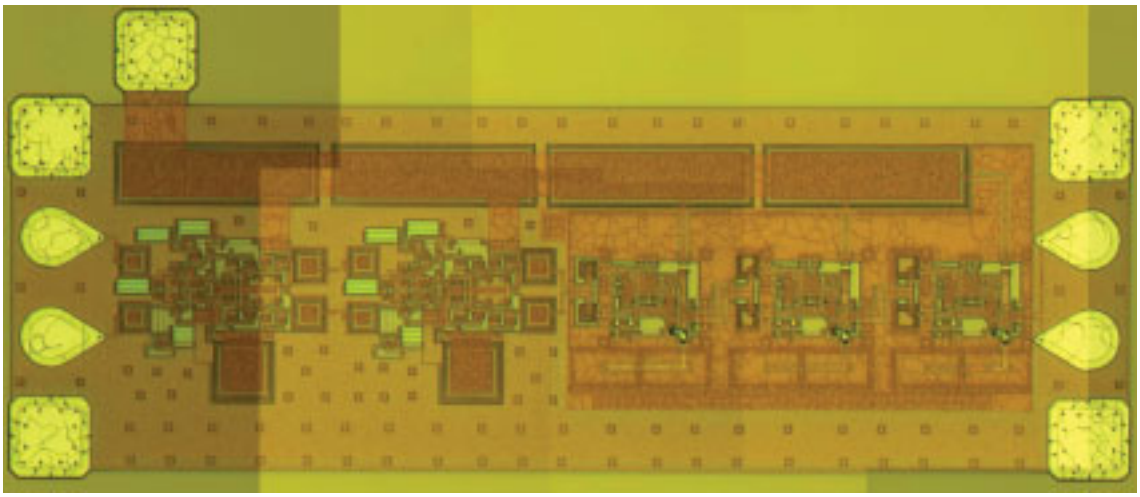

Fig. 8.21: Photo of the 32:1 frequency divider using Atmel's SiGe2RF technology ($1130 \times 460\ \mu m^2$)

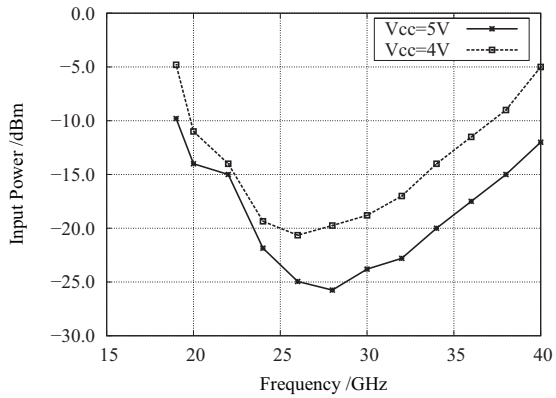

Fig. 8.22: Sensitivity measurements of the 32:1 frequency divider using Atmel's SiGe2RF technology in a 50 Ω test environment

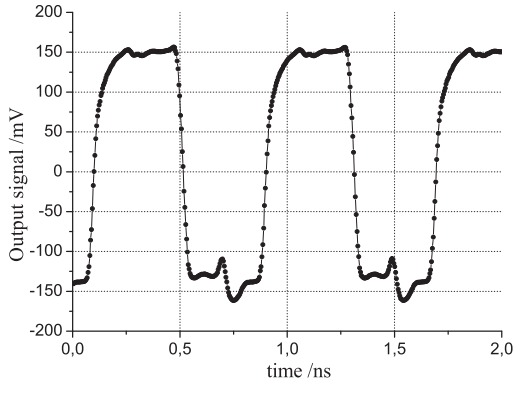

Fig. 8.23: Time domain measurement of the 32:1 frequency divider in steady operation using Atmel's SiGe2RF technology with an input signal of -10 dBm at 40 GHz

8.7 Conclusion

In this chapter, a wide overview of successfully designed frequency dividers was presented. The two major topologies (static and dynamic) were utilized. The dynamic divider was used to operate at the highest possible frequencies while the static approach was utilized to divide the lower frequency domain. For the dynamic frequency divider, a transimpedance amplifier was added to the standard topology to drastically improve the broadband performance as well as sensitivity. The static frequency divider was designed with low power consumption as the main goal. Using IHP's BiCMOS technology, a state of the art IC was obtained, reaching very good performance such as wide operational bandwidth, high maximum frequency of operation and low power consumption on a compact die area. Using Atmel's SiGe bipolar technology, a 32:1 frequency divider combining the advantages of the dynamic and static topology was obtained. The IC reaches record $f_{max,op}$ for a 0.8 μm SiGe HBT technology. The chosen values and parameters of each element of the dynamic dividers using Atmel's and IHP's technologies are depicted in Appendix F. An overview of the performance of the previously presented dividers is presented in table 8.2.

Topology	dynamic	dynamic	static	dynamic/static
Technology	IHP	ATMEL	ATMEL	ATMEL
Divide ratio	2	2	2	32
Icc /mA	35	36	26	150/110
Vcc /V	5	5	5	5/4
$f_{min,op}$-$f_{max,op}$ /GHz	22-93	8-40*	2-19	19-40*
$f_{max,op}/P_{DC}$	0.53	0.22	0.15	0.05/0.09
Layout size /μm^2	295 × 475	435 × 400	360 × 330	1130 × 460

Tab. 8.2: Performance overview of the designed frequency dividers (*: Limited by the measurement equipment)

Chapter 9

Conclusion and Outlook

In this work, the possibility to realize high performance millimeter-wave integrated circuits using silicon bipolar technologies with transit frequency less than three times higher than the operational frequency of the developed circuits was investigated. Additionally, in order to reduce the overall cost of the ICs, a re-use approach was studied on a wide range of ICs to be implemented in different applications. These studies were performed by using two different technologies (Atmel's SiGe2RF was used for frequencies below 50 GHz and IHP's SG25H1 was used for IC design targeting the 77-81 GHz automotive radar application).

The first step in order to initiate reliable simulations was to achieve an accurate modeling of the passive elements which are the foundation of the design core. This was performed using a scalable model for the thin-film microstrip lines and a library of lumped elements which were formerly characterized on-wafer and deembedded subsequently.

Several approaches were investigated in order to realize good millimeter-wave amplifier ICs. The first topology was based on a single-ended LNA using lumped elements. Three cascaded stages based on a cascode configuration were used to achieve high gain, good matching and high reverse isolation performance on a single and highly compact IC. Once the first LNA (operating at 35 GHz) was successfully characterized, by keeping the elementary cell (biasing, transistor size, layout) unchanged and performing slight modifications on the reactive elements, the center frequency of this IC was shifted to much higher frequencies.

Even if this approach brought very good results on-wafer, the packaging of single-ended ICs is always challenging when reaching the millimeter-wave domain. To overcome this issue, differential LNAs were studied. These ICs were designed using Atmel's low-cost technology and IHP's BiCMOS technology for 77-81 GHz SRR applications. As for the previously mentioned LNAs, multi-stage cascode topology had to be provided to reach

high gain and improve the isolation. To offer a more flexible layout solution, thin-film microstrip lines were utilized. Even on a lossy silicon substrate, these LNAs achieved very good performance. As for the lumped elements based LNAs, the LNAs were designed with a re-use approach. By shortening the TFMSLs, a wide shift of the operational frequency was successfully obtained.

To design the VCOs, several topologies using a common VCO core architecture and different buffer amplifiers were emphasized. The VCO core is of the negative resistance type and implement an efficient phase noise reduction technique. Two types of output buffer were presented: A low-power compact common-base approach and a cascode topology with high output power. The VCO with common-base output buffer achieved low-power consumption, reasonable output power and very low phase noise on a very compact die area. The VCO with cascode output stage resulted in a high output power with low phase noise performance. As for the LNAs, the measured VCOs successfully operate beyond one third of the transistor f_T. By modifying the passive elements as well as the varactor configuration, a shift in frequency was possible, therefore proving the possibility of design re-use.

A millimeter-wave down-converter mixer was also designed. Because this IC had to be useful for an extremely wide spectral region, no narrow-band matching was provided. The designed mixer is based on a Gilbert-cell mixer topology and achieved very reasonable conversion gain and highly symmetrical differential output voltage. Because only one reactive element was included in the design, the layout is highly compact. This very broadband mixer showed good performance even if used beyond $f_T/3$.

Finally, the design of wideband frequency dividers was investigated. Two major topologies were studied, the dynamic frequency divider (also called analog or regenerative) and the static frequency divider (also called digital). The dynamic frequency divider was used for the first stages to divide the high frequencies. In order to improve the sensitivity and broadband operation, a differential transimpedance stage was implemented. This addition is rarely presented in other published IC designs. By using such approach, the fabricated frequency dividers show very good performance. The static frequency dividers were designed to divide the low frequencies. By cascading dynamic and static dividers, a high ratio high sensitivity broadband frequency divider operating far beyond $f_T/3$ was characterized. Because of the wideband performance of the dividers, these ICs can be used for applications operating at different frequency ranges, therefore showing the design re-use capability.

In conclusion, the possibility to design integrated circuits operating beyond one third of the technology f_T with very good performance was fully proved and the design re-use capability of the proposed topologies was demonstrated. In the future, in order to further

improve the overall performance, fully integrated systems might be developed. Such approach will allow the suppression of most of the critical pads and will result in a low-cost high performance millimeter-wave front-end.

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List of Acronyms and Symbols

A	Ampere
AC	Alternating current
ACC	Automotive Cruise Control
ADC	Analog Digital Converter
ADS	Advanced Design System
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BV_{CEo}	Collector-emitter breakdown voltage
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical mechanical planarization or polishing
CPW	Coplanar Waveguide
dB	Decibel
DC	Direct current
DSP	Digital Signal Processing
DUT	Device Under Test
EM	Electromagnetic
f_m	Offset frequency
f_{max}	Maximum frequency of oscillation
FMCW	Frequency Modulated Continuous Wave
f_o	Center frequency
f_{op}	Operational frequency
f_{osc}	Oscillation frequency
f_T	Transit frequency
GaAs	Gallium-Arsenide
Ge	Germanium
GHz	Giga Hertz
GSG	Ground-Signal-Ground
GSGSG	Ground-Signal-Ground-Signal-Ground
GSSG	Ground-Signal-Ground
HBT	Heterojunction Bipolar Transistor

HDTV	High Definition Television
HEMT	High Electron Mobility Transistor
HiCUM	High Current Model
IC	Integrated Circuit
IF	Intermediate Frequency
LMDS	Local Multipoint Distribution Service
LNA	Low Noise Amplifier
LO	Local Oscillator
LOCOS	Local Oxidation of Silicon
LRR	Long Range Radar
mm-wave	Millimeter Wave
MIM	Metal-Insulator-Metal
MHz	Mega Hertz
MMIC	Monolithic Microwave Integrated Circuit
MOS	Metal-Oxide-Semiconductor
NF	Noise Figure
NF_{min}	Minimum noise figure
$P_{1dB,in}$	Input Referred 1 dB compression point
$P_{1dB,out}$	Output Referred 1 dB compression point
P_{DC}	Power dissipation
PLL	Phase Locked Loop
RF	Radio frequency
RFD	Regenerative Frequency Divider
RFIC	Radio frequency Integrated Circuit
SAW	Surface Acoustic Wave
SHR	Super Heterodyne Receiver
Si	Silicon
SIC	Selectively Implanted Collector
SiGe	Silicon Germanium
SiP	System in Package
SoC	System on Chip
S-parameters	Scattering parameters
SRR	Short Range Radar
STI	Shallow Trench Isolation
T	Temperature
TFMSL	Thin-Film Microstrip Line
TIA	Transimpedance Amplifier

UWB	Ultra Wide Band
V	Volt
VBIC	Vertical Bipolar Intercompany Model
VCO	Voltage Controlled Oscillator
V.G.	Virtual Ground
W	Watt

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Appendix A

Chip Photos of the Amplifiers

This appendix provides chip photos of the singled-ended amplifiers based on lumped-elements designed using Atmel's SiGe HBT technology.

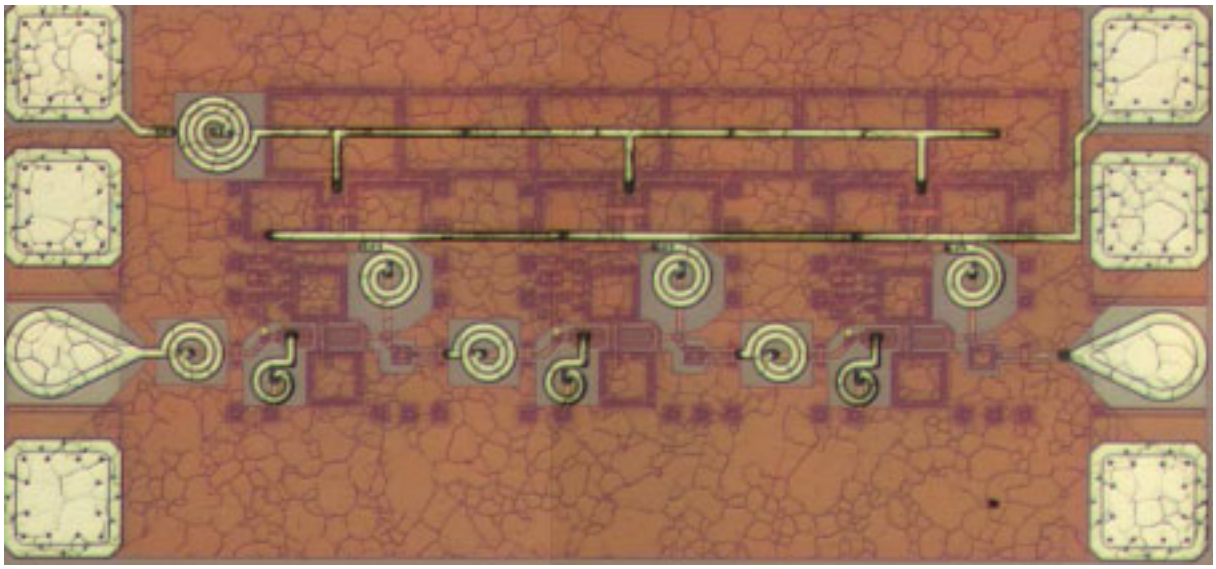


Fig. A.1: Chip photo of the 35 GHz Low Noise Amplifier (823 × 380 μm^2)

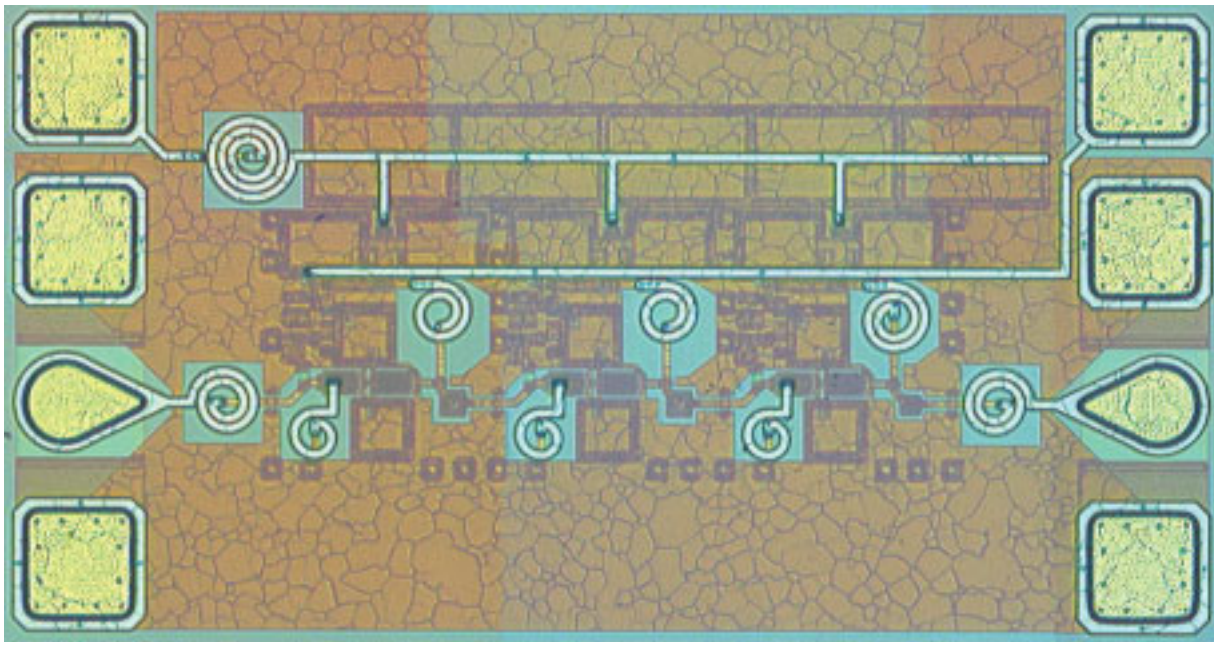


Fig. A.2: Chip photo of the 39 GHz Low Noise Amplifier (735 × 380 μm^2)

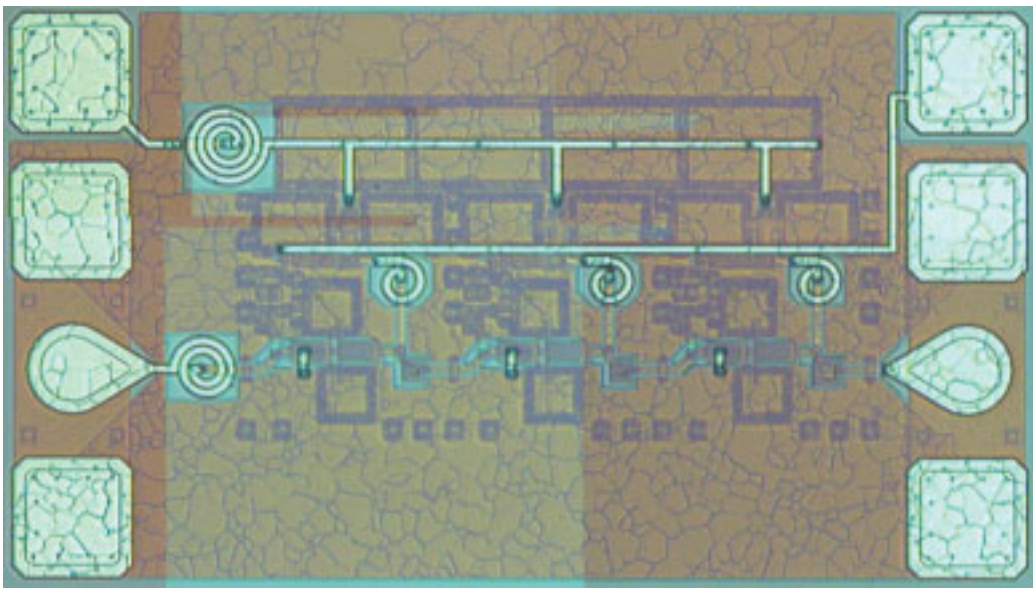


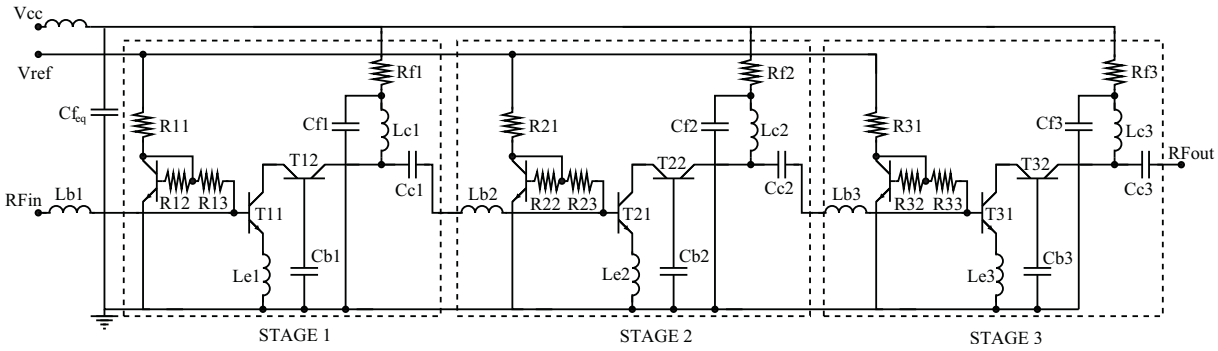
Fig. A.3: Chip photo of the Low Noise Amplifier (680 × 380 μm^2)

Appendix B

Millimeter-Wave Amplifiers

In this appendix, the values and parameters of every component used to design the single-ended 35 GHz amplifier (SiGe2RF), the differential 40 GHz amplifier (SiGe2RF) and the 79 GHz amplifier (IHP) are presented. Because of the similarity between the single-ended 35 GHz LNA and the other designed single-ended amplifiers, the latest are not described here. Because the 58 GHz, 63 GHz and 70 GHz differential amplifiers were obtained simply by increasing the length of the TFMSLs of the 79 GHz LNA, they are also not presented. For the transistors parameters: ***Config.***: Configuration of the contacts (***B***: base, ***E***: emitter, ***C***: collector), ***E.L.***: Emitter length, ***E.W.***: Emitter width. For the inductors parameters: 1/4 ***turns***: Amount of quarter turns of the spiral inductors, ***w***: width, ***s***: spacing between the metal lines, ***ri***: inner radius.

35 GHz single-ended amplifier (Atmel SiGe2RF)

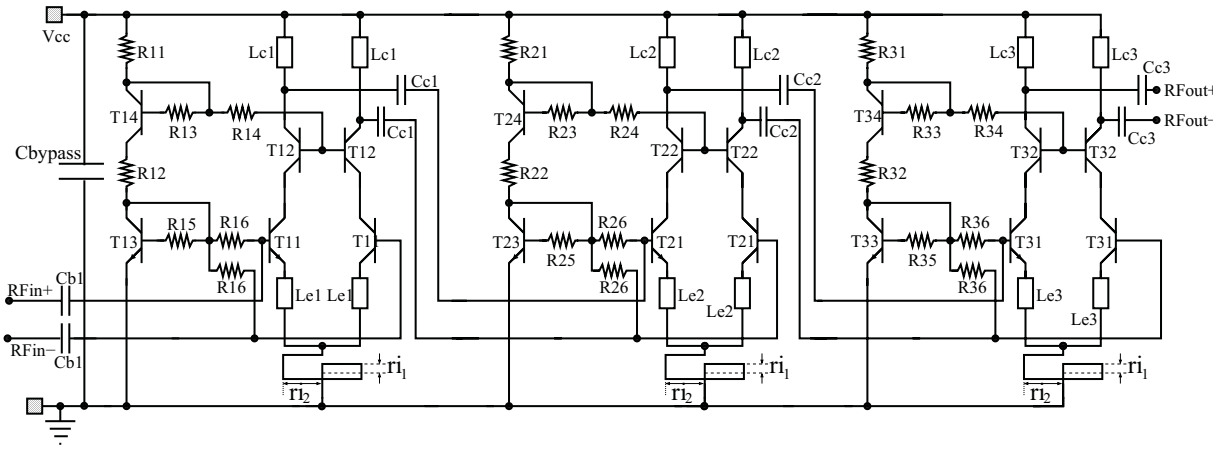


1^{st} stage				
Resistor	Value			
R_{11}	1000 Ω			
R_{12}	4000 Ω			
R_{13}	1000 Ω			
R_{f1}	15 Ω			
Transistor	Config.		E.L.	E.W.
T_{11}	CBEBC		20 μm	0.5 μm
T_{12}	CBEBC		20 μm	0.5 μm
T_{b1}	CBEBC		10 μm	0.5 μm
Capacitor	Value			
C_{c1}	40 fF			
C_{f1}	2 x 1.7 pF			
C_{feq}	30 pF			
Inductor	1/4 turns	w	s	ri
L_{b1}	8	4 μm	2 μm	10 μm
L_{e1}	4	4 μm	2 μm	10 μm
L_{c1}	8	4 μm	2 μm	10 μm

2^{nd} stage				
Resistor	Value			
R_{21}	1000 Ω			
R_{22}	4000 Ω			
R_{23}	1000 Ω			
R_{f2}	15 Ω			
Transistor	Config.		E.L.	E.W.
T_{21}	CBEBC		20 μm	0.5 μm
T_{22}	CBEBC		20 μm	0.5 μm
T_{b2}	CBEBC		10 μm	0.5 μm
Capacitor	Value			
C_{c2}	40 fF			
C_{f2}	2 x 1.7 pF			
Inductor	1/4 turns	w	s	ri
L_{b2}	8	4 μm	2 μm	10 μm
L_{e2}	4	4 μm	2 μm	10 μm
L_{c2}	8	4 μm	2 μm	10 μm

3^{rd} stage				
Resistor	Value			
R_{31}	700 Ω			
R_{32}	4000 Ω			
R_{33}	1000 Ω			
R_{f3}	15 Ω			
Transistor	Config.	E.L.	E.W.	
T_{31}	CBEBC	20 μm	0.5 μm	
T_{32}	CBEBC	20 μm	0.5 μm	
T_{b3}	CBEBC	10 μm	0.5 μm	
Capacitor	Value			
C_{c3}	40 fF			
C_{f3}	2 x 1.7 pF			
Inductor	1/4 turns	w	s	ri
L_{b3}	8	4 μm	2 μm	10 μm
L_{e3}	4	4 μm	2 μm	10 μm
L_{c3}	8	4 μm	2 μm	10 μm

40 GHz differential amplifier (Atmel SiGe2RF)

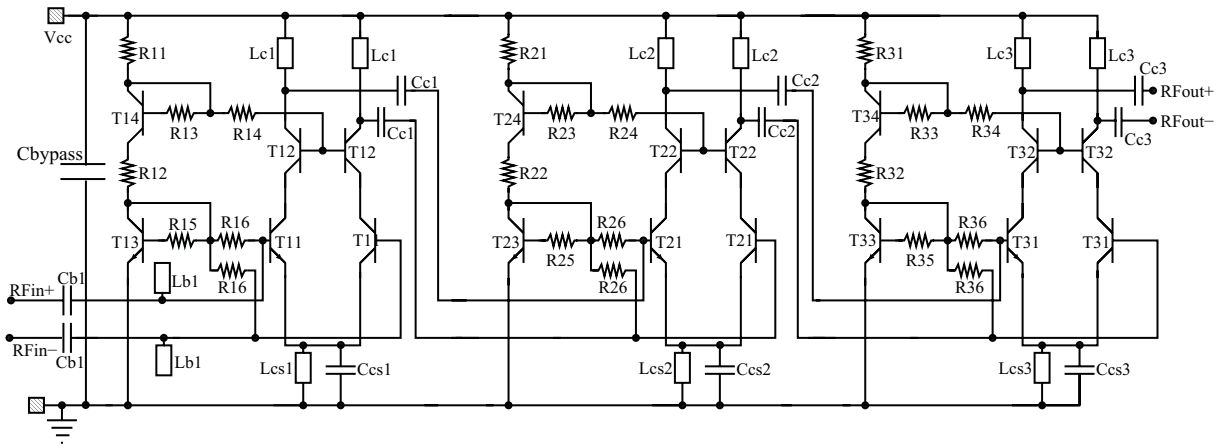


1^{st} stage				
Resistor	Value			
R_{11}	260 Ω			
R_{12}	295 Ω			
R_{13}	2000 Ω			
R_{14}	2000 Ω			
R_{15}	2000 Ω			
R_{16}	1000 Ω			
Transistor	Config.		E.L.	E.W.
T_{11}	CBEB		10 μm	0.5 μm
T_{12}	CBEB		10 μm	0.5 μm
T_{13}	CBEB		10 μm	0.5 μm
T_{14}	CBEB		10 μm	0.5 μm
Capacitor	Value			
C_{b1}	120 pF			
C_{c1}	50 pF			
$C_{bypass_{eq}}$	25 pF			
TFMSL	Width		Length	
L_{c1}	3 μm		400 μm	
L_{e1}	3 μm		200 μm	
Inductor	1/4 t.	w	s	$ri_{1/2}$
		in μm		
L_{cs1}	8	3	3	3/30

2^{nd} stage				
Resistor	Value			
R_{11}	140 Ω			
R_{12}	275 Ω			
R_{13}	2000 Ω			
R_{14}	2000 Ω			
R_{15}	2000 Ω			
R_{16}	1000 Ω			
Transistor	Config.		E.L.	E.W.
T_{11}	CBEB		10 μm	0.5 μm
T_{12}	CBEB		10 μm	0.5 μm
T_{13}	CBEB		10 μm	0.5 μm
T_{14}	CBEB		10 μm	0.5 μm
Capacitor	Value			
C_{c1}	50 pF			
TFMSL	Width		Length	
L_{c1}	3 μm		400 μm	
L_{e1}	3 μm		200 μm	
Inductor	1/4 t.	w	s	$ri_{1/2}$
		in μm		
L_{cs1}	8	3	3	3/30

3^{rd} stage			
Resistor	Value		
R_{11}	140 Ω		
R_{12}	275 Ω		
R_{13}	2000 Ω		
R_{14}	2000 Ω		
R_{15}	2000 Ω		
R_{16}	1000 Ω		
Transistor	Config.	E.L.	E.W.
T_{11}	CBEB	10 μm	0.5 μm
T_{12}	CBEB	10 μm	0.5 μm
T_{13}	CBEB	10 μm	0.5 μm
T_{14}	CBEB	10 μm	0.5 μm
Capacitor	Value		
C_{c1}	50 pF		
TFMSL	Width	Length	
L_{c1}	3 μm	400 μm	
L_{e1}	3 μm	200 μm	
Inductor	1/4 t.	w	s	$ri_{1/2}$
		in μm		
L_{cs1}	8	3	3	3/30

79 GHz differential amplifier (IHP SG25H1)



1^{st} stage			
Resistor	Value		
R_{11}	600 Ω		
R_{12}	150 Ω		
R_{13}	4k Ω		
R_{14}	1k Ω		
R_{15}	4k Ω		
R_{16}	1k Ω		
Transistor	Cell N°	E.L.	E.W.
T_{11}	4	0.84 μm	0.25 μm
T_{12}	4	0.84 μm	0.25 μm
T_{13}	1	0.84 μm	0.25 μm
T_{14}	1	0.84 μm	0.25 μm
Capacitor	Value		
C_{b1}	1 pF		
C_{c1}	18.5 fF		
C_{cs1}	100 fF		
C_{bypass}	8 pF		
TFMSL	Width	Length	
L_{b1}	2 μm	175 μm	
L_{c1}	2 μm	230 μm	
L_{cs1}	2 μm	40 μm	

2^{nd} stage			
Resistor	Value		
R_{21}	600 Ω		
R_{22}	150 Ω		
R_{23}	4k Ω		
R_{24}	1k Ω		
R_{25}	4k Ω		
R_{26}	1k Ω		
Transistor	Cell N°	E.L.	E.W.
T_{21}	4	0.84 μm	0.25 μm
T_{22}	4	0.84 μm	0.25 μm
T_{23}	1	0.84 μm	0.25 μm
T_{24}	1	0.84 μm	0.25 μm
Capacitor	Value		
C_{c2}	17 fF		
C_{cs2}	100 fF		
Inductor	Width	Length	
L_{c2}	2 μm	230 μm	
L_{cs2}	2 μm	40 μm	

3^{rd} stage			
Resistor	Value		
R_{31}	350 Ω		
R_{32}	90 Ω		
R_{33}	4k Ω		
R_{34}	1k Ω		
R_{35}	4k Ω		
R_{36}	1k Ω		
Transistor	Config.	E.L.	E.W.
T_{31}	4	0.84 μm	0.25 μm
T_{32}	4	0.84 μm	0.25 μm
T_{33}	1	0.84 μm	0.25 μm
T_{34}	1	0.84 μm	0.25 μm
Capacitor	Value		
C_{c3}	38 fF		
C_{cs}	100 fF		
Inductor	Width	Length	
L_{c3}	2 μm	190 μm	
L_{cs3}	2 μm	40 μm	

Appendix C

Chip Photos of the VCOs

In this section, the chip photos of all the designed VCOs are depicted. The VCOs with common-base output buffer are first presented, then the oscillators with cascode output buffer is showed.

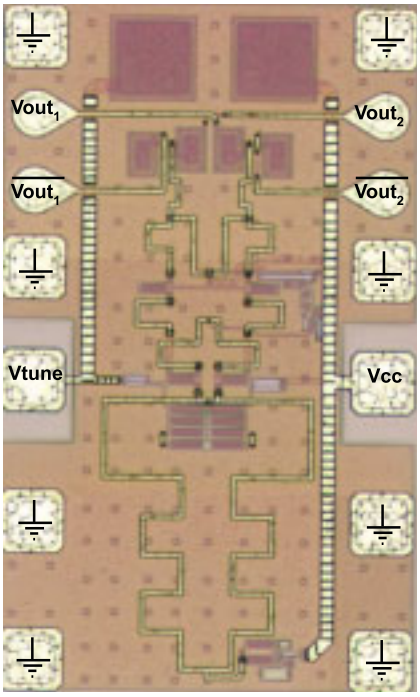


Fig. C.1: Chip photo of the voltage controlled oscillator with differential common-base output buffer (1^{st} version). The chip size is 865 $\times$ 565 μm^2

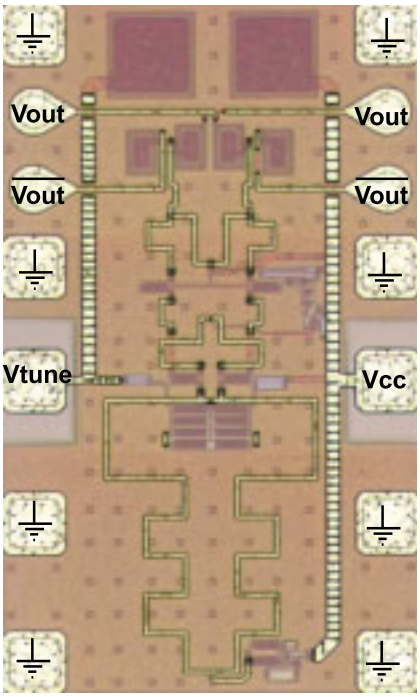


Fig. C.2: Chip photo of the voltage controlled oscillator with differential common-base output buffer (2^{nd} version). The chip size is 865×565 μm^2

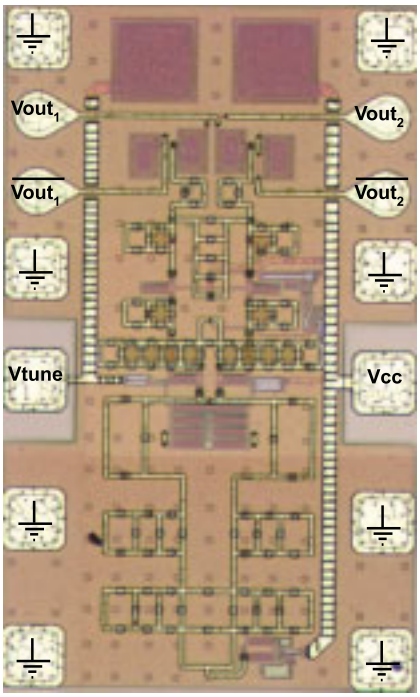


Fig. C.3: Chip photo of the voltage controlled oscillator with differential common-base output buffer (version designed with trimmable line technique). The chip size is $865 \times 565\ \mu m^2$

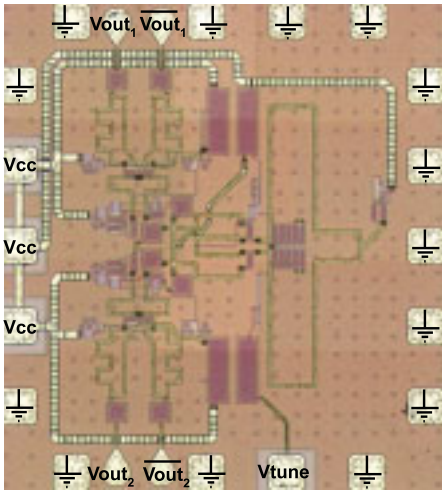


Fig. C.4: Chip photo of the voltage controlled oscillator with differential cascode output buffer (1^{st} version). The chip size is $890 \times 1100\ \mu m^2$

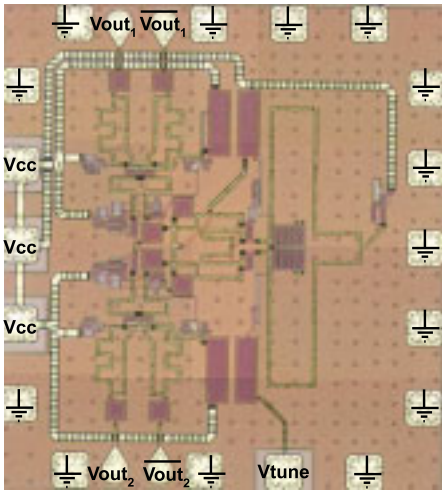


Fig. C.5: Chip photo of the voltage controlled oscillator with differential cascode output buffer (2^{nd} version). The chip size is 890 $\times$ 1100 μm^2

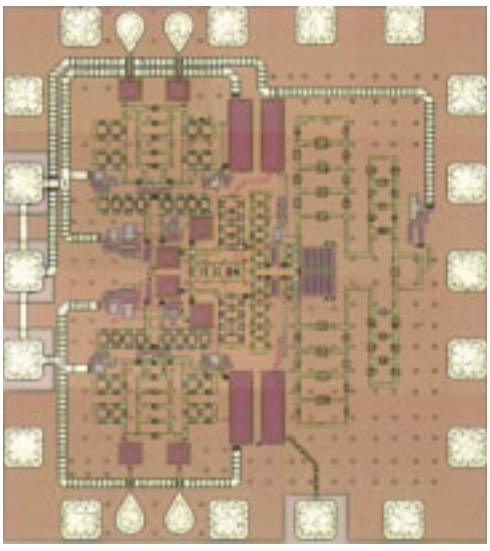
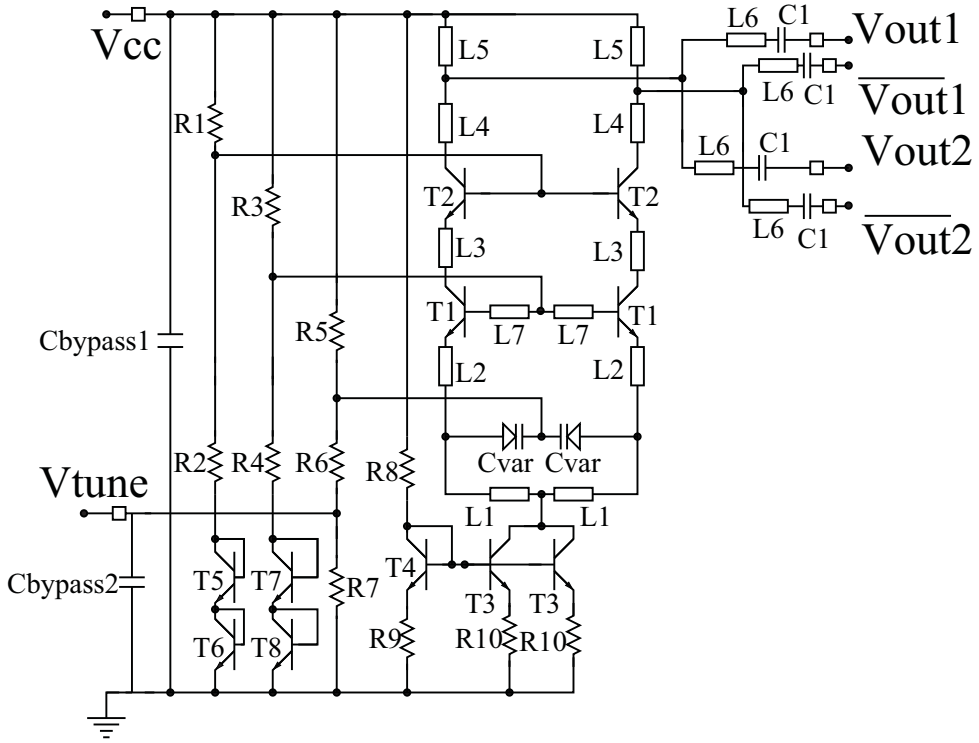


Fig. C.6: Chip photo of the voltage controlled oscillator with differential cascode output buffer (version with trimmable line technique). The chip size is 890 $\times$ 1100 μm^2

Appendix D

Millimeter-Wave VCOs

This section gives an overview of the values and parameters which were utilized to design the VCOs with common-base output buffer and cascode output buffer. Only the first versions described in chapter 6 are presented here. For the transistors parameters: ***Config.***: Configuration of the contacts (***B***: base, ***E***: emitter, ***C***: collector), ***E.L.***: Emitter length, ***E.W.***: Emitter width.



VCO core				
Transistor	Config.	Finger Number	E.L.	E.W.
T_1	CBEB	1	30 μm	0.5 μm
C_{var}	CBEB (non-SIC)	4	40 μm	0.5 μm

TFMSL	Width	Length
L1	3 μm	800 μm
L2	3 μm	40 μm
L7	3 μm	170 μm

Capacitor	Value
$C_{bypass2}$	10 pF

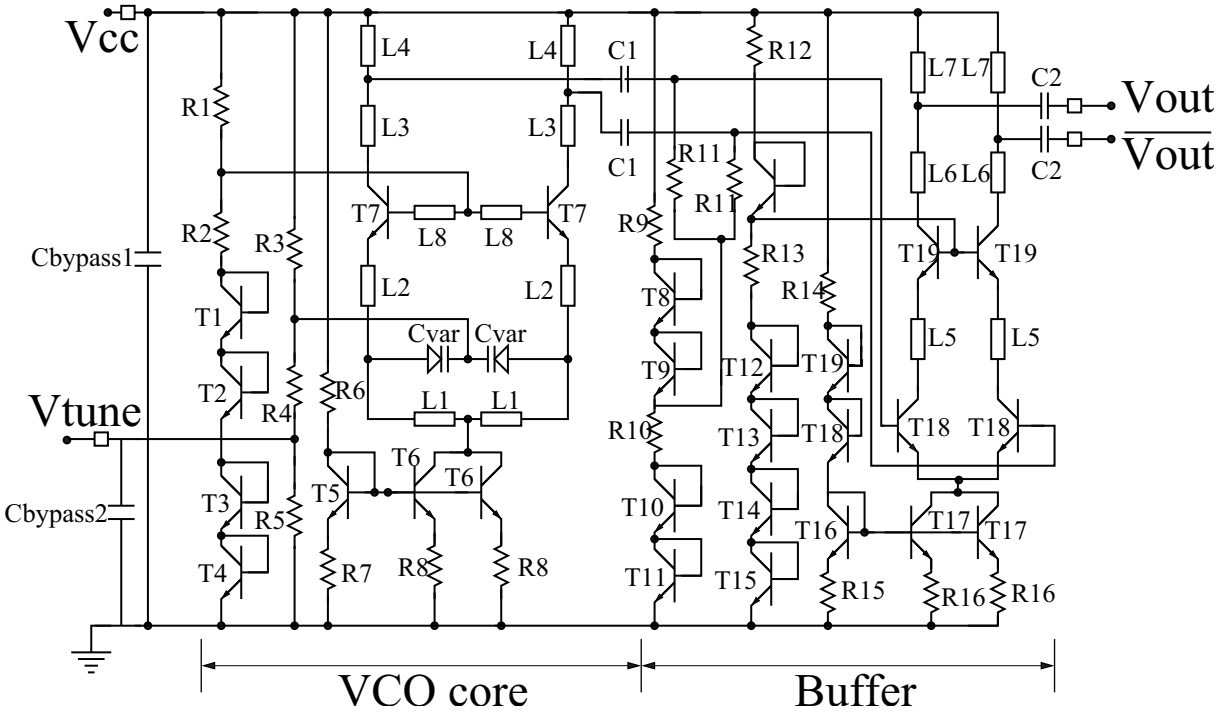
Output buffer			
Transistor	Config.	E.L.	E.W.
T_2	CBEB	30 μm	0.5 μm

TFMSL	Width	Length
L3	3 μm	110 μm
L4	3 μm	130 μm
L5	3 μm	110 μm
L6	3 μm	200 μm

Capacitor	Value
C_1	0.5 pF
$C_{bypass1}$	10 pF

Biasing network	
Resistor	Value
R_1	600 Ω
R_2	620 Ω
R_3	980 Ω
R_4	1k Ω
R_5	4k Ω
R_6	1k Ω
R_7	10k Ω
R_8	850 Ω
R_9	126 Ω
R_{10}	21 Ω

Transistor	Config.	E.L.	E.W.
T_3	CBEB	30 μm	0.5 μm
T_4	CBEB	5 μm	0.5 μm
T_5	CBEB	5 μm	0.5 μm
T_6	CBEB	5 μm	0.5 μm
T_7	CBEB	5 μm	0.5 μm
T_8	CBEB	5 μm	0.5 μm



VCO core			
Transistor	Config.	E.L.	E.W.
T_7	CBEB	30 μm	0.5 μm
C_{var}	5 x CBEB	40 μm	0.5 μm
TFMSL	Width	Length	
L1	3 μm	800 μm	
L2	3 μm	40 μm	
L3	3 μm	200 μm	
L4	3 μm	200 μm	
L8	3 μm	120 μm	
Capacitor	Value		
C_1	0.5 pF		
$C_{bypass1}$	5 pF		

Biasing network (VCO)			
Resistor	Value		
R_1	290 Ω		
R_2	660 Ω		
R_3	2.4k Ω		
R_4	2.6k Ω		
R_5	10k Ω		
R_6	650 Ω		
R_7	372 Ω		
R_8	62 Ω		
Transistor	Config.	E.L.	E.W.
T_1	CBEB	5 μm	0.5 μm
T_2	CBEB	5 μm	0.5 μm
T_3	CBEB	5 μm	0.5 μm
T_4	CBEB	5 μm	0.5 μm
T_5	CBEB	5 μm	0.5 μm
T_6	CBEB	30 μm	0.5 μm
Capacitor	Value		
$C_{bypass2}$	5 pF		

Output buffer			
Transistor	Config.	E.L.	E.W.
T_{18}	CBEB	20 μm	0.5 μm
T_{19}	CBEB	20 μm	0.5 μm

TFMSL	Width	Length
L5	3 μm	195 μm
L6	3 μm	300 μm
L7	3 μm	200 μm

Capacitor	Value
C_2	0.5 pF

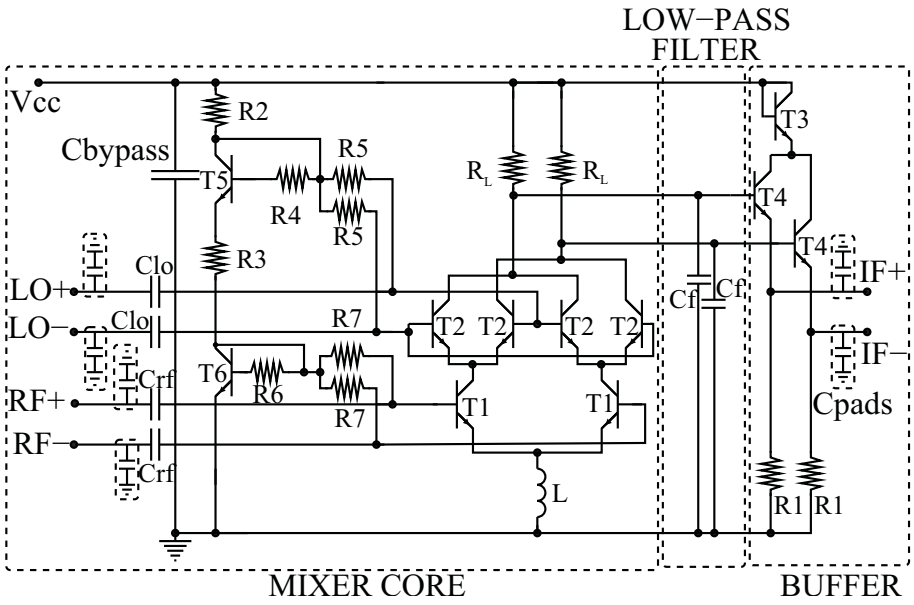
Biasing network (buffer)	
Resistor	Value
R_9	920 Ω
R_{10}	30 Ω
R_{11}	3k Ω
R_{12}	290 Ω
R_{13}	660 Ω
R_{14}	680 Ω
R_{15}	84 Ω
R_{16}	21 Ω

Transistor	Config.	E.L.	E.W.
T_8	CBEB	5 μm	0.5 μm
T_9	CBEB	5 μm	0.5 μm
T_{10}	CBEB	5 μm	0.5 μm
T_{11}	CBEB	5 μm	0.5 μm
T_{12}	CBEB	5 μm	0.5 μm
T_{13}	CBEB	5 μm	0.5 μm
T_{14}	CBEB	5 μm	0.5 μm
T_{15}	CBEB	5 μm	0.5 μm
T_{16}	CBEB	5 μm	0.5 μm
T_{17}	CBEB	20 μm	0.5 μm
T_{18}	CBEB	5 μm	0.5 μm
T_{19}	CBEB	5 μm	0.5 μm

Appendix E

Down-Converter Mixer

In this appendix, the values and parameters of each component utilized to design the fully differential down-converter mixer are presented. For the transistors parameters: ***Config.***: Configuration of the contacts (***B***: base, ***E***: emitter, ***C***: collector), ***E.L.***: Emitter length, ***E.W.***: Emitter width. For the inductors parameters: 1/4 ***turns***: Amount of quarter turns of the spiral inductors, ***w***: width, ***s***: spacing between the metal lines, ***ri***: inner radius.



Gilbert cell				
Resistor	Value			
R_L	150 Ω			
Transistor	Config.		E.L.	E.W.
T_1	CBEB		20 μm	0.5 μm
T_2	CBEB		20 μm	0.5 μm
Capacitor	Value			
C_{bypass}	2 pF			
C_{lo}	0.3 pF			
C_{rf}	0.3 pF			
Inductor	1/4 turns	w	s	ri
L	8	4 μm	2 μm	10 μm

Output buffer			
Resistor	Value		
R_1	x Ω		
Transistor	Config.	E.L.	E.W.
T_3	2 x CBEB	20 μm	0.5 μm
T_4	CBEB	20 μm	0.5 μm

Low-pass filter	
Capacitor	Value
C_f	0.5 pF

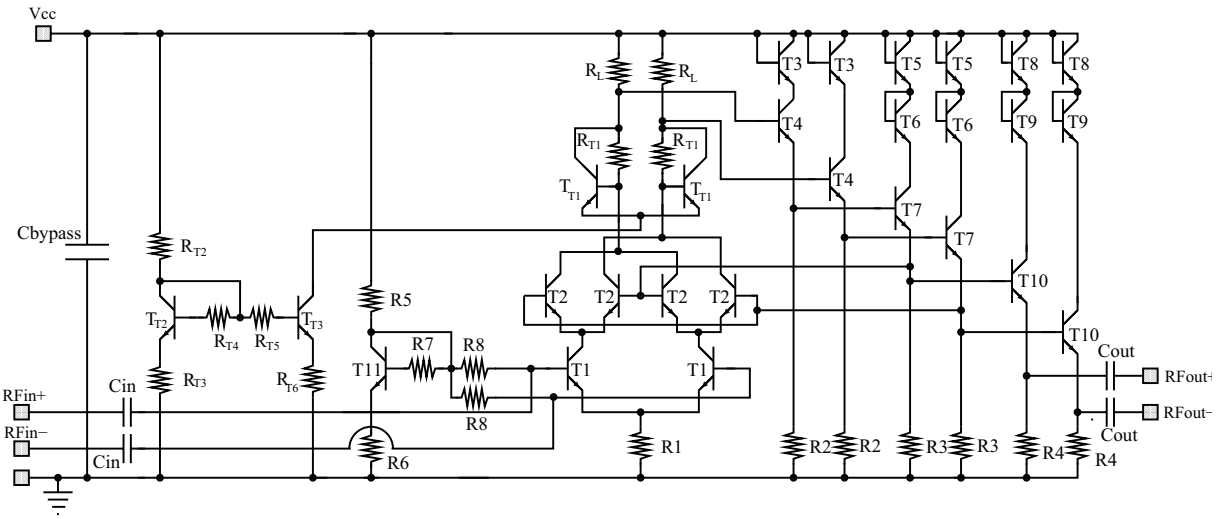
Biasing network			
Resistor	Value		
R_2	675 Ω		
R_3	150 Ω		
R_4	4k Ω		
R_5	1k Ω		
R_6	4k Ω		
R_7	1k Ω		
Transistor	Config.	E.L.	E.W.
T_5	CBEB	5 μm	0.5 μm
T_6	CBEB	5 μm	0.5 μm

Appendix F

Frequency Dividers

This appendix describes the values and parameters of the components used to design the dynamic frequency dividers using Atmel's SiGe2RF technology as well as IHP's SG25H1 technology. For the transistors parameters: ***Config.***: Configuration of the contacts (***B***: base, ***E***: emitter, ***C***: collector), ***E.L.***: Emitter length, ***E.W.***: Emitter width.

Atmel SiGe2RF



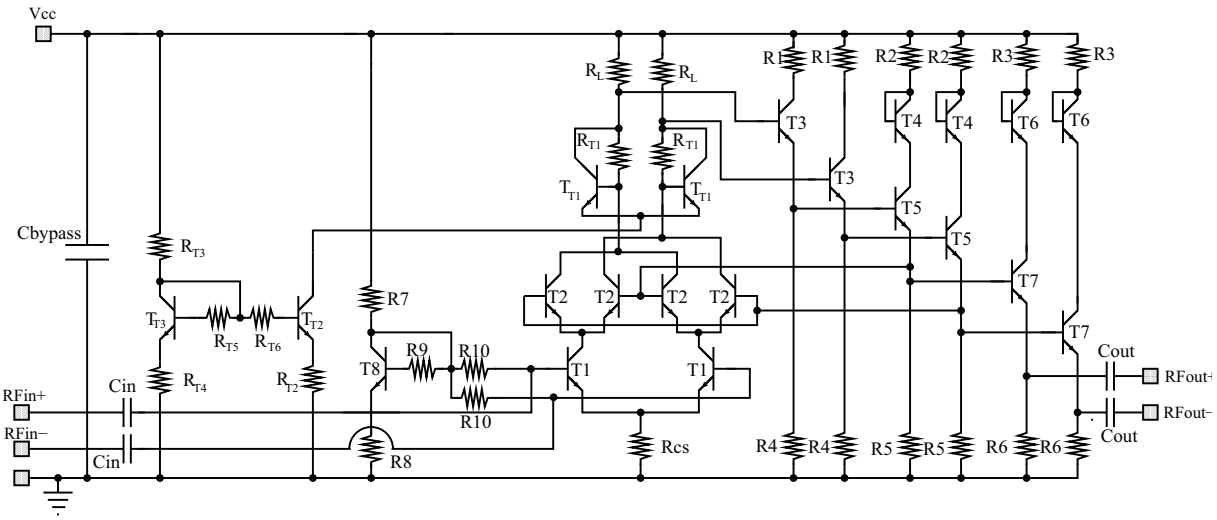
Gilbert cell			
Resistor	Value		
R_L	150 Ω		
R_1	63 Ω		
R_{T1}	300 Ω		
Transistor	Config.	E.L.	E.W.
T_1	CBEB	5 μm	0.5 μm
T_2	CBEB	5 μm	0.5 μm
T_{T1}	CBEB	5 μm	0.5 μm
Capacitor	Value		
C_{bypass}	2 pF		
C_{in}	200 fF		

Emitter followers			
Resistor	Value		
R_2	800 Ω		
R_3	600 Ω		
R_4	600 Ω		
Transistor	Config.	E.L.	E.W.
T_3	CBEB	5 μm	0.5 μm
T_4	CBEB	5 μm	0.5 μm
T_5	CBEB	5 μm	0.5 μm
T_6	CBEB	5 μm	0.5 μm
T_7	CBEB	5 μm	0.5 μm
T_8	CBEB	5 μm	0.5 μm
T_9	CBEB	5 μm	0.5 μm
T_{10}	CBEB	5 μm	0.5 μm
Capacitor	Value		
C_{out}	300 fF		

Biasing network	
Resistor	Value
R_5	850 Ω
R_6	126 Ω
R_7	1000 Ω
R_8	1000 Ω
R_{T2}	850 Ω
R_{T3}	120 Ω
R_{T4}	1000 Ω
R_{T5}	1000 Ω
R_{T6}	60 Ω

Biasing network			
Transistor	Config.	E.L.	E.W.
T_{11}	CBEB	5 μm	0.5 μm

IHP SG25H1



Gilbert cell			
Resistor	Value		
R_L	330 Ω		
R_1	60 Ω		
R_{T1}	570 Ω		
Transistor	Cell N°	E.L.	E.W.
T_1	2	0.84 μm	0.25 μm
T_2	1	0.84 μm	0.25 μm
Capacitor	Value		
C_{bypass}	1 pF		
C_{in}	0.2 pF		

Emitter followers			
Resistor	Value		
R_1	100 Ω		
R_2	100 Ω		
R_3	110 Ω		
R_4	900 Ω		
R_5	540 Ω		
R_6	540 Ω		
Transistor	Cell N°	E.L.	E.W.
T_3	1	0.84 μm	0.25 μm
T_4	1	0.84 μm	0.25 μm
T_5	1	0.84 μm	0.25 μm
T_6	1	0.84 μm	0.25 μm
T_7	1	0.84 μm	0.25 μm
Capacitor	Value		
C_{out}	x pF		

Biasing network	
Resistor	Value
R_7	2200 Ω
R_8	100 Ω
R_9	1000 Ω
R_{10}	1000 Ω
R_{T2}	274 Ω
R_{T3}	800 Ω
R_{T4}	100 Ω
R_{T5}	4000 Ω
R_{T6}	2000 Ω

Biasing network			
Transistor	Config.	E.L.	E.W.
T_8	1	0.84 μm	0.25 μm
T_{T2}	1	0.84 μm	0.25 μm
T_{T3}	1	0.84 μm	0.25 μm

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- Liu, G., **Chartier, S.**, Trasser, A., Schumacher, H. "Fully Integrated Millimeter-Wave VCO with 32 % Tuning Range" Topical Meeting on Silicon Monolithic Integrated Circuits in RF systems, San Diego, CA, USA, 19-21 Jan. 2009 (Accepted for Oral Presentation)

- Schleicher, B., **Chartier, S.**, Fischer, G., Korndörfer, F., Borngräber, J., Feger, T., Schumacher, H., "A Compact Low-Power SiGe:C BiCMOS Amplifier for 77-81 GHz Automotive Radar", Proc. 2008 IEEE Topical Meeting on Silicon Monolithic ICs in RF Systems (SiRF), Orlando, FL, USA, January 23-25, 2008, pp 195-198

- **Chartier, S.**, Schleicher, B., Feger, T., Purtova, T., Fischer, G., Schumacher, H., "79 GHz fully integrated fully differential Si/SiGe HBT amplifier for automotive radar applications", Analog Integrated Circuits and Signal Processing, Springer, Vol. 55, Number 1, April 2008, pp. 77-83

- **Chartier, S.**, Sönmez, E., Dederer, J., Schleicher, B., Schumacher, H. "Millimeter-Wave Si/SiGe HBT Frequency Divider Using Dynamic and Static Division Stages", Asia-Pacific Microwave Conference 2007 (APMC 2007), 11-14 Dec. 2007

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Curriculum Vitae

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Born on 31 March 1979 in Auchel, France
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Education

- **September 2002 - September 2003**
  Master's Degree in Microelectronic at the University of Lille, France / **Diplôme d'Etudes Supérieures Spécialisées** Microélectronique, radiofréquences et Hyperfréquences at the Université de Lille I, France (*with honors*)
- **September 2001 - September 2002**
  Maîtrise de physiques, Faculté Jean Perrin, Lens, France (*with honors*)
- **September 2000 - September 2001**
  Licences es Sciences-Physiques, Faculté Jean Perrin, Lens, France
- **September 1997 - September 2000**
  DEUG Sciences de la Matière, Faculté Jean Perrin, Lens, France (*with honors*)

Professional Experience

- **December 2007 - Present:**
  Member of the scientific staff at the Fraunhofer Institute for Applied Solid State Physics (IAF), Freiburg, Germany
- **October 2003 - November 2007:**
  Research associate at the Institute of Electron Devices, University of Ulm, Ulm, Germany
- **March 2003 - September 2003:**
  Internship at the Institute of Electron Devices and Circuits, University of Ulm, Ulm, Germany
- **June 2002 - August 2002:**
  Internship at the Laboratoire de Physique des Lasers et Molécules, University of Lille, Lille, France