Ingmar Kallfass

Comprehensive Nonlinear Modelling of Dispersive Heterostructure Field Effect Transistors and their MMIC Applications

Cuvillier Verlag Göttingen

Comprehensive Nonlinear Modelling of Dispersive Heterostructure Field Effect Transistors and their MMIC Applications

Dissertation

zur Erlangung des akademischen Grades eines

Doktor-Ingenieurs (Dr.- Ing.)

der Fakultät für Ingenieurwissenschaften

der Universität Ulm

von

Ingmar Kallfass

aus Stuttgart

1. Gutachter:	Professor Dr.-Ing. Hermann Schumacher
2. Gutachter:	Professor Dr. Thomas J. Brazil
Amtierender Dekan:	Professor Dr.-Ing. Hans-Jörg Pfleiderer
Datum der Promotion:	24. April 2006

2005

Bibliografische Information Der Deutschen Bibliothek
Die Deutsche Bibliothek verzeichnet diese Publikation in der Deutschen Nationalbibliografie; detaillierte bibliografische Daten sind im Internet über http://dnb.ddb.de abrufbar.
1. Aufl. - Göttingen : Cuvillier, 2006
Zugl.: Ulm, Univ., Diss., 2005
ISBN 3-86537-923-0

Nonnenstieg 8, 37075 Göttingen
Telefon: 0551-54724-0
Telefax: 0551-54724-21
www.cuvillier.de

1. Auflage, 2006
Gedruckt auf säurefreiem Papier

ISBN 3-86537-923-0

Acknowledgements

This work has been carried out at the Department of Electron Devices and Circuits of the University of Ulm. I gratefully acknowledge my debt to Professor Hermann Schumacher, whose excellent advice in the field of modelling and microwave circuit design has driven and motivated all aspects comprised in this work. He has built an excellent working environment, which promotes scientific achievements through a stimulating and sustained team dynamic.

Initial parts of this work have been carried out under the framework of the European Commission's Training and Mobility of Researchers Programme. My profoundest thanks to Professor Thomas Brazil at University College Dublin, for sharing his outstanding knowledge and work in the field of microwave theory and techniques. His continuous support and advice form, in a way, the essential backbone of this work. Sincere thanks also to my colleagues at UCD, especially Michael Wren, Breandan O'Hannaigh and Anding Zhu, for the technical discussions and, even more importantly, the overwhelming welcome in Ireland.

I am very grateful for the fruitful and excellent cooperation on the subject of the SiGe mHEMT technology and acknowledge the support from DaimlerChrysler Research, especially Dres. Ulf König, Hans-Joest Herzog, Thomas Hackbarth and Marco Zeuner. The Imperial College in London, particularly Dr. Kostis Michelakis, and Dr. Brian Raynor from the Fraunhofer Institute of Applied Physics in Freiburg for the joint wafer run of the SiGe mHEMT.

Many thanks to Innovative Processing AG for providing the InP pHEMT samples for characterisation and model extraction.

I acknowledge gratefully the important and helpful support of United Monolithic Semiconductors in Orsay and Ulm, particularly the help of Jan Grünenpütt, Phillipe Fellon, Charles Teyssandier, Klaus Beilenhoff and Eric Leclerc. Many thanks to UMS for providing GaAs pHEMT samples, the possibility of pulsed-IV measurements and MMIC fabrication.

For the stimulating discussions and their support in mixer measurements, I am especially indebted to Dres. Walter Ludwig and Axel Brokmeier of European Aeronautic Defence and Space Company.

This work would not have been possible without the enduring support and patience of my wife, Michelle, and the extraordinary support and advice of my parents.

Contents

Introduction

The Pseudomorphic High Electron Mobility Transistor (pHEMT) today is established as the prime transistor technology in analog front-ends of microwave and millimeter-wave applications. This is due to its up to date unrivalled capability of combining high cutoff frequencies with high power- and low noise performance. With the GaAs based device type offering highest maturity and availability, it is leading the microwave markets in wireless communication-, space-, defence- and automotive applications. In order to further improve cutoff frequencies and low noise performance, the metamorphic HEMT (mHEMT) concept has been developed, combining the advantages of a high In content in the channel region with GaAs substrates. Best performance, however, is reached in InP based pHEMT devices, which at the same time offer integrability with laser- and photo diode devices used in today's high-speed optical communication systems up to 80 Gbps. These well established technologies today are rivalled by potentially low-cost technologies, e.g. due to the improving power capability of high-speed SiGe heterojunction bipolar transistor (HBT) devices and the increased frequency performance of RF CMOS technologies, such as Silicon-on-Insulator (SOI) and strained-Si concepts. More recently, devices based on large bandgap materials like the GaN HEMT on SiC or Si substrates are entering high power markets like base stations in wireless communications. The mHEMT concept can also be applied to Si based devices by the introduction of strained-Si and strained-(Si)Ge channels formed on a SiGe buffer layer. This offers the potential of combining the high-frequency and low-noise HEMT performance with the ultra high integration density of conventional digital CMOS on the way towards the realisation of microwave System-on-Chip (SoC) applications.

A short time to market and prize competitiveness are the decisive factors for the success of products in the area of monolithic microwave ($f = 1...30\,\mathrm{GHz}$) and mm-wave ($f > 30\,\mathrm{GHz}$) integrated circuits (MMIC) and their systems. Therefore, an important element of the development chain of analog and mixed-signal ICs are accurate and efficient simulation models, enabling a reliable computer-aided design (CAD) prior to fabrication, and reducing or eliminating the need for costly and time-consuming redesign iterations. This is especially true for the III-V and advanced HEMT technologies, since they have to compete with the low-cost, high-volume Si-wafer based technologies mentioned above. Global validity in both the voltage operating domain as well as the frequency- and time domain qualifies a transistor model together with its computational efficiency when implemented into a simulation environment. In a comparison to purely physical and behavioural modelling approaches, the

compact, equivalent-circuit based models offer the best compromise between global validity, computational efficiency and adaptability to technology changes. The complex modulation schemes and stringent linearity requirements in modern electronic systems emphasize the need for such globally valid and efficient device models.

A particular challenge and area of research are frequency dispersive effects, present in all of the cutting-edge transistor technologies, due to effects of self-heating, carrier trapping and de-trapping, interface and surface charges as well as impact ionisation. On the device level, dispersion introduces a frequency- or time dependence to the current-voltage (IV) characteristics. Here, primarily the nonlinear drain current characteristics are concerned and most relevant for the overall device performance. On the circuit level, this has an impact on all of the major figures of merit in analog ICs. A dispersion model is required to accurately reflect both the static and the dynamic characteristics in MMICs.

This thesis presents a new custom model, universally applicable to dispersive HEMT transistors. The topics addressed cover areas from device characterisation and modelling, to the design and fabrication of MMIC applications. A novel theory for the inclusion of multiple time constant dispersion effects is developed and integrated into a nonlinear device model topology. Also, based on a novel unified approach to charge-conservative capacitance modelling, a nonlinear HEMT capacitance model is developed. An efficient drain current equation is employed to model both static and dynamic IV characteristics. The model, identical in topology and nonlinear functions, is fully extracted and validated for the following four different HEMT technologies:

- a 0.1 μm gate length strained-Si/SiGe mHEMT technology developed by Daimler-Chrysler Research,
- a 0.2 μm InP/InGaAs/InP pHEMT technology from Innovative Processing AG (IPAG),
- a commercial, state-of-the-art 0.15 μm AlGaAs/InGaAs/GaAs pHEMT high frequency, low-noise process, offered by United Monolithic Semiconductors (UMS) and
- the power version of the 0.15 μm GaAs pHEMT by UMS.

Based on the simulation model, which has been readily implemented into a conventional CAD environment, innovative MMIC applications with record performance have been successfully designed, fabricated and characterised.

In case of the strained-Si/SiGe mHEMT, the first full large-signal model has allowed for the successful realisation of the first and up to date only MMICs in this technology. A travelling-wave amplifier reaches 40 GHz with a gain of 4 dB.

Extraction and validation of the model for the InP pHEMT further proves the universal suitability of the adopted model topology and nonlinear functions, in particular the frequency dispersion part. The model is the first full large-signal model developed for this particular technology, enabling full circuit design and simulation capability.

As a supplement to the excellent foundry models of both the low-noise and the power version of the GaAs pHEMT, the presented model adds the dispersion capability as well as the more accurate nonlinear capacitance model. Travelling-wave MMICs have been realised in the power version of the GaAs pHEMT technology. A novel circuit concept is shown to act both as an ultra-broadband mixer and a variable gain amplifier (VGA). In excellent agreement with model prediction, a 2 dB conversion loss is reached within a bandwidth exceeding 50 GHz, while in amplifier mode, the gain can be controlled between 5...12 dB within a 43 GHz bandwidth.

Chapter 1

Modelled HEMT Technologies

This chapter deals with the different HEMT technologies which have been investigated by characterisation and model extraction. For all of them, a complete large-signal model including frequency dispersion has been developed.

Device performance related to the model extraction process is reviewed here. The discussion has a focus on electrical device characteristics and figures of merit (FOM). Technological issues are briefly discussed but extensively referenced only for the strained-Si/SiGe technology. For physics of the more conventional InP- and GaAs based devices as well as for basic HEMT operation theory, the reader is invited to refer to some of the excellent literature on this topic [1, 2, 3, 4]. Selected device physics will also be discussed in more detail in the section on frequency dispersion effects in chapter 2.2.

Special on-wafer modelling transistor samples with coplanar pad contacts and of varying gate size have kindly been provided by the respective device manufacturers. De-embedding techniques, described in detail in chapter 3.1, are employed to characterise and model the intrinsic HEMT devices.

1.1 Strained-Si/SiGe mHEMT

Strained-Si/SiGe Heterostructure Field-Effect Transistors (HFET) exploit the advantageous properties of the SiGe material system and its heterostructures to achieve significant speed improvement over conventional Si. Such devices can be realised in a variety of forms. Common to all concepts is the use of thin strained-Si or strained-(Si)Ge layers grown on top of a relaxed (virtual) substrate:

- Used as surface channel devices, one can realise n-channel and p-channel MOSFET structures. This concept has the prospect of significant speed enhancement to conventional CMOS and is therefore pursued by a number of major semiconductor companies, such as IBM [5, 6, 7], Intel, Philips and Atmel [8].

- In buried-channel devices, the principle of a two-dimensional electron- or hole gas (2DEG, 2DHG) in a quantum well is adapted to the $Si_{1-x}Ge_x$ material system. In

MOSFET-like devices with a gate dielectric layer, the channel is induced in a strained-Si layer by charge inversion. Technologically less complex devices use a channel which receives its carriers from donor layers on top and/or below, while the gate is typically formed by a metal-semiconductor (MS) or Schottky gate. Such devices are commonly designated as modulation-doped field-effect transistor (MODFET) or, in the case of n-channel devices, as HEMT. The buried-channel concept has the advantage of achieving higher cutoff frequencies due to reduced interface scattering. Also, being technologically less complex, it is more cost effective. SiGe MODFETs make use of strained-Si layers for n-type conduction or strained-(Si)Ge layers for p-type conduction. Such devices have been developed mainly by IBM [9, 10, 11, 12] and DaimlerChrysler Research [13, 14, 15] and have reached an impressive state of maturity. In Europe, in a close cooperation of several research groups, the development of the strained-Si/SiGe mHEMT approach has received support from several research projects, primarily the European Commission's SIGMUND [16] and Training and Mobility of Researchers (TMR) Network "SiGe Hetero Devices" [17] as well as the British EPSRC project SiGeMOS [18].

The formation of strained layers requires an underlying relaxed SiGe virtual substrate (VS). This in turn requires a buffer layer, grown on top of the Si substrate and allowing for lattice constant adjustment to the relaxed SiGe VS. Therefore, the device type is in principle a metamorphic one and hence designated as mHEMT in this work. To date, the realisation of these buffer layers is subject to intense research, motivated by the reduction of the necessary vertical layer thickness with the aim of achieving a flat topology favourable for a future integration of the SiGe mHEMT with standard Si CMOS. Several European groups are pursuing this aim employing different buffer technologies. In addition to the graded buffer using molecular-beam epitaxy (MBE), the approach used by DaimlerChrysler Research Ulm [19], techniques like low-temperature epitaxy (LTE) [20], low energy plasma enhanced chemical vapour deposition (LEPECVD) [21] and He-implantation assisted relaxation [22] are investigated.

Introducing alloys with Germanium into Si-based semiconductor devices offers various possibilities of improving the electrical performance of transistors. The difference in bandgap energy E_g of these two elements and their alloys allows for the realisation of hetero-interfaces in the conduction- and valence bands, a process often referenced as "bandgap-engineering". In the well-established SiGe HBT technology, for instance, the difference in bandgap energy in the base and emitter leads to a dramatic increase of current gain or emitter efficiency due to the suppression of reverse carrier injection from the base into the emitter. The MODFET, on the other hand, exploits the increased mobility of carriers when being spacially separated from their ionized donators/acceptors acting as scattering centers. In addition to mobility enhancement due to reduced scattering, one also exploits the significantly higher mobility of carriers in strained $Si_{1-x}Ge_x$ layers itself. The best mobility results are obtained for buried-channel devices (reduced interface scattering). For n-channel devices, record values

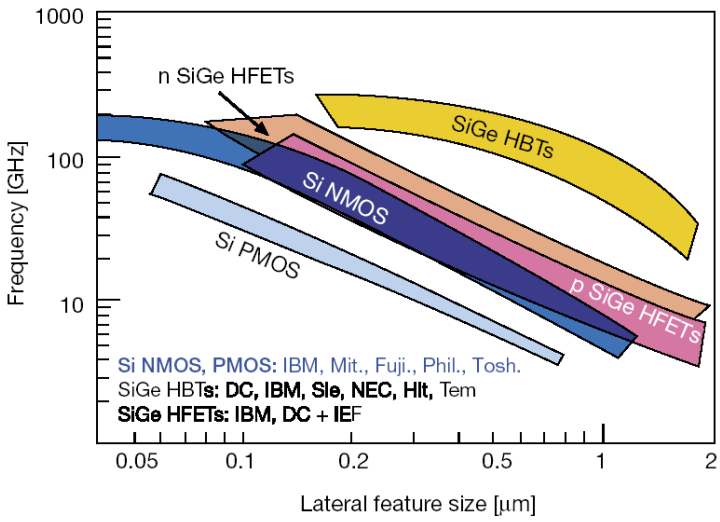

Figure 1.1: Maximum frequencies of oscillation of n- and p-channel SiGe HFETs compared to standard Si MOS and SiGe HBT, with respect to lateral device size. Source: [29].

of $\mu_n = 2800$ cm^2/Vs have been reported [23], an approximately six-fold increase to the universal electron mobility of inversion layers in Si [24][25]. In p-channel MODFETs, hole mobilities of $\mu_p = 3000\,$cm^2/Vs have been achieved [26], representing an 18-fold increase to universal hole mobility in Si .

Fig. 1.1 shows the maximum frequencies of oscillation f_{max} of n- and p-channel SiGe MODFETs obtained from the main research groups compared to those of standard Si nMOS and pMOS as well as SiGe HBT technologies. The highest published results for the n-channel mHEMT type to date are $f_T = 90$ GHz and $f_{max} = 188$ GHz for the DaimlerChrysler device [27] and $f_T = 92$ GHz and $f_{max} = 212$ GHz for a recent IBM device [28].

In the SiGe mHEMT developed by DaimlerChrysler [30, 31] and employed in this work, a 2DEG is formed in a strained-Si quantum well, sandwiched between two Sb-doped SiGe supply layers. Obtaining a quantum well for electrons in the Si/SiGe material system is not so obvious, since it is well known from the SiGe HBT that the bandgap difference between Si and SiGe results in a valence band offset of almost the same magnitude $\Delta E_V \approx \Delta E_g$ and $\Delta E_C \approx 0$ eV [32]. An offset in the conduction band is achieved when the large bandgap Si material is strained. Then, a staggered or type-II hetero-interface is formed, generating the required conduction band quantum well for the HEMT channel [15, 33, 7]. All epitaxial layers are grown by MBE. In order to form a relaxed SiGe layer acting as VS, a relatively thick graded buffer is grown on the Si wafer. Fig. 1.2 shows the complete layer stack of the device, including the graded buffer, virtual substrate, active MBE layers as well as the HEMT structure. The 2 μm thick graded buffer has a final Ge content of 40 %.

In the frame of this work, the strained-Si/SiGe mHEMT has been extensively characterised in terms of its DC-, dynamic small- and large-signal- as well as microwave noise characteristics.

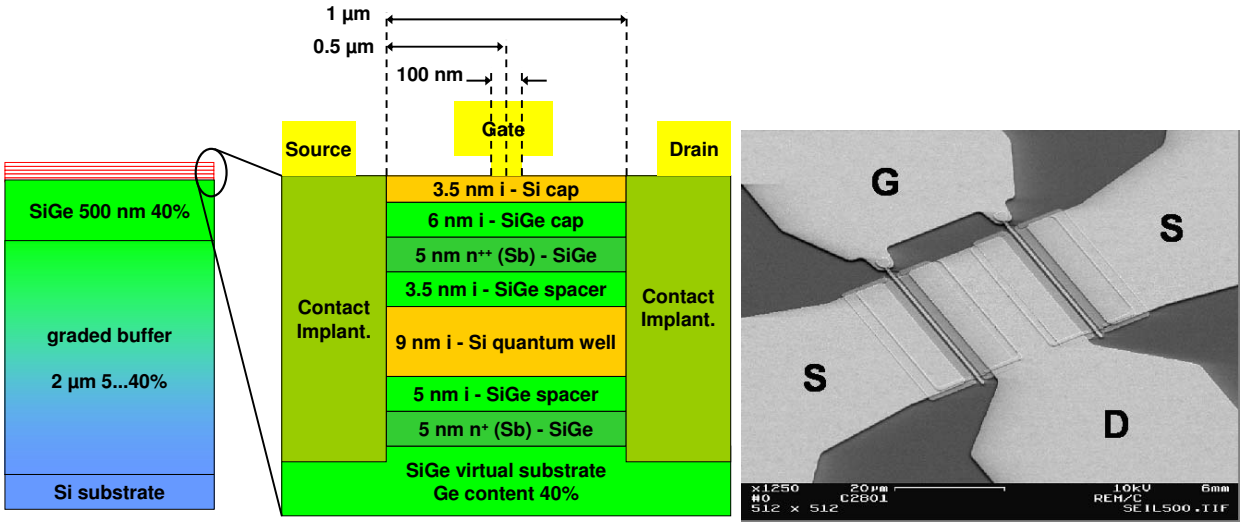

Figure 1.2: Left: Strained-Si/SiGe mHEMT layer stack including the virtual substrate- and epitaxial HEMT layers. Right: Device microphotograph with π-shaped gate structure.

Parameter	Symbol	Unit	Typical
Transition frequency	f_{T}	GHz	51
Maximum freq. of oscillation (via U)	f_{max}	GHz	101
Maximum transconductance (dynamic)	$g_{\mathrm{m,max}}$	mS/mm	250
Output conductance (dynamic)	g_{ds}	mS/mm	13
Optimum gate-source voltage ($g_{\mathrm{m,max}}$)	$V_{\mathrm{gs,opt}}$	V	-0.3
Optimum drain current ($g_{\mathrm{m,max}}$)	I_{dss}	mA/mm	75
Threshold voltage	V_{t}	V	-0.7
Drain-source breakdown voltage	V_{bds}	V	3.5

Table 1.1: Strained-Si/SiGe mHEMT figures of merit.

Fig. 1.3 shows the extrapolation of f_{T} and f_{max} under maximum gain conditions in a $2\,\mathrm{x}\,50\,\mu$m gate width, $0.1\,\mu$m gate length strained-Si/SiGe mHEMT. Typical measured cutoff frequencies are $f_{\mathrm{T}} = 51$ GHz and $f_{\mathrm{max}} = 101$ GHz. Fig. 1.3(right) plots cutoff frequencies versus drain voltage. f_{T} doesn't drop significantly down to very low voltages of about $V_{\mathrm{ds}} = 0.4$ V. This is the reason why, recently, the SiGe mHEMT's advantages in the field of low-power applications have been investigated [34, 35].

Fig. 1.4 shows the minimum noise figure F_{min} together with associated gain G_{ass}. The device achieves as low as 1.8 dB noise at 24 GHz, important e.g. for applications in this ISM (industrial-scientific-medical) band. In the Ku-band, a noise figure of about 0.5 dB is achieved with a respectable associated gain of 11.9 dB. Optimum bias for low-noise operation is $V_{\mathrm{gs}} = -0.3$ V and $V_{\mathrm{ds}} = 2.5$ V. The right plot of Fig. 1.4 shows cutoff frequencies versus gate voltage. The voltage regime for high f_{T} extends well down to low gate bias, where low noise operation occurs.

Table 1.1 lists the main figures of merit of the strained-Si/SiGe mHEMT.

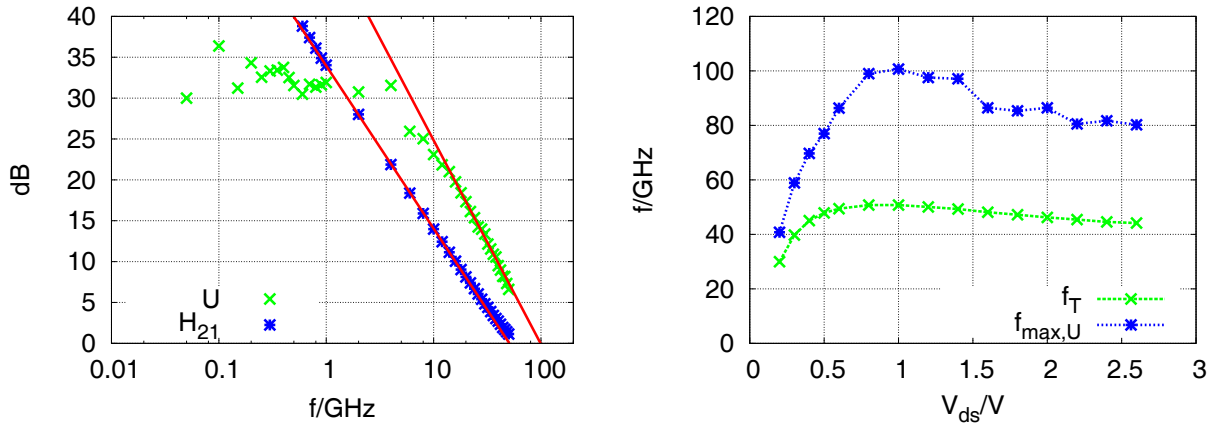

Figure 1.3: Extrapolation of f_{T} and f_{max} in a 2x50 μm strained-Si/SiGe mHEMT (left). The plot of cutoff frequencies versus drain voltage shows the device's suitability for low-power operation (right).

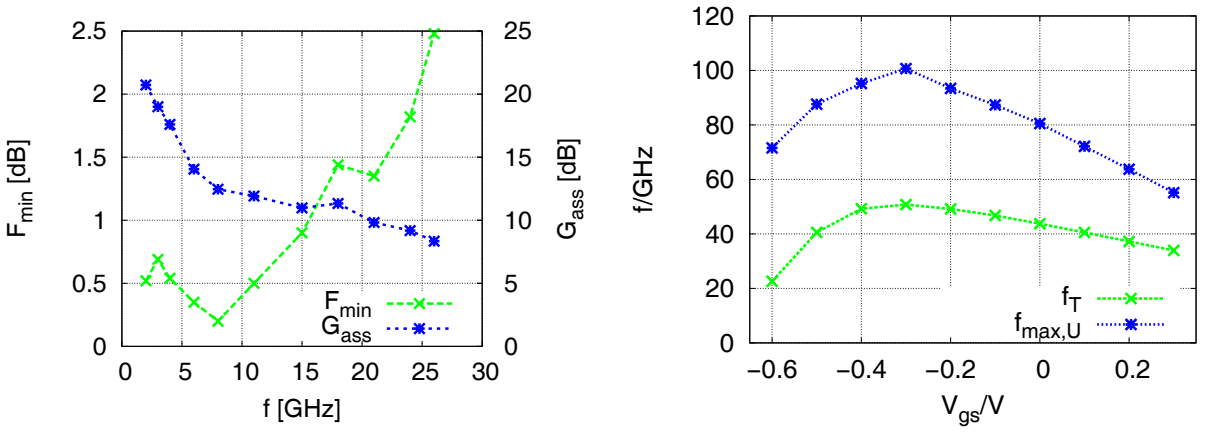

Figure 1.4: F_{min} and G_{ass} in a 2 x 50 μm strained-Si/SiGe mHEMT versus frequency (left). Plotting cutoff frequencies versus gate voltage reveals that high gain is achieved together with low noise (right).

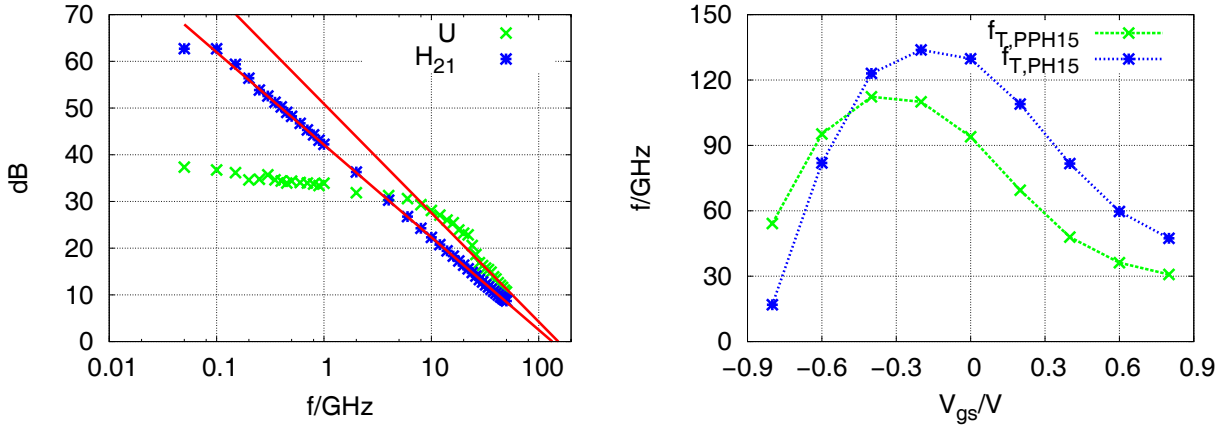

Figure 1.5: Extrapolation of f_T and f_{max} in a 2x50 μm PH15 device (left). Comparison of PH15- and PPH15 transition frequency versus gate voltage (right).

This performance data together with the achieved technological maturity and reproducibility recommend the strained-Si/SiGe mHEMT for the realisation of microwave and mm-wave applications. The device offers high cutoff frequencies with low-noise and adequate power capabilities. Previous modelling work concentrated on physical and small-signal model extraction [36, 37]. The developed model in this work is the first full large-signal model for the SiGe mHEMT together with the rigorous investigation and modelling of frequency dispersion. Its implementation in a circuit design environment has enabled the design and realisation of the first Si/SiGe MMIC applications [38, 39].

1.2 Low Noise- and Power AlGaAs/GaAs pHEMT

On-wafer transistor samples of the commercial 0.15 μm gate length GaAs pHEMT process "PH15" from UMS are used for characterisation and model extraction. The PH15 process is optimised for low noise- and high frequency performance of its active devices. This very mature and optimised technology reaches a measured f_T of 134 GHz and f_{max} of 152 GHz. The power variant of the 0.15 μm GaAs pHEMT process from UMS is abbreviated as PPH15. The process trades a reduction in the cutoff frequencies with $f_T = 112\,\text{GHz}$ and $f_{max} = 97\,\text{GHz}$ for a high breakdown voltage of $V_{bds} = 8\,\text{V}$. This is achieved by introducing double supply layers, i.e. delta-doping is used both below and on top of the InGaAs quantum well [40]. Doping levels are reduced compared to the single-supply of the PH15 process, resulting in higher breakdown voltage. Fig. 1.5 shows the comparison of f_T versus gate voltage for PH15 and PPH15. Both the maximum value and the gate voltage for maximum gain are shifted. Table 1.2 shows selected figures of merit for the PH15- and PPH15 pHEMT technologies.

Fig. 1.6 shows a microphotograph of a $4\,\text{x}\,75\,\mu$m PPH15 transistor sample in common-source configuration. In addition to being grounded by via holes, the source contacts are

Parameter	Symbol	Unit	PH15	PPH15
Transition frequency	f_{T}	GHz	134	112
Maximum freq. of oscillation (via U)	f_{max}	GHz	152	97
Maximum transconductance (dynamic)	$g_{\mathrm{m,max}}$	mS/mm	900	720
Output conductance (dynamic)	g_{ds}	mS/mm	40	70
Optimum gate-source voltage ($g_{\mathrm{m,max}}$)	$V_{\mathrm{gs,opt}}$	V	-0.1	-0.3
Optimum drain current ($g_{\mathrm{m,max}}$)	I_{dss}	mA/mm	350	270
Threshold voltage	V_{t}	V	-0.8	-1.0
Drain-source breakdown voltage	V_{bds}	V	3.8	8.0

Table 1.2: Low noise- and power AlGaAs/GaAs pHEMT (PH15 and PPH15) figures of merit.

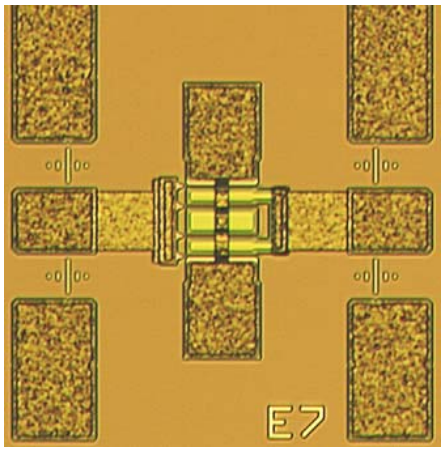

Figure 1.6: Microphotograph of a $4\,\mathrm{x}\,75\,\mu$m PPH15 transistor with coplanar GSG contact pads and source via holes.

connected by an air-bridge. The transistor dedicated to modelling purposes is carried out with coplanar ground-signal-ground (GSG) contact pads for on-wafer characterisation capability.

The model developed in this work represents a supplement to the foundry design kit models for these devices. The following improvements recommend the new model when compared to the design kit:

- A single model achieves accurate and global small- and large signal performance and may replace the three separate design kit versions (small-signal model, nonlinear model in linear- and nonlinear model in saturation regimes)

- The new model achieves global small-signal validity, whereas the foundry small-signal model is validated for particular bias voltages ($g_{\mathrm{m,max}}$ and F_{min}) exclusively in the saturated operating region.

- The frequency dispersion part is entirely new. The nonlinear foundry models are based on pulsed-IV measurements in order to accurately reflect the dynamic device

characteristics. Static device characteristics are not correctly predicted. Also, as shown in chapter 3.5, pulsed-IV measurements are not capable of including dispersion effects with high corner frequencies, such as impact ionisation.

- The foundry models describe the nonlinearities of the gate-to-source capacitance C_{gs}, but assume constant gate-drain capacitance C_{gd}. The new model describes both nonlinearities in novel charge-conservative capacitance expressions.
- The new model improves accuracy in the millimeter wave regime by the inclusion of the non-quasi static resistor R_{gdi} in series to C_{gd} (see Fig. 3.9).
- Transient simulation capability is added, too, whereas another special foundry model is required for that purpose.

1.3 InGaAs/InP pHEMT

The InP pHEMT process of IPAG and University of Duisburg [41] has been developed for monolithic integration of optical and electronic devices in order to realise OEIC applications for high-speed optical communication systems. The HEMT structure and epitaxial layers are integrated together with HBTs and PIN receiver photodiodes as well as passives (MIM capacitors and resistors). The $0.2\,\mu$m gate length transistor uses a strained $In_{0.61}Ga_{0.39}As$ channel layer with InP layers on top acting as spacer-, supply layer and Schottky barrier. Fig. 1.7 shows the transistor layer stack. The channel forms in a 17 nm thick InGaAs quantum well, receiving its carriers from a single n-doped supply layer on top, separated from the hetero-interface via a nominally intrinsic InP spacer layer.

Only few data is reported in the literature for the electrical properties of strained-InGaAs on relaxed InP buffers. For strained $In_{0.69}Ga_{0.31}As$ on InP and at room temperature, [42] states a bandgap energy of 661 meV, a conduction band offset of $\Delta E_{\mathrm{C}} = 315 \pm 25\,\mathrm{meV}$ as well as an electron mobility of $\mu_{\mathrm{n}} \approx 18000\,\mathrm{cm}^2/\mathrm{Vs}$ and the saturated electron velocity of $v_{\mathrm{sat}} \approx 3.0 \cdot 10^7\,\mathrm{cm/s}$.

Table 1.3 lists the main parameters in terms of electrical performance of this technology, fully characterised within the frame of this work. The $2\,\mathrm{x}\,40\,\mu$m device reaches a measured f_{T} of 114 GHz and f_{max} of 119 GHz (Fig. 1.8) at $V_{\mathrm{gs,opt}} = 0.1\,\mathrm{V}$[1].

The application and validation of the nonlinear custom model to the InP devices underlines its universal suitability for HFET technologies. The same model in terms of topology and nonlinear functions, as described in the following chapters, has been used for all technologies introduced here.

[1] In the samples used for model extraction, the passivation process introduced a shift in threshold voltage of $\approx 0.15\,\mathrm{V}$ compared to the typical threshold of about $V_{\mathrm{t}} = -0.4\,\mathrm{V}$ in this technology.

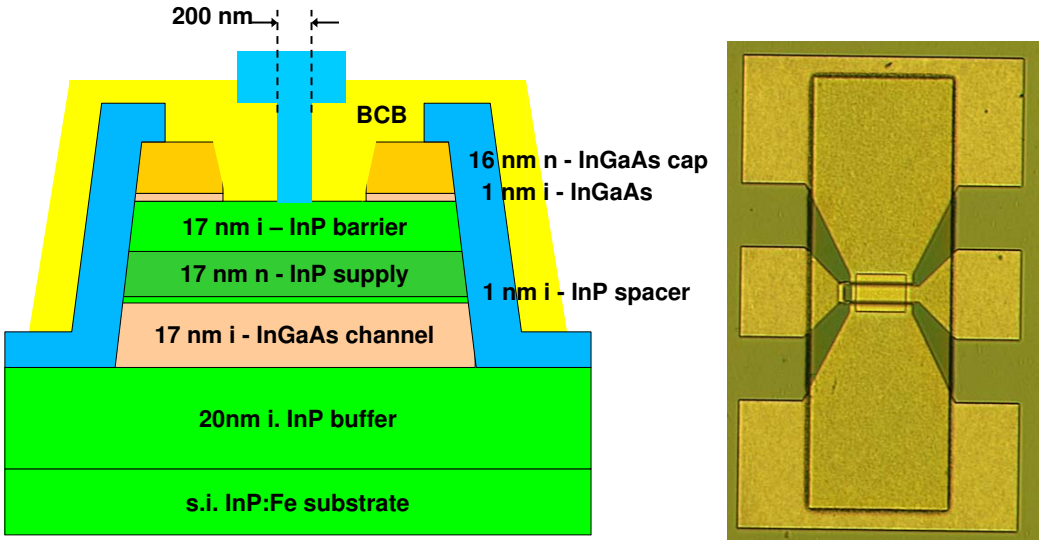

Figure 1.7: Layer Stack of a 200 nm gate length InGaAs/InP pHEMT (left). Microphotograph of a $2\,\mathrm{x}\,40\,\mu$m device with coplanar GSG contact pads (right).

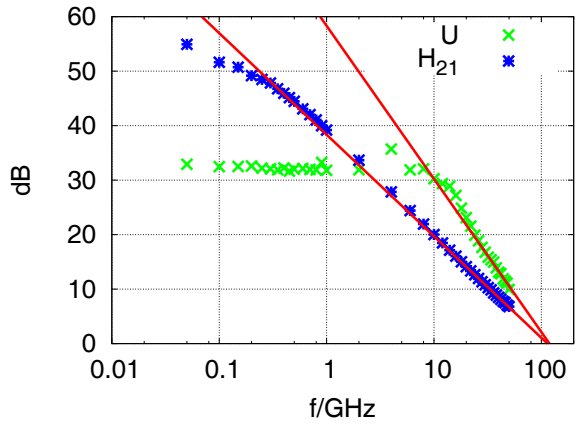

Figure 1.8: Transition frequency and maximum frequency of oscillation under maximum gain conditions in a $2\,\mathrm{x}\,40\,\mu$m InP pHEMT device.

Parameter	Symbol	Unit	Typical
Transition frequency	f_T	GHz	114
Maximum freq. of oscillation (via U)	f_max	GHz	119
Maximum transconductance (dynamic)	$g_\mathrm{m,max}$	mS/mm	1010
Output conductance (dynamic)	g_ds	mS/mm	21
Optimum gate-source voltage ($g_\mathrm{m,max}$)	$V_\mathrm{gs,opt}$	V	0.1
Optimum drain current ($g_\mathrm{m,max}$)	I_dss	mA/mm	170
Threshold voltage	V_t	V	-0.25
Drain-source breakdown voltage	V_bds	V	4.5

Table 1.3: Measured figures of merit of the InGaAs/InP pHEMT.

Chapter 2

Modelling of Frequency Dispersion in HFETs

Common to all HEMT technologies described in the previous chapter is the presence of dispersive effects, which are not negligible for accurate circuit design. Therefore, this chapter outlines the issue of frequency dispersion in HFETs and its incorporation in device models. The efficient and accurate modelling of such effects represents the main task of the thesis.

After discussing the physical- and empirical modelling approaches in HFETs, an overview of the different physical effects responsible for frequency dispersion is given. State-of-the-art dispersion models are described and discussed. The importance of including dispersion in device models for circuit design is demonstrated. Finally, the methods for obtaining dynamic IV characteristics adopted in this work are presented.

2.1 Physical- Versus Empirical Large-Signal Modelling

In the literature, different and partially conflicting usage is made of the designation "physical" and "empirical" in conjunction with FET models. Strictly speaking, physical modelling consists of solving electromagnetic field- and transport equations as well as quantum mechanics, based on an input of material parameters and detailed geometrical information of the devices' layer structures. Purely physical modelling techniques are useful in the development and optimisation of new transistor technologies. The computational efficiency required in circuit design, however, calls for equivalent circuit based models. Although any lumped element equivalent circuit will be but an approximation of the real transistor device, some of those models may also be called physical. This is generally the case when the model's nonlinear element functions employ parameters which can be directly linked to physical entities, e.g. built-in potentials, mobilities μ or, in the case of hetero-devices, energy band offsets. Model parameters like threshold voltage V_t and the transconductance parameter β are then expressed as a function of such purely physical parameters. Typically, however, the validity of physical model parameters and equations is limited to a certain operating regime of the

transistor device, e.g. the saturated operating region. To achieve a full nonlinear device model, the expressions for different operating conditions are then linked together by smoothing functions and additional parameters assuring continuity of partial derivatives. This constitutes an empirical process and the model reduces to a semi-physical nature. Popular examples for such semi-physical models are the BSIMv3 model and its follow-up versions [43] and the EKV-model [44] developed for Si MOSFET technologies. For HFETs, semi-physical models have been deduced e.g. in [45]. Thus, a physical model can be defined as one which does not make use of parameter extraction and -optimisation based on characterisation of the modelled device. Frequently, however, some of the required entities for the development of a physical model are either unknown or cannot be determined to a satisfactory degree of accuracy in modern semiconductor devices. Then, the originally physical model parameters are extracted from device measurements, just as in the case of empirical model parameters.

Consequently, an empirical model can be defined as one whose parameters are extracted from measurements performed on the devices which are to be modelled. In the case of HEMTs dedicated to MMIC design, special on-wafer modelling transistor samples and de-embedding procedures are used for that purpose. Empirical models may be sub-divided in three categories: analytical, table-based and behavioural. The analytical type uses an equivalent circuit topology whose nonlinear elements are described via analytic equations, which may be partly related to physical properties or entirely empirical. Table-based models use measurement data that is directly used in the definition of the nonlinear model elements, without deriving the parameters of analytical equations for these elements. Interpolation splines are employed to obtain nonlinear characteristics, typically derived from multi-bias small-signal data (e.g. [46, 47]). Behavioural modelling is aimed at the system level and used both for single transistors and matched amplifiers. Behavioural models are typically built on large-signal measurement data and use Volterra-series to formulate nonlinear behaviour (e.g. [48, 49, 50]).

Fig. 2.1 qualitatively compares the suitability of physical- and empirical (analytical as well as table-based) models for HFETs in terms of important criteria in circuit design. The centre of interest is not achieved globally in the different model types: while the intimate relationship of physical models with devices allow for easy adaptability to technology changes and consistent parameter correlation in spread analysis, they suffer in simulation efficiency in terms of convergence, global validity and computation time. Table-based spline models, being based entirely on measurement data, are easy to extract and computationally efficient. However, all relation to physics is lost and their validity is limited to the characterisation regime, which may result in convergence problems under strong nonlinear operation. The analytical model approach offers a compromise between simulation efficiency and global validity one one side, and physical interpretability of its parameters on the other side.

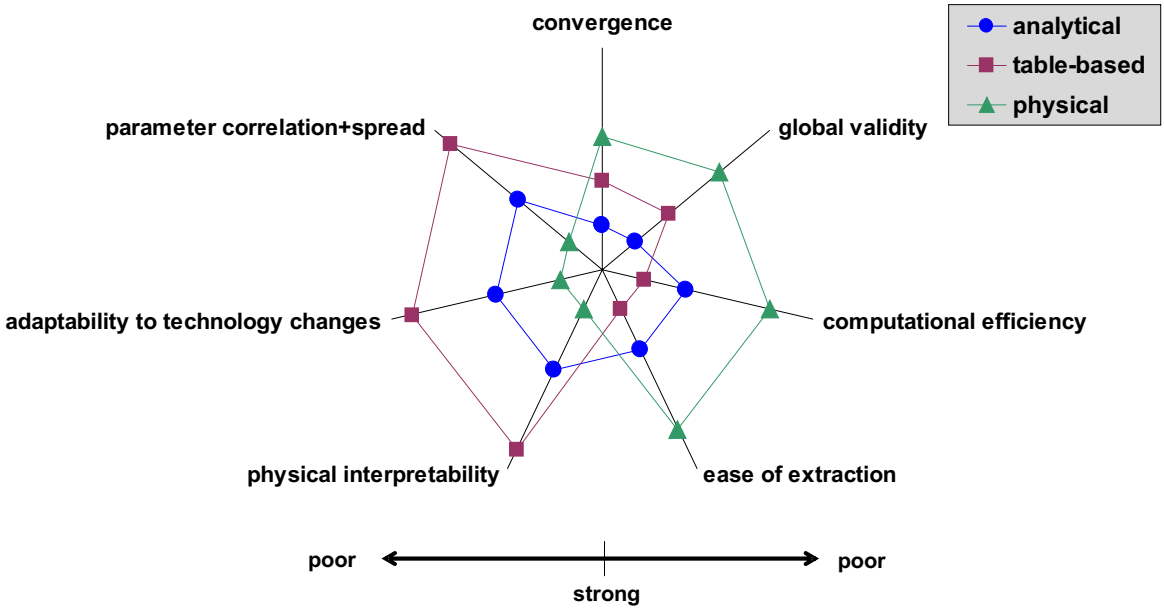

Figure 2.1: Qualitative comparison of physical- and empirical (analytical as well as table-based) HFET models in terms of important circuit design criteria. In the diagram, best performance is indicated close to the centre. Analytical models are the best compromise between relation to device physics and efficiency in simulation.

2.2 Effects of Frequency Dispersion in HFET Devices

Several physical effects are responsible for frequency dispersion in HFET devices. Depending on the device type and substrate, different dispersion effects are predominant and have distinct influence. The following discussion briefly introduces the individual phenomena and their impact on device characteristics. As justified in the previous section, the presented new modelling technique is of empirical nature. Dispersion phenomena are described by the model solely in terms of time constants and impact on drain current characteristics, without considering their physical origin. Therefore, the discussion here will focus on the qualitative impact of individual dispersion effects on drain current characteristics.

From a general point of view, the density of charges in an HFET is frequency dependent, affecting both the conductive, i.e. current, and reactive, i.e. capacitance, components within the device. In fact, characterisation methods like Deep Level Transient Spectroscopy (DLTS) [51] are typically employed to investigate the density and energy level of charge traps in semiconductors by monitoring capacitance - and sometimes also current - transients. The reason for modelling efforts to concentrate on the drain current response lies in the time constants or corner frequencies of dispersion effects. The most dominant effects occur in the kHz-, MHz- and lower GHz range. At these frequencies, the conduction currents in present-day HEMTs dominate the displacement currents, and it is generally sufficient to model capacitances above any dispersion corner frequency, i.e. in the microwave regime.

- **Thermal- or self-heating effect**: with increasing current density the channel region of the device heats up due to the dissipated power. Increasing temperature in turn results in a reduction of carrier mobility μ, saturation velocity v_{sat} and consequently, drain current. Both μ and v_{sat} vary approximately inversely with temperature and effective mobility can be described by the following equation [52]:

$$\mu = \frac{\mu_0}{1 + \frac{P_{\mathrm{diss}}}{P_{\mathrm{eff}}}} \tag{2.1}$$

  where μ_0 is the carrier mobility at ambient temperature, P_{diss} is the statically dissipated power and P_{eff} is a scaling constant. The thermal effect in HEMTs depends on the thermal conductivity k of the underlying substrate and buffer layers. At room temperature, bulk InP has $k = 68\,\mathrm{W/mK}$, which is about 33 % higher than that of bulk GaAs with $k = 51\,\mathrm{W/mK}$. Also, since the thermal effect scales with total current, it becomes more pronounced in large devices, dedicated to power applications. Therefore, among the devices modelled in this work, the self-heating effect will be most pronounced in the GaAs pHEMT. Bulk Si at room temperature has a high thermal conductivity of $k = 130\,\mathrm{W/mK}$. However, a $Si_{0.6}Ge_{0.4}$ alloy has a much lower conductivity of $k \approx 8\,\mathrm{W/mK}$ [53]. The investigated SiGe mHEMT device, being grown on an undoped relaxed $Si_{0.6}Ge_{0.4}$ buffer, will therefore also experience self-heating to some extent. The self-heating effect, in large devices with low k like the GaAs pHEMT

and under high static power operation, will lead to the typical negative slope in static output characteristics. If the high-power regime is entered only dynamically by a signal or waveform, the device doesn't change temperature fast enough and thermal current reduction does not take place, but will adopt an average temperature corresponding to that of the quiescent- or bias point Q of the device. Self-heating therefore is frequency-dependent and gives rise to a dispersion effect.

- **Traps**: in the channel region of the device energy states, called "traps", may exist within the bandgap, capturing or "trapping" free electrons or holes. Traps may stem from impurity atoms, crystalline defects and dislocations, interfaces or grain boundaries. Trapped carriers reduce the free carrier density which constitutes the drain current. Traps basically introduce two time constants, the trapping time taken to capture the carriers, and the de-trapping time taken to release carriers back into the conduction- or valence bands. This effect therefore introduces dispersion to drain current.

- **Interface and Surface States**: at epitaxial layer interfaces or surfaces, particularly at hetero-interfaces, the presence of bond breaks, lattice dislocations or impurity atoms introduces charges that modify the effective potentials within the active device region, and consequently, drain current. Similarly to traps, the presence of such charges is subject to time constants, introducing yet another dispersive characteristic [54].

- **Impact Ionisation**: under extremely high field strengths, occurring at the drain end of a HEMT channel and at high V_{ds}, electrons can gain sufficient kinetic energy to cause impact ionisation. This results in avalanche current flowing partly into the substrate (Kink current) and into the gate (gate-drain breakthrough), but also towards the source. Since it takes time for impact ionisation to occur, this effect is dispersive and doesn't happen if the high field strengths do not exist long enough, e.g. under high frequency operation. The impact ionisation effect exists in any HEMT type, but is most pronounced in the small bandgap InGaAs channel layer of the InP device [55].

Fig. 2.2 summarises the impact of frequency dispersion effects on drain current characteristics for a $8\,\mathrm{x}\,100\,\mu$m GaAs power pHEMT (PPH15) device. Static output characteristics are compared to dynamic ones obtained via integration of dynamic $g_{\mathrm{m}}/g_{\mathrm{ds}}$ data (see chapter 2.5). In the high power region, the device undergoes self-heating. In the knee region, the substantial difference between dynamic and static curves is mainly attributed to the impact of trapping effects. Finally, at high V_{ds}, the static curves show the onset of impact ionisation, which is eliminated in the dynamic characteristics.

A discussion of frequency dispersion would not be complete without mentioning dispersion effects in GaN HEMTs, which are the main obstacle to achieving the theoretically possible high output power levels at microwave frequencies. Current collapse designates the reduction of dynamic- compared to static current and is attributed to the development of parasitic

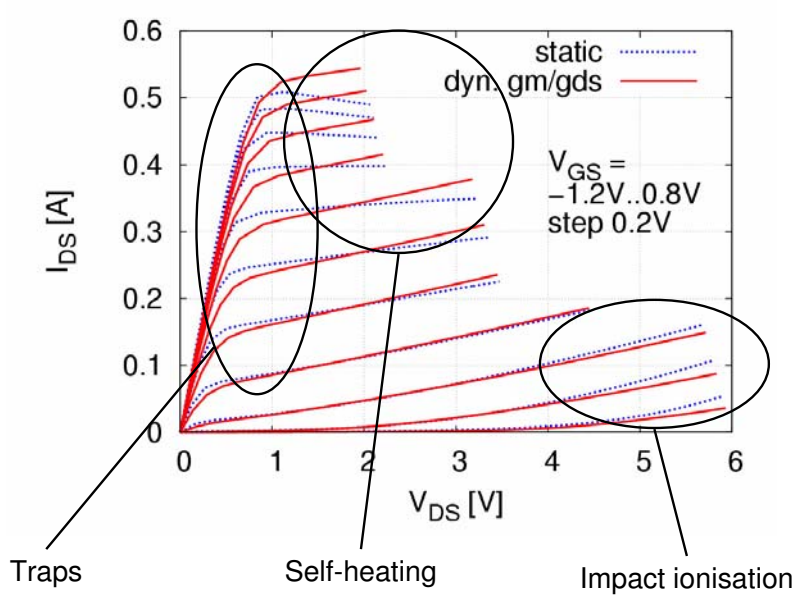

Figure 2.2: Static and dynamic drain current characteristics of a $8\,\mathrm{x}\,100\,\mu$m GaAs power pHEMT. Major regions affected by dispersion effects are highlighted.

charge in the drain region close to the gate (formation of a so-called "virtual second gate") [56] as well as trapping effects in the GaN buffer layer. The current response to a change in gate voltage is limited by the charging- and de-charging of this interface charge. The terms "gate lag" or "drain lag" are employed when referencing the same effect with respect to pulsed operation and transient response [57].

Another dispersion mechanism caused by impact ionisation is referred to as Kink effect in thick film SOI MOSFETs, where a frequency-dependent Kink current between the drain and body region (undepleted part of the silicon layer on oxide) is generated [58].

2.3 State-of-the-Art Modelling Approaches

An overview of state-of-the-art modelling approaches to frequency dispersion is given. The discussion focuses on equivalent circuit-based models, i.e. such dispersion models that are based on a topology of electrical circuit elements, and therefore can be implemented in a CAD environment.

2.3.1 Thermal models

Thermal models incorporate temperature as a circuit parameter. An R-C type subcircuit is used to represent instantaneous device temperature. More recent thermal models suggest the incorporation of several, typically two, thermal time constants (e.g. [59]) representing fast and slow thermal effects related to different regions or layers of the device. Fig. 2.3 shows

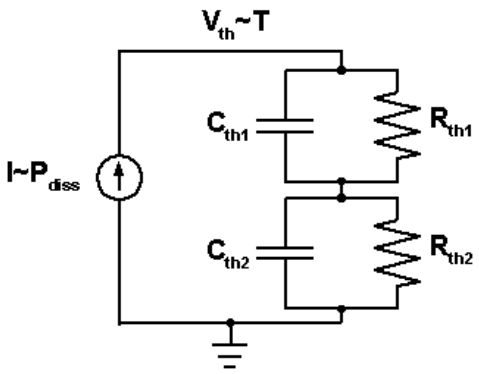

Figure 2.3: Thermal sub-circuit, representing temperature as a function of power dissipation and thermal resistance.

a thermal subcircuit with two time constants. Temperature, or rather "equivalent thermal voltage", results from the instantaneous power $P_{\mathrm{diss}} = I_{\mathrm{ds}} \cdot V_{\mathrm{ds}}$ in the device, when dissipated in a thermal resistance R_{th}.

Several model approaches to include temperature effects can be distinguished:

- In the physically intuitive approach, one or several parameters in the drain current model are a function of temperature, typically the threshold voltage $V_{\mathrm{t}}(T)$ and maximum transconductance $\beta(T)$. The correct implementation requires an additional iterative algorithm to solve for P_{diss} in the thermal circuit [60].

- The drain current model, initially a function of two terminal voltages $I_{\mathrm{ds}} = f(V_{\mathrm{gs}}, V_{\mathrm{ds}})$, uses the thermal voltage V_{th} from the sub-circuit as third voltage in calculating $I_{\mathrm{ds}} = f(V_{\mathrm{gs}}, V_{\mathrm{ds}}, V_{\mathrm{th}} = T)$, e.g. [61].

- The thermal voltage gives rise to a correction of drain current and/or the gate controlling voltage. This is implemented by additional temperature-dependent voltage- and current sources [46].

In reality, thermal conductivity is itself a temperature dependent material parameter, so R_{th} in thermal models should be a function of temperature. This, however, is not included in state-of-the-art device level models. Thermal models are used both for HFET and HBT devices [62]. Today, they are incorporated in several commercial models, e.g. the BSIMSOI model [63] and the "high current model" (HICUM) [64] for HBT transistors.

2.3.2 Static- and Dynamic Current Sources

The first dispersion models concentrated on frequency dependent output conductance in GaAs MESFET devices [65]. Under typical device operation in saturation, the dynamic output conductance is higher than the one derived from static characteristics. This is due

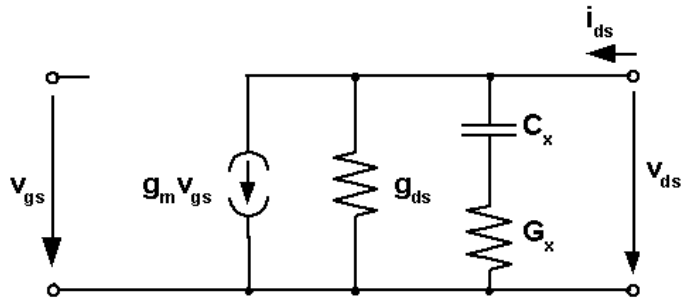

Figure 2.4: Early small-signal dispersion models describe a linear, frequency-dependent correction to output conductance (only the dispersion part of the model is shown here).

to self-heating with corner frequencies typically in the lower kHz range. A series R-C combination between drain and source achieves the observed behaviour. Fig. 2.4 shows only the dispersion part of the model topology which assumes a linear correction to dynamic output conductance, i.e. independent of bias. This approach was first proposed in [66], adopted in [67] and expanded in [68] to substrate- and buffer layer effects. Similarly, a linear dispersion correction to transconductance can be included by a series R-C combination in parallel to the source series resistor R_s [69].

A large-signal model topology which includes the voltage-dependence of dispersion as well as its impact on transconductance combines two nonlinear current sources, of which one affects only the dynamic characteristics. Fig. 2.5 shows the large-signal topology and the resulting linearised small-signal dispersion circuit. Note that the V_ds dependence of the dispersion current I_dsx gives rise to a second transconductance g_dsx in the small-signal circuit. This dispersion model topology has been built into the EE_HEMT1 model of ADS [70] and was adopted in [46, 71] as well as for GaN-based MESFETs in [72, 73].

The G_x-C_x combination serves several purposes:

- Separation of the dynamic source from the DC model via C_x
- Convergence of the model even under DC analysis via G_x.
- Determination of the dispersion time constant.

The current source I_ds0 describes static characteristics: $I_\mathrm{ds0} = I_\mathrm{ds,dc}$. Under dynamic conditions, when C_x represents a short circuit, the total drain current becomes the sum of I_ds0 and I_dsx. One therefore attributes the difference between dynamic drain current characteristics $I_\mathrm{ds,ac}$ and static ones to the dispersion source: $I_\mathrm{dsx} = I_\mathrm{ds,ac} - I_\mathrm{ds,dc}$.

This model topology offers the correct description of both static and dynamic current characteristics. Also, it has the potential of being extended to include several dispersion sources in parallel, similar to the approach described in this work. The topology shows some disadvantages, however. For instance, while being necessary for convergence, G_x introduces

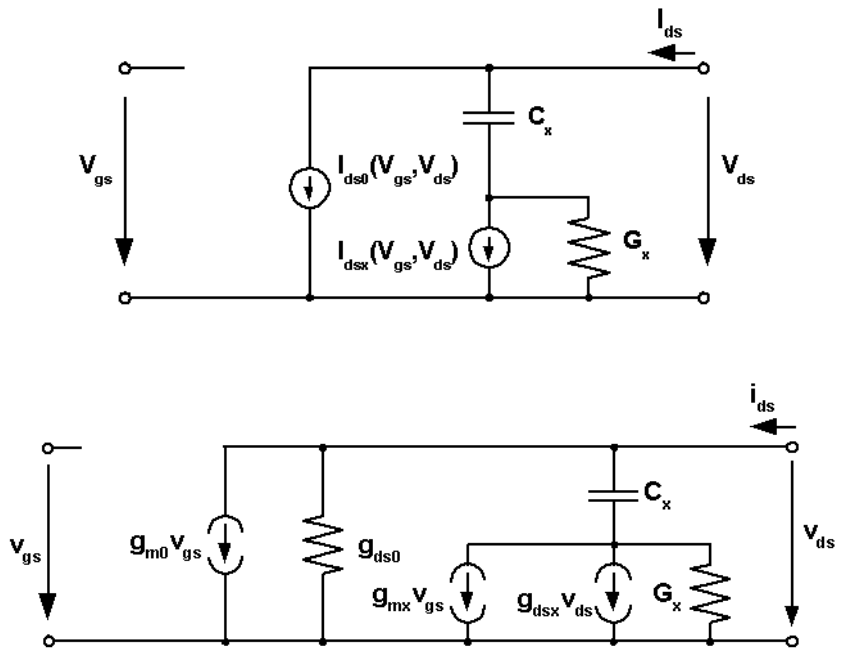

Figure 2.5: RC-type dispersion model combining a static and dynamic nonlinear drain current source. Large-signal (top) and linearised topology (bottom).

an error to output conductance. This will be discussed in more detail in chapter 3.5.2, where a comparison is drawn to the approach developed in this work.

2.3.3 Equivalent Voltage Sources

Another empirical approach to modelling dispersion is the use of equivalent voltage sources in the FET circuit topology [74]. A non-dispersive FET model is surrounded by voltage sources, e.g. at the gate and drain terminal, to correct the externally applied voltages V_{ds} and V_{gs} in a way to achieve the dynamically observed IV characteristics (Fig. 2.6).

Although this approach may accurately describe the dynamic device performance, it is neither capable of incorporating both static and dynamic models, nor will it reflect the tran-

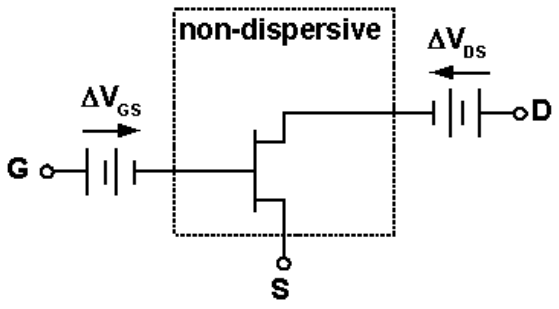

Figure 2.6: Example of an equivalent-voltage dispersion model topology.

sition between static and dynamic operation. To overcome this problem, the same group has suggested an R-C topology in [75]. A conceptionally similar approach which overcomes the transition problem uses two FET submodels separated by a capacitively coupled resistive voltage divider [76]. The difficulty of the equivalent-voltage approach lies in the determination of the correction voltages ΔV_{gs} and ΔV_{ds}, which represents an additional parameter extraction procedure. Also, no distinction is made between different dispersion effects and -time constants.

2.4 Importance of a Dispersion Model in Circuit Design

Generally, designers use in-house models or foundry design kit models in the simulation phase of circuit development. The most frequently employed models are non-dispersive such as

- **Small-signal models**, extracted from S-parameter measurements performed at microwave frequencies[1].
- Large-signal models **based on pulsed-IV characteristics** and table-based large-signal models **based on multi-bias small-signal data**.
- Large-signal models **based on DC-IV characteristics**.

The following discussion focuses on the simulation errors introduced by using non-dispersive models in the design of circuits for different applications. A quantitative investigation of the impact of dispersion on device and circuit performance is carried out for the modelled HEMT technologies of this work in chapters 3.5 and 4.

2.4.1 Static Analysis

Any kind of integrated circuit as well as any type of simulation of small- or large-signals requires a static analysis to evaluate the following:

- Bias conditions of all nonlinear elements in the circuit. In the case of HEMTs, static analysis results in the quiescent condition $Q = (V_{\mathrm{gs0}}, V_{\mathrm{ds0}})$ as well as DC currents I_{ds0} and I_{gs0}.
- Static power consumption of individual devices, stages and the full MMIC.

Obviously, only a large-signal model representing the DC-IV characteristics will give accurate results. Non-dispersive dynamic large-signal models deviate significantly. Fig. 2.7 shows the

[1] In some cases, S-parameter measurements are de-embedded and directly used as small-signal model.

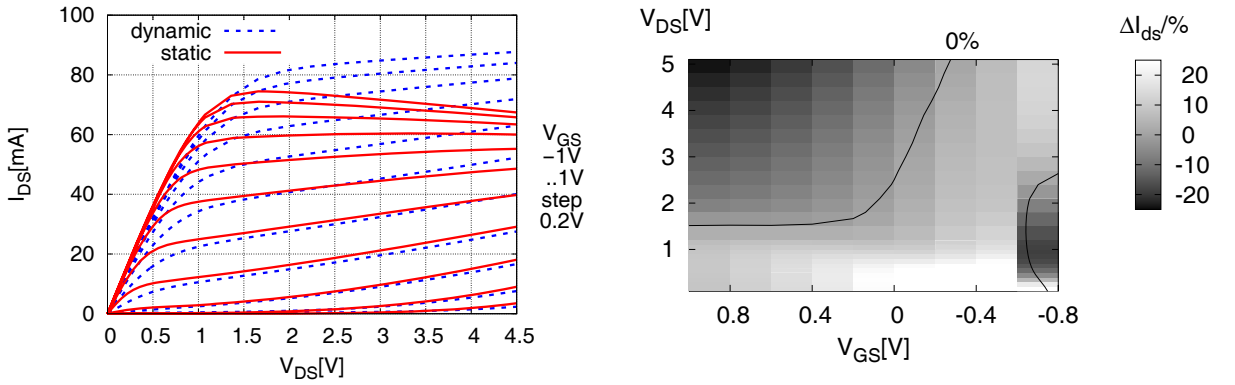

Figure 2.7: Left: Static and dynamic (obtained from $g_\mathrm{m}/g_\mathrm{ds}$ integration) drain current in a $2\,\mathrm{x}\,50\,\mu$m PH15 device. Right: Relative difference of current in percent.

purely static and purely dynamic drain current characteristics of a 2x50 μm GaAs pHEMT (PH15), as well as the relative deviation of current

$$\Delta I_\mathrm{ds} = \frac{I_\mathrm{ds,static} - I_\mathrm{ds,dynamic}}{I_\mathrm{ds,dynamic}} \tag{2.2}$$

While typical bias points like class A or -B operation will not produce significant errors in DC prediction, some applications use devices biased in the linear operating regime or in the knee region, where a deviation of more than 20 % arises. Such is the case for

- resistive FET mixers, which use the channel conductance of the device as voltage-controlled resistor,
- drain mixers, which use devices biased in the knee region, switched between linear and saturated operation by the local oscillator (LO) drive signal,
- feedback amplifiers and variable gain amplifiers (VGA), which use the FET as voltage-controlled resistor in the feedback path (such a circuit has been realised in the frame of this work and is discussed in chapter 4.2).

2.4.2 Small-Signal Circuits

In general, the major figures of merit of small-signal circuits such as low noise amplifiers (LNA) and transimpedance amplifiers (TIA) may be derived from small-signal models. The small-signal entities affected by dispersion are transconductance and output conductance. The mentioned applications typically lie well in the microwave regime, where dispersion effects do not play a role and the small-signal model will accurately predict device characteristics. The circuit designer, however, needs to be aware of the following exceptions:

- Some **ultra-broadband applications in high bit rate optical communication systems** not only require high cutoff frequencies, but simultaneously need to operate

down to very low frequencies of some kHz to accommodate the spectral components of directly modulated digital bit streams. The synchronous digital hierarchy (SDH) protocols employed in such systems require for example the detection of the 30 kHz frame synchronization pulse of synchronous transport modules (STM) [77]. In those cases, a non-dispersive small-signal model valid only at microwave frequencies will introduce errors to important criteria such as gain, output matching and the phase delay ripple evaluation at low frequencies.

- Even if no large-signal analysis is considered, a minimum requirement even in small-signal circuits will be to decide on the **bias conditions** of the nonlinear devices in the circuit. When the small-signal analysis is carried out via linearisation of a purely dynamic large-signal model, the bias conditions assumed for linearisation will be affected by the errors discussed in the previous section.

2.4.3 Large-Signal Frequency Domain Circuits

Dedicated large-signal circuits, whose characteristics are mainly investigated in the frequency domain, like power amplifiers (PA), mixers and oscillators, are concerned with general linearity and intermodulation issues. Under large-signal sinusoidal excitation (e. g. one- or two-tone input power), the output signal spectrum results from the instantaneous values of the conductive and reactive element values during one input signal cycle. Of these, trans- and output conductance are primarily affected by frequency dispersion. The error introduced to effective conductances by a purely static model is shown in Fig. 2.8 for the voltage operating plane of a $2\,\mathrm{x}\,50\,\mu$m PH15 device.

$$\Delta g_\mathrm{m} = \frac{g_\mathrm{m,static} - g_\mathrm{m,dynamic}}{g_\mathrm{m,dynamic}} \tag{2.3}$$

$$\Delta g_\mathrm{ds} = \frac{g_\mathrm{ds,static} - g_\mathrm{ds,dynamic}}{g_\mathrm{ds,dynamic}} \tag{2.4}$$

The key performance criteria affected by dispersion are

- **Gain compression**. The voltage gain G_V of a single transistor in common-source configuration in a first-order approximation at low frequencies obeys

$$G_\mathrm{V} = -g_\mathrm{m} \cdot \left(Z_\mathrm{L} || \frac{1}{g_\mathrm{ds}} \right) \tag{2.5}$$

  where Z_L is the frequency-dependent load impedance. At large input power levels, the signal will trace a path in the voltage plane which enters regions of significant deviation of both trans- and output conductance. This is shown in Fig. 2.8 for a 12 GHz, 0 dBm power signal, with the device being loaded by a $50\,\Omega$ impedance and biased for optimum gain. Major parts of the trace ellipse lie in areas where e.g. static g_m introduces an error

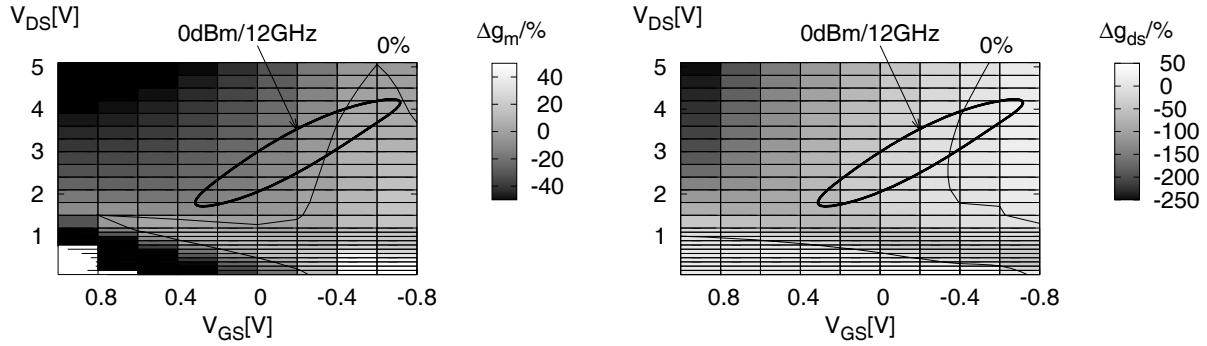

Figure 2.8: Relative difference in effective transconductance (left) and effective output conductance (right) in a $2\,\mathrm{x}\,50\,\mu$m PH15 device. The thin line signifies 0 % deviation. Trace of a 0 dBm, 12 GHz signal with $50\,\Omega$ load impedance.

of approximately 20 %. Obviously, for different bias points, higher power levels and higher frequencies (widening of ellipses) the differences become even more significant.

- Creation of **intermodulation** frequency components in the output signal spectrum, resulting from the nonlinearities in g_m and g_ds over a full cycle of the beat frequency of a multi-tone excitation.

- **Power added efficiency** (PAE), an important figure of merit in power applications, requires both accurate DC- and dynamic analysis:

$$\mathrm{PAE} = \frac{P_\mathrm{rf,out} - P_\mathrm{rf,in}}{P_\mathrm{DC}} \tag{2.6}$$

- The **self biasing effect** in nonlinear devices results from the unsymmetrical compression of the signal and a resulting DC component in the frequency spectrum. While gain compression arises in the dynamic domain, the self-biasing of course is governed by the static characteristics. Therefore, the self-biasing effect, like PAE, requires both a correct dynamic and static model.

2.4.4 Large-Signal Time Domain Circuits

Applications targeting operation in the time domain include e.g. pulsed power amplifiers as well as the multiplexers and power amplifiers in optical communication systems using time division multiplexing- and modulation schemes. The dispersive drain current characteristics show up in time domain simulations e.g. for

- **Pulse transients**. In the time domain, without a dispersion model, the drain current response to a step change in input terminal voltage is delayed by the drain current time delay τ and has an RC time constant resulting from the device's input capacitance and

its total input series resistance. This time constant will typically lie in the picosecond range (e.g. $C_{\text{in}} = 200\,\text{fF}$, $R_{\text{in}} = 5\,\Omega$) and be neglected within the transient analysis time step resolution. In reality, the step response is a superposition of several exponentially decaying functions with time constants in the micro- and millisecond range (see chapter 3.5.4).

- **Turn-on transients**. Of particular interest in pulsed amplifiers is the turn-on transient response, where mainly the self-heating effect with its relatively large associated time-constant leads to time dependent output signal characteristics.

- **Eye diagram** simulations. Evaluation of the eye diagram opening is the major figure of merit in high bit rate communication systems and their components. Here, the frequency-dependent gain characteristics of dispersive devices lead to a narrowing of the eye opening.

2.4.5 System Level

On the system level, today, an emphasis lies on highly linear amplifiers and the adoption of predistortion linearisation techniques and feedback loops in order to meet the stringent linearity demands of complex digital modulation schemes such as code division multiple access (CDMA). Linearity performance on the system level is typically evaluated via spectral regrowth and adjacent channel power ratios (ACPR) in envelope simulations and measurements.

Memory effects are defined as the general dependency of magnitude and phase distortion on the input signal or on modulation frequencies [78]. They are attributed both to frequency dependent biasing circuitry and nonlinear devices with frequency dispersion [79].

Consequences of memory effects are:

- In memoryless or quasi-memoryless systems, the amount of magnitude and phase distortion depends only on the instantaneous input signal. In systems experiencing memory effects, AM/AM and AM/PM characteristics are dependent on signal history [80].

- Third-order intermodulation products and intercept points become unsymmetrical in the lower- and upper sidebands and are dependent on tone spacing.

The inclusion of memory effects in system level design today is tackled by behavioural modelling techniques using Volterra series (e.g. [81]) and neural networks (e.g. [82]).

2.5 Obtaining Dynamic IV Characteristics

Any dispersion model relies on the description of dynamic drain current characteristics. While behavioural models typically are built on the basis of dynamic large-signal characterisation data, device level equivalent circuits use the nonlinear drain-source current source(s),

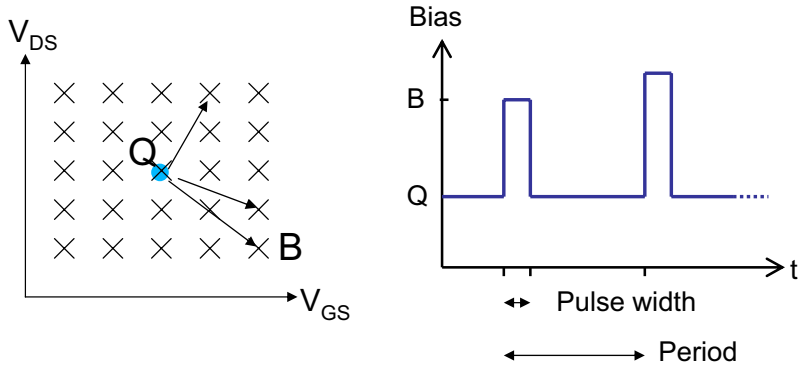

Figure 2.9: Pulsed-IV measurement principle and parameters.

whose characteristics are derived from dynamic drain current IV characteristics. Two methods are commonly employed to obtain dynamic IV characteristics: pulsed-IV and integration of dynamic trans- and output conductance. Both techniques are combined in the new dispersion modelling approach presented in this work and are briefly introduced here.

2.5.1 Pulsed-IV Characterisation

Pulsed-IV measurement systems are dedicated time domain setups to obtain dynamic drain current characteristics. Originating from a quiescent condition $Q = [V_{\mathrm{gs0}}, V_{\mathrm{ds0}}]$, short voltage pulses are applied to the device for measuring the "instantaneous" current. By sweeping both the gate- and drain voltage pulses over the whole IV plane, as illustrated in Fig. 2.9, one obtains the IV characteristics of the device under test (DUT).

Measurement parameters are

- the quiescent condition Q
- the pulse width
- the duty cycle or pulse period

With pulsed-IV measurements it is possible to eliminate the impact of those dispersion effects which have associated time constants above the minimum applicable pulse width, typically those of trapping effects and self-heating. For the small time during which the voltage pulse is applied, the dispersion state cannot change quickly enough, i.e. the device stays in the state adopted in the quiescent condition. A sufficiently large duty cycle, e.g. a 1 ms pulse period with 1 μs pulse width, ensures that the device has enough time to return to the quiescent condition in between two pulses.

Models which do not contain a dispersion part will typically be built only on characteristics obtained from a quiescent condition in a typical bias point in saturation. Such is the

case of the PH15- and PPH15 design kit models of UMS [83]. This ensures that the model reflects the static and dynamic response of a transistor used in class A amplifier configuration. Obviously, any different use of the device within a circuit topology leads to errors in both the static and dynamic model prediction.

The pulsed-IV measurement setup used in this work consists of a DIVA D225 dynamic IV analyzer from Accent Optical Technologies, capable of delivering pulses with as low as 100 ns width, in conjunction with an on-wafer prober. Several examples of pulsed-IV measurements are included in the discussion of the dispersion model in chapter 3.5.

2.5.2 Numerical Integration of Dynamic Trans- and Output Conductance

The second technique uses small-signal transconductance g_{m} and output conductance g_{ds}, derived from a multitude of bias conditions across the whole IV plane. Such data forms the direct basis of table-based spline interpolation models (e.g. [84]), where it has been shown to be capable of accurately describing dynamic device characteristics.

Linearisation of the nonlinear drain current with respect to its controlling voltages yields g_{m} and g_{ds}:

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{gs}}} \tag{2.7}$$

$$g_{\mathrm{ds}} = \frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{ds}}} \tag{2.8}$$

In other words, g_{m} and g_{ds} form the gradient of the drain current as a function of V_{gs} and V_{ds}:

$$\bigtriangledown I_{\mathrm{ds}}(V_{\mathrm{gs}}, V_{\mathrm{ds}}) = \begin{pmatrix} g_{\mathrm{m}}(V_{\mathrm{gs}}, V_{\mathrm{ds}}) \\ g_{ds}(V_{\mathrm{gs}}, V_{\mathrm{ds}}) \end{pmatrix} \tag{2.9}$$

The nonlinear, dynamic current-voltage characteristics can therefore, in principle, be rebuilt from integrating the nonlinear, dynamic trans- and output conductances. The latter can be extracted from the linear twoport parameters of the device at the respective bias conditions. At low and moderate frequencies, where the influence of reactive device components is negligible compared to the real components, transconductance g_{m} and output conductance g_{ds} may be obtained from the device's Y-parameters[2] via

$$g_{\mathrm{m}} = \Re\{Y_{21}\} \tag{2.10}$$

$$g_{\mathrm{ds}} = \Re\{Y_{22}\} \tag{2.11}$$

At microwave frequencies, considering a full, eight-element, small-signal FET equivalent circuit, trans- and output conductance become a function of the other Y-parameters as

[2]internal Y-parameters, obtained from subtracting the influence of pad parasitics and series resistance from the measured S-parameters, see chapter 3.3.

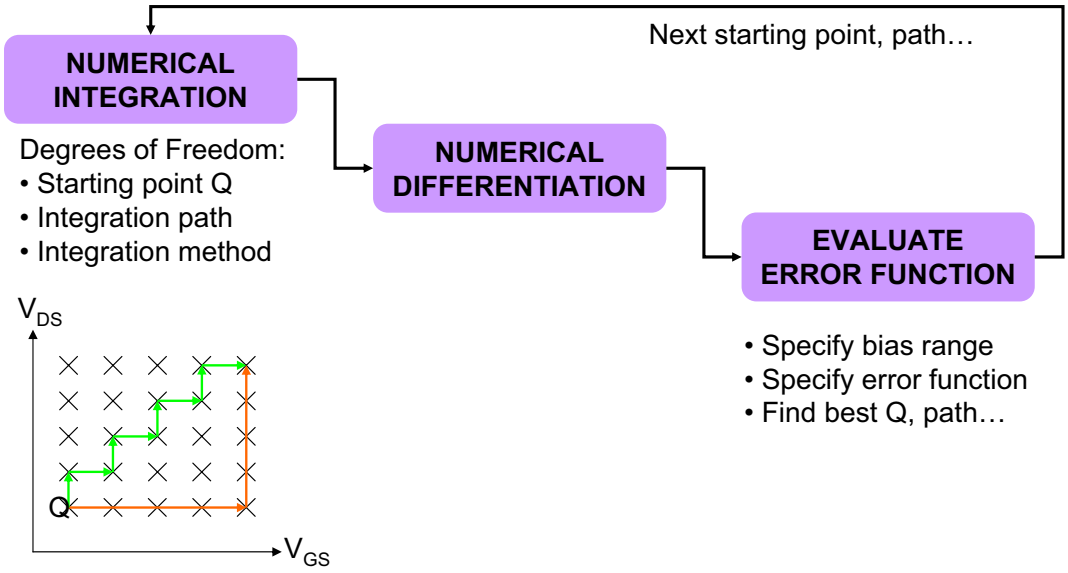

Figure 2.10: Algorithm for obtaining dynamic IV characteristics from numerical integration of g_m and g_ds.

well [85] (see Appendix A and chapter 3.3). Performing this extraction for a whole matrix of bias conditions yields the right side in equation (2.9). Provided integrability of the obtained trans- and output conductances, i.e. if g_m and g_ds fulfil equation (2.9), the current at voltage V_gs and V_ds may be found by

$$I_\mathrm{ds}\left(V_\mathrm{gs}, V_\mathrm{ds}\right) = I_\mathrm{ds}\left(V_\mathrm{gs0}, V_\mathrm{ds0}\right) + \int_{V_\mathrm{gs0}}^{V_\mathrm{gs}} g_\mathrm{m}\left(\xi, V_\mathrm{ds0}\right)\partial\xi + \int_{V_\mathrm{ds0}}^{V_\mathrm{ds}} g_\mathrm{ds}\left(V_\mathrm{gs0}, \eta\right)\partial\eta \tag{2.12}$$

where $(V_\mathrm{gs0}, V_\mathrm{ds0})$ is the quiescent voltage condition, from which the integration originates. Since $g_\mathrm{m}\left(V_\mathrm{gs}, V_\mathrm{ds}\right)$ and $g_\mathrm{ds}\left(V_\mathrm{gs}, V_\mathrm{ds}\right)$ have been obtained independently, however, (2.9) will not necessarily be satisfied, and the integration becomes path dependent. In analogy to the charge conservation problematic discussed in chapter 3.4.1, the path dependence signifies that the vector field (g_m, g_ds) is non-conservative, i.e. does not derive from a scalar current function I_ds [86]. An optimum I_ds therefore needs to be found, which best fits the extracted g_m and g_ds when linearised.

Integration of dynamic g_m and g_ds data in the development of nonlinear models is applied frequently (e.g. [87][46]). The numerical integration sequence adopted in this work follows the scheme depicted in Fig. 2.10. For obtaining the nonlinear dynamic IV characteristics from multi-bias small-signal information the following steps are undertaken:

1. Numerical Integration

The following degrees of freedom can be distinguished in the process:

- Starting point

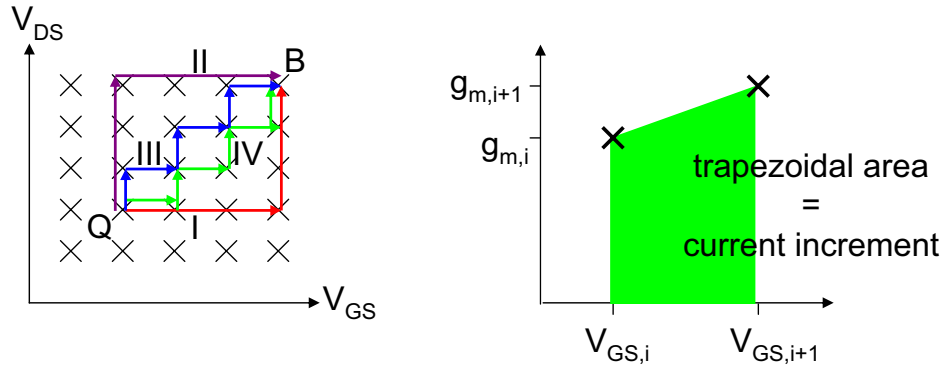

Figure 2.11: Numerical integration of g_{m} and g_{ds}. (a) integration path possibilities, (b) trapezoidal rule.

The integration process can originate from different starting points. The current constant is chosen to be the static current. The starting point of the integration therefore represents the quiescent point Q, similar to the quiescent condition during pulsed-IV characterisation.

$$I_{\mathrm{ds,ac}}|_Q = I_{\mathrm{ds,dc}}|_Q \tag{2.13}$$

- Integration path
  The integrated current value at a particular voltage condition may be found by integrating g_{m} and g_{ds} via different integration paths. Fig. 2.11(a) shows the four different paths used in minimizing the error function.
  I: first integrate g_{m} along constant V_{ds}, then integrate g_{ds}.
  II: first integrate g_{ds} along constant V_{gs}, then integrate g_{m}.
  III: integrate one step in g_{ds}, then one step in g_{m}.
  IV: integrate one step in g_{m}, then one step in g_{ds}.

- Integration method
  Numerical integration is carried out by introducing Lagrange interpolation polynoms to the tabulated values of g_{m} or g_{ds}, resulting in quadrature formulas. The basic two-point quadrature formula is called the trapezoidal rule. For integration of g_{m} along constant V_{ds}, for instance, the drain current value is evaluated as

$$I_{\mathrm{ds},i+1} = I_{\mathrm{ds},i} + \frac{1}{2}\left(g_{\mathrm{m},i+1} + g_{\mathrm{m},i}\right)\left(V_{\mathrm{gs},i+1} - V_{\mathrm{gs},i}\right) \tag{2.14}$$

  as illustrated in Fig. 2.11(b). Integration of g_{ds} is carried out accordingly.

2. Numerical Differentiation

The partial derivatives of the nonlinear current obtained from the integration process are evaluated numerically by calculating

$$\left.\frac{\Delta I_{\mathrm{ds}}\left(V_{\mathrm{gs}}, V_{\mathrm{ds}}\right)}{\Delta V_{\mathrm{gs}}}\right|_{V_{\mathrm{ds}}=\mathrm{const.}} \tag{2.15}$$

$$\left.\frac{\Delta I_{\mathrm{ds}}\left(V_{\mathrm{gs}}, V_{\mathrm{ds}}\right)}{\Delta V_{\mathrm{ds}}}\right|_{V_{\mathrm{gs}}=\mathrm{const.}} \tag{2.16}$$

3. Error Function Evaluation

The differentiated values can now be compared to the original dynamic trans- and output conductance at every bias condition by evaluating either the total or relative deviation. A similar approach was introduced in [88]. Here, the Gaussian error, i.e. the quadratic relative deviation, is taken into account:

$$\Delta_{\mathrm{m}}^2 = \left(\frac{\frac{\Delta I_{\mathrm{ds}}}{\Delta V_{\mathrm{gs}}} - g_{\mathrm{m}}}{g_{\mathrm{m}}}\right)^2 \tag{2.17}$$

$$\Delta_{\mathrm{ds}}^2 = \left(\frac{\frac{\Delta I_{\mathrm{ds}}}{\Delta V_{\mathrm{ds}}} - g_{\mathrm{ds}}}{g_{\mathrm{ds}}}\right)^2 \tag{2.18}$$

The deviation at a single bias condition can be defined by introducing weights to the individual errors in trans- and output conductance:

$$\Delta^2 = w_{\mathrm{m}} \cdot \Delta_{\mathrm{m}}^2 + w_{\mathrm{ds}} \cdot \Delta_{\mathrm{ds}}^2 \tag{2.19}$$

The value of the error function of a particular integration method is obtained by summing up all single-bias deviations within a specified bias range A:

$$E = \sum_{A} \Delta^2 \tag{2.20}$$

The algorithm iterates all four integration paths in all possible quiescent conditions and finds the combination where E is at its minimum. Fig. 2.12 shows an example of numerical integration of the dynamic g_{m} and g_{ds} of a $2\,\mathrm{x}\,50\,\mu$m strained-Si/SiGe mHEMT. Extraction parameters are $w_{\mathrm{m}} = 1$, $w_{\mathrm{ds}} = 0.5$. Optimised bias range is $V_{\mathrm{gs}} = -0.5...0.3\,V$ and $V_{\mathrm{ds}} = 0.1...2.6\,V$. The optimum quiescent point for integration was $V_{\mathrm{gs}} = -0.3\,V$ and $V_{\mathrm{ds}} = 1.0\,V$. The best integration path was number III in Fig. 2.11.

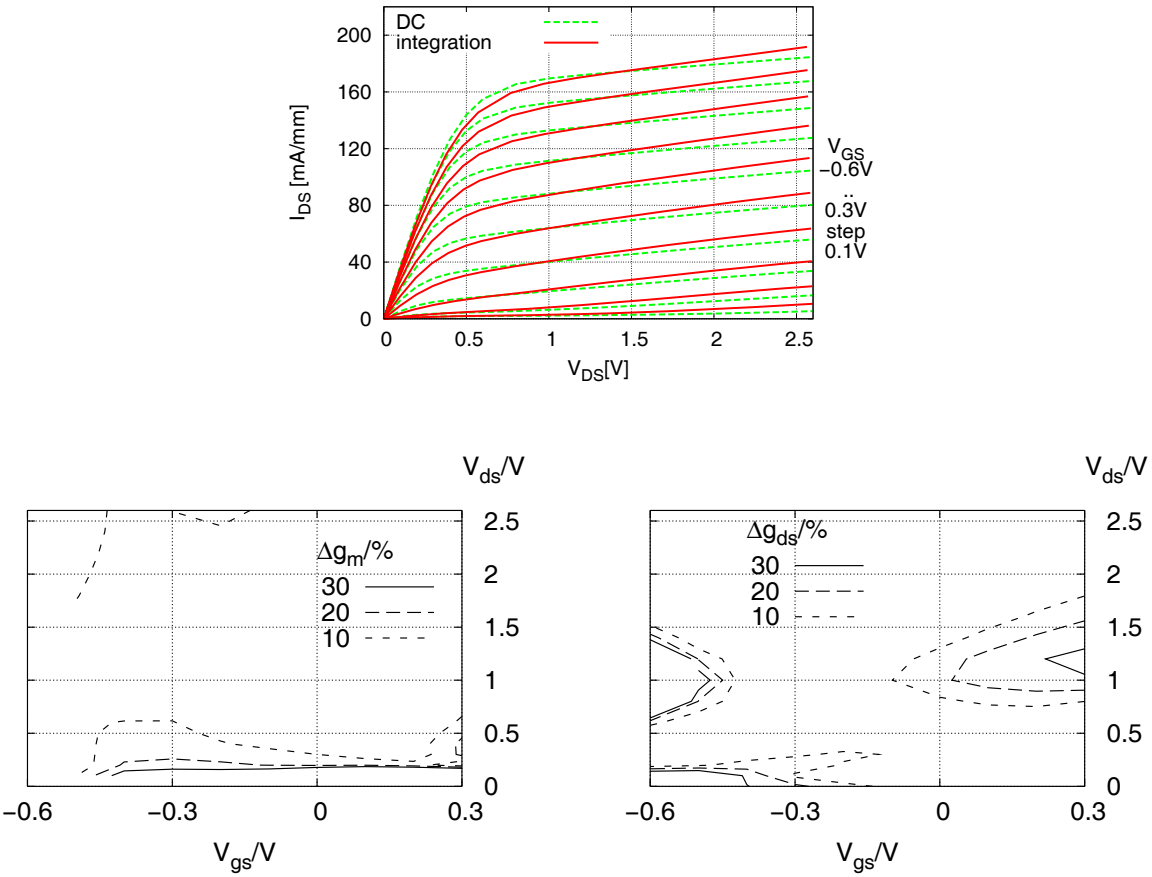

Figure 2.12: Example of numerical g_m/g_{ds} integration for obtaining nonlinear dynamic IV characteristics of a $2\,\mathrm{x}\,50\,\mu$m strained-Si/SiGe mHEMT. Dynamic IV compared to static curves (top). Global deviation of g_m (bottom left), global deviation of g_{ds} (bottom right) of dynamic IV relative to measured g_m and g_{ds}, respectively.

Chapter 3

Universal Large-Signal HFET Model

This chapter describes the full large-signal models for the SiGe-, InP- and GaAs HEMTs, progressing from the model topology and its static and dynamic nonlinear functions to the parameter extraction procedure, implementation into a CAD simulation environment and, finally, model verification in a comparison to measurements.

An efficient, analytical model expression is adopted for both static and dynamic drain current nonlinearities and modified to include particularities of HFET characteristics.

A unified approach to charge-conservative capacitance modelling is introduced and novel capacitance expressions are developed and applied to the different technologies. A new theory for the modelling of multiple time constant frequency dispersion is introduced and applied. Both components constitute the dynamic nonlinear model part and are incorporated into a complete HFET equivalent circuit topology.

3.1 Advanced De-embedding Technique

The term "de-embedding" denotes the determination of parasitic electrical characteristics of layout elements in the periphery of the core FET device and the analytical reduction of measurement data by the influence of the embedding network. In on-wafer modelling transistors, the embedding network typically consists of coplanar contact pad structures (see e.g. Fig. 1.6). A distinction needs to be made as to what the "core" device represents. In modelling, the core device typically signifies the active FET region, i.e. the channel region below the gate, denoted "intrinsic FET" in Fig. 3.1. The final model used in circuit design, however, will need to include the contact parasitics of the gate-, drain- and source regions, represented by a series L-R combination ("extrinsic FET").

Parasitic effects of the embedding network are pad capacitance to ground as well as series inductance and resistance of both the pad structure and the terminal contacts[1]. In standard de-embedding techniques, no distinction is made in the embedding network between elements external and internal to the extrinsic FET device. The advanced de-embedding network used

[1] In Si-based devices, the de-embedding network typically contains additional elements, such as a resistance in series to the pad capacitors to account for the conductive substrate.

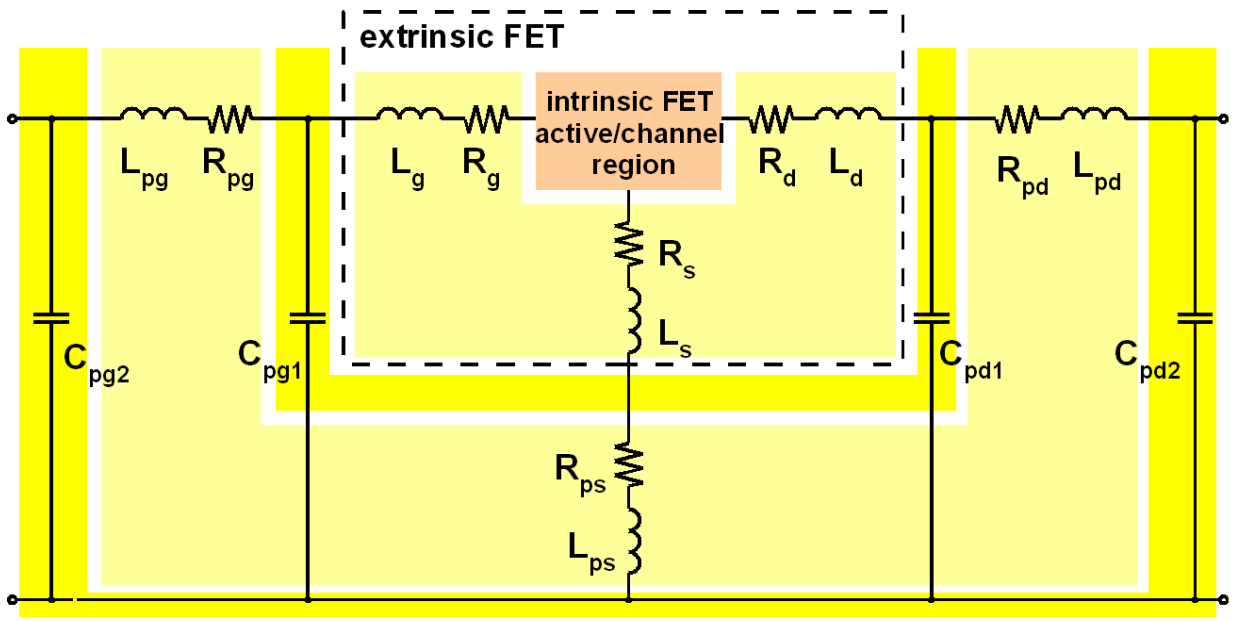

Figure 3.1: Advanced de-embedding network.

in this work overcomes this drawback (Fig. 3.1). It separates both the series inductance and resistance of each terminal into the pad structure and the extrinsic FET. Additionally, gate- and drain pad capacitors are included as π-type networks in an approximation of the distributed nature of the pad structures. Conveniently, terminal inductance, resistance and capacitance are represented in terms of total value and separation ratio:

$$L_{\mathrm{x}} = L_{\mathrm{pxt}} \cdot l_{\mathrm{pxq}} \qquad L_{\mathrm{px}} = L_{\mathrm{pxt}} \cdot (1 - l_{\mathrm{pxq}}) \tag{3.1}$$

$$R_{\mathrm{x}} = R_{\mathrm{pxt}} \cdot r_{\mathrm{pxq}} \qquad R_{\mathrm{px}} = R_{\mathrm{pxt}} \cdot (1 - r_{\mathrm{pxq}}) \tag{3.2}$$

$$C_{\mathrm{px1}} = C_{\mathrm{pxt}} \cdot c_{\mathrm{pxq}} \qquad C_{\mathrm{px2}} = C_{\mathrm{pxt}} \cdot (1 - c_{\mathrm{pxq}}) \tag{3.3}$$

where indices x represent gate-, drain- and source terminals, indices t denote total inductance, resistance and capacitance, p the pad part, and indices q denote separation ratios.

Several techniques allow for the determination of embedding network elements. If available, special on-wafer SHORT and OPEN structures will yield the pad series- and parallel elements C_{pxt}, L_{px} and R_{px}. No information is obtained for the elements embodied in the extrinsic FET. The so-called "cold FET" method uses a transistor biased below threshold and at $V_{\mathrm{ds}} = 0\,\mathrm{V}$ to obtain pad capacitance C_{pxt} from the Y-parameters of the resulting parallel capacitance equivalent circuit [89]. DC gate current- and Z-parameters of a FET biased under forward gate conduction and at $V_{\mathrm{ds}} = 0\,\mathrm{V}$ are used to obtain total series inductance L_{xt} and total series resistance R_{xt} of all terminals from the corresponding series R-L equivalent circuit [89, 90]. If no OPEN and SHORT structures are available during model extraction, the separation between pad- and extrinsic FET contribution to inductance and

resistance as well as the pad capacitance ratios need to be chosen based on a consideration of the physical pad layout or based on careful tuning of the ratios c_{pxq}, l_{xq} and r_{xq}.

Once all values of the embedding network elements have been found, the following de-embedding algorithm, similar to the approach taken in [89], allows for the bias-independent correction of measured S-parameters to the core device reference plane:

$$[S] \overset{S}{\underset{Y}{\rightarrow}} \begin{array}{c} Y'_{11} = Y_{11} - j\omega C_{\mathrm{pg2}} \\ Y'_{12} = Y_{12} \\ Y'_{21} = Y_{21} \\ Y'_{22} = Y_{22} - j\omega C_{\mathrm{pd2}} \end{array} \overset{Y}{\underset{Z}{\rightarrow}} \begin{array}{c} Z'_{11} = Z_{11} - (R_{\mathrm{pg}} + R_{\mathrm{ps}}) - j\omega\,(L_{\mathrm{pg}} + L_{\mathrm{ps}}) \\ Z'_{12} = Z_{12} - R_{\mathrm{ps}} - j\omega L_{\mathrm{ps}} \\ Z'_{21} = Z_{21} - R_{\mathrm{ps}} - j\omega L_{\mathrm{ps}} \\ Z'_{22} = Z_{22} - (R_{\mathrm{pd}} + R_{\mathrm{ps}}) - j\omega\,(L_{\mathrm{pd}} + L_{\mathrm{ps}}) \end{array} \tag{3.4}$$

$$\overset{Z}{\underset{Y}{\rightarrow}} \begin{array}{c} Y'_{11} = Y_{11} - j\omega C_{\mathrm{pg1}} \\ Y'_{12} = Y_{12} \\ Y'_{21} = Y_{21} \\ Y'_{22} = Y_{22} - j\omega C_{\mathrm{pd1}} \end{array} \overset{Y}{\underset{Z}{\rightarrow}} \begin{array}{c} Z'_{11} = Z_{11} - (R_{\mathrm{g}} + R_{\mathrm{s}}) - j\omega\,(L_{\mathrm{g}} + L_{\mathrm{s}}) \\ Z'_{12} = Z_{12} - R_{\mathrm{s}} - j\omega L_{\mathrm{s}} \\ Z'_{21} = Z_{21} - R_{\mathrm{s}} - j\omega L_{\mathrm{s}} \\ Z'_{22} = Z_{22} - (R_{\mathrm{d}} + R_{\mathrm{s}}) - j\omega\,(L_{\mathrm{d}} + L_{\mathrm{s}}) \end{array} \overset{Z}{\underset{Y}{\rightarrow}} [Y_{\mathrm{i}}] \tag{3.5}$$

Here, $[S]$ is the measured S-parameter matrix, $[Y_{\mathrm{i}}]$ are the core FET (internal) Y-parameters and $\overset{S}{\underset{Y}{\rightarrow}}$ represents a transformation of **S- to Y**-parameters [91]. The correction sequence is illustrated in Fig. 3.1, where the corresponding subtraction layers are indicated by embedding blocks. This algorithm has been implemented in the parameter extraction software FETfit (chapter 3.6) and was adopted in the modelling phase of all presented HFET devices.

Note on Series Resistance and Bias Networks

Special importance has to be paid to series resistance in the FET terminals, i.e. R_{gt}, R_{dt} and R_{st}. Any static gate- and drain current will introduce a voltage drop across these resistors and reduce the static intrinsic junction voltages V_{gsi} and V_{dsi} compared to the externally applied voltages V_{gs} and V_{ds} by some amount (compare Fig. 3.3):

$$V_{\mathrm{dsi}} = V_{\mathrm{ds}} - I_{\mathrm{gs}} \cdot R_{\mathrm{st}} - I_{\mathrm{ds}} \cdot (R_{\mathrm{st}} + R_{\mathrm{dt}}) \tag{3.6}$$

$$V_{\mathrm{gsi}} = V_{\mathrm{gs}} - I_{\mathrm{gs}} \cdot (R_{\mathrm{gt}} + R_{\mathrm{st}}) - I_{\mathrm{ds}} \cdot R_{\mathrm{st}} \tag{3.7}$$

In case of R_{s}, the (output) drain current introduces a voltage drop that reduces the (input) controlling voltage V_{gsi} and therefore introduces negative feedback. The nonlinear drain current is controlled by the internal voltages:

$$I_{\mathrm{ds}}(V_{\mathrm{gsi}}, V_{\mathrm{dsi}}) \tag{3.8}$$

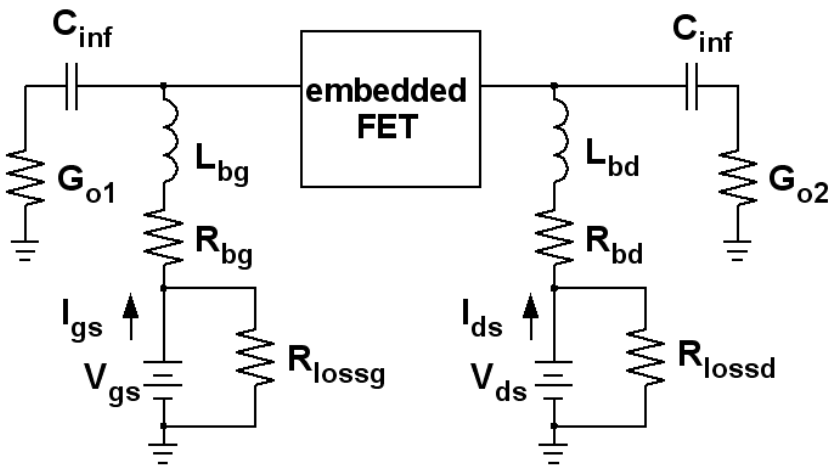

Figure 3.2: Parasitic bias network elements.

The small-signal trans- and output conductance, obtained from linearisation of the drain current are

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{gsi}}} \tag{3.9}$$

$$g_{\mathrm{ds}} = \frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{dsi}}} \tag{3.10}$$

Externally, one measures effective trans- and output conductance. These are related to the intrinsic values by

$$g_{\mathrm{m,eff}} = \frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{gs}}} = \frac{g_{\mathrm{m}}}{1 + g_{\mathrm{m}} R_{\mathrm{st}} + g_{\mathrm{ds}} \left(R_{\mathrm{st}} + R_{\mathrm{dt}}\right)} \tag{3.11}$$

$$g_{\mathrm{de,eff}} = \frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{ds}}} = \frac{g_{\mathrm{ds}}}{1 + g_{\mathrm{ds}} \left(R_{\mathrm{st}} + R_{\mathrm{dt}}\right) + g_{\mathrm{m}} R_{\mathrm{st}}} \tag{3.12}$$

During the de-embedding process, the value of R_{gt} will also be obtained. If the transistor is operated under normal conditions, i.e. with reverse bias of the gate diodes, the influence of R_{gt} on the static characteristics is negligible, because only the gate leakage current is flowing in that case. R_{gt} is a crucial element, however, when it comes to modelling the dynamic device characteristics since it introduces attenuation to any dynamic signal. Despite having no influence on the transition frequency f_{T} of the device, R_{gt} enters into the calculation of f_{max} [92, 32].

Parasitic series resistance arises not only in the device, but may also occur in the measurement setup used to obtain static or dynamic characteristics. External sources of series resistance include for example the bias-T's in an S-parameter measurement setup, non-ideal voltage sources or resistive cable- and adapter losses. The de-embedding network in Fig. 3.1 therefore needs to be extended, taking into account additional losses in the bias network. The full bias network is shown in Fig. 3.2, where all external series losses are included in

resistors R_{bg} and R_{bd}. Terminations G_{o1} and G_{o2} describe the 50 Ω dynamic environment, capacitors and inductors allow for a lower cutoff frequency of the bias-T's, while resistors R_{lossg} and R_{lossd} describe parallel current loss in the bias network.

In characterisation systems dedicated to accurate IV measurements (e.g. static and pulsed-IV systems), series losses may generally be neglected. However, typical values of R_{bg} and R_{bd} may reach 2 Ω in an S-parameter measurement environment. Although they don't affect the dynamic measurement, voltage drops occurring in the bias network will introduce an additional difference between the applied voltages and those resulting at the device terminals. In DC analysis, the total series resistance therefore becomes

$$R_{\mathrm{gt}}^{'} = R_{\mathrm{gt}} + R_{\mathrm{bg}} \tag{3.13}$$

$$R_{\mathrm{dt}}^{'} = R_{\mathrm{dt}} + R_{\mathrm{bd}} \tag{3.14}$$

Since all static and dynamic nonlinear model elements are functions of the intrinsic terminal voltages, an accurate knowledge of all series resistors in the equivalent circuit is crucial to the development of accurate device models. Especially in devices carrying large currents, the inclusion of R_{bd} is of particular importance.

3.2 Static Model

Fig. 3.3 shows the full DC model topology, i.e. all reactive components and model branches are omitted. The static model consists of the main drain-source nonlinear current source I_{ds}, Schottky gate diodes D_{gs} and D_{gd}, and the series resistors R_{g}, R_{d} and R_{s}, arising from resistance of the ohmic contacts and sheet resistance of the drain and source implant areas as well as the gate contact metal.

The static model part is essential for accurate prediction of power consumption in MMICs, which also enters into important figures of merit like power added efficiency. Of equal importance is the accurate simulation of biasing conditions in the MMIC, allowing for the reliable design and optimisation of biasing circuits as well as the usage of self-biasing concepts.

3.2.1 Modified COBRA drain current model

Many different model expressions have been developed for the description of nonlinear drain current characteristics in HFETs. Among the most popular analytical expressions are the Curtice-Ettenberg [93], Angelov/Chalmers [94] and Tajima [95] models. Mostly, such models are based on the empirical Curtice model approach which combines a description of the saturated current with a $\tanh(x)$ function to include the linear operating regime of the transistor [96].

In this work, the "COBRA" expression [97] is employed. The original model equation has been developed by Dr. V. Cojocaru and Prof. T.J. Brazil at University College Dublin, hence

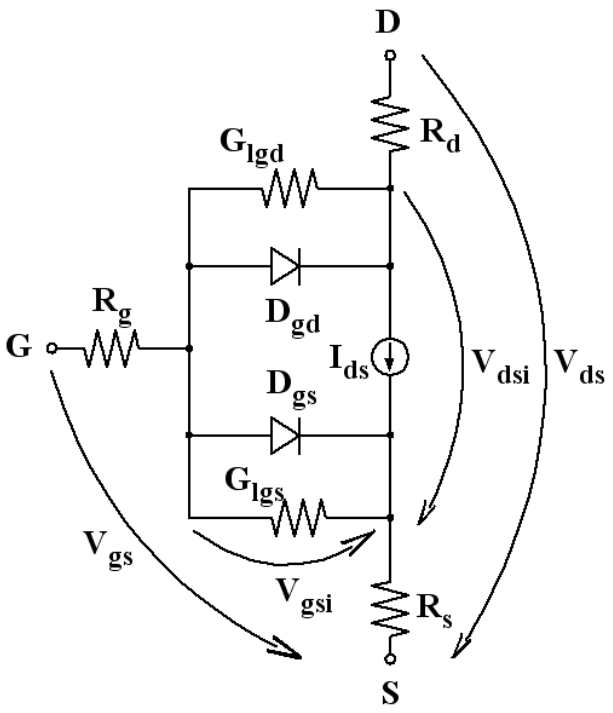

Figure 3.3: Static HFET model topology including nonlinear gate- and drain current elements.

its name. While being conceptionally simple and computationally efficient, this empirical model proves to be very well suited to describe the characteristics of all HFET devices investigated in this work. It is capable of describing typical current nonlinearities like transconductance compression and onset of impact ionisation current. Many aspects of this model recommend it for use in the development of a FET model dedicated to circuit simulation:

- The model uses a single analytical expression to describe drain current characteristics in all operating regimes, i.e. a single expression is used over the whole IV plane. Global continuity of the current expression together with its partial derivatives to infinite orders allows for excellent convergence behaviour even under strong nonlinear operation.

- The modified expression employed here uses a total of only eleven parameters. This results in reduced complexity and the possibility of direct parameter extraction combined with efficient numerical optimisation.

- Although being of empirical nature (the mathematical topology backbone is the Curtice model), most parameters of the model can be linked to physical effects in the device, such as threshold voltage, gain, gain compression etc.

The original expression from [97] has been modified in this work to allow for a more general description of gain compression. The new, modified current expression is

$$I_{\mathrm{ds}} = \beta \cdot V_{\mathrm{eff}}^{\frac{\lambda}{1+\mu V_{\mathrm{ds}}^2+\xi V_{\mathrm{eff2}}^{\eta}}} \cdot \tanh\left(\alpha V_{\mathrm{ds}}\left(1+\zeta V_{\mathrm{eff}}\right)\right) \tag{3.15}$$

$$V_{\mathrm{eff}} = \frac{1}{2}\left(V_{\mathrm{gs}} - V_{\mathrm{t1}} + \sqrt{\left(V_{\mathrm{gs}} - V_{\mathrm{t1}}\right)^2 + \delta^2}\right) \tag{3.16}$$

$$V_{\mathrm{t1}} = \left(1+\beta^2\right) V_{\mathrm{to}} - \gamma V_{\mathrm{ds}} \tag{3.17}$$

$$V_{\mathrm{eff2}} = \frac{1}{2}\left(V_{\mathrm{gs}} - V_{\mathrm{t2}} + \sqrt{\left(V_{\mathrm{gs}} - V_{\mathrm{t2}}\right)^2 + \delta^2}\right) \tag{3.18}$$

$$V_{\mathrm{t2}} = \left(1+\beta^2\right) V_{\mathrm{to}} \tag{3.19}$$

In (3.15), the term responsible for gain compression is in the numerator of the exponential current term: $\xi V_{\mathrm{eff2}}^{\eta}$. For positive ξ and V_{eff2}, this term introduces a decrease in current with increasing gate-source voltage. The additional parameter η allows for a nonlinear influence of the gate-source voltage on the exponential expression. At the same time, complexity may be reduced by changing from V_{eff}, which has a V_{ds}-dependence attached to it via parameter γ, to the simple effective gate overtravel V_{eff2}.[2]

In GaAs-based devices, due to the low thermal conductivity of the substrate, the thermal effect on static IV characteristics plays an important role, especially for large transistors with relatively high power dissipation. A second modification has been introduced in the COBRA current expression to account for self-heating under static and very low frequency conditions, using a simple but sufficiently accurate approach [52]:

$$I_{\mathrm{ds}} = \frac{I_{\mathrm{ds}'}}{1 + \pi_{\mathrm{eff}} I_{\mathrm{ds}'} V_{\mathrm{ds}}} \tag{3.20}$$

In this equation, $I_{\mathrm{ds}'}$ denotes the current of the original COBRA model. Since temperature is not a model parameter in the approach taken in this work, the power scaling parameter π_{eff} has to be extracted from measurements. It can be found by extracting the COBRA expression for devices with very small total gate periphery, where current reduction due to self-heating may be neglected and π_{eff} has no significant impact. Applying this parameter set to larger devices using linear scaling, one can then extract π_{eff} to describe the current reduction at higher static power levels. That way, the model becomes scalable with respect to gate width. For modelling of dynamic, isothermal IV characteristics, π_{eff} is set to zero.

With these modifications, the COBRA model can be employed to describe both DC- and dynamic IV characteristics of all investigated HEMT transistors. For model implementation (see chapter 3.7), the analytic formulations of transconductance g_{m} and output conductance g_{ds}, i.e. the partial derivatives of the drain current expression with respect to the terminal

[2] V_{eff}, the gate "overtravel", is the basis of the overall saturation current. Its calculation is done in a way to assure continuous derivatives while offering a function to give $V_{\mathrm{eff}} \approx 0V$ for $V_{\mathrm{gs}} < V_{\mathrm{t1}}$, but $V_{\mathrm{eff}} \approx V_{\mathrm{gs}} - V_{\mathrm{t1}}$ for $V_{\mathrm{gs}} > V_{\mathrm{t1}}$.

Parameter	Unit	Description
α	V^{-1}	linear regime, voltage-controlled resistor operation of the FET device
β	S	maximum transconductance, multiplied by the effective gate voltage V_{eff}.
γ	1	output conductance, obtained by introducing a V_{ds}-dependence to V_{eff}.
δ	V	deviation from "square-law" in device transmission characteristics. Numerical purpose: keep V_{eff} from becoming zero.
ζ	V^{-1}	introduces V_{gs}-dependence to α, i.e. allows for additional V_{gs}-dependence of the channel resistance under non-saturated conditions $V_{ds} < V_k$.
λ	1	deviation from "square-law" in device transmission characteristics
μ	V^{-2}	onset of impact ionization- or breakthrough current, occurring at high drain potentials
ξ	V^{-1}	main g_m-compression parameter. Reduction of saturation current with increasing gate potential (formation of parasitic MESFET channel with reduced carrier mobility and saturation velocity).
η	1	g_m- compression
V_{to}	V	threshold voltage for small V_{ds}, i.e. in the linear operating regime
π_{eff}	W^{-1}	power dissipation scaling factor

Table 3.1: COBRA model parameters and their physical signification.

voltages are required. These expressions are listed in the complete model equation listing in Appendix B.

Table 3.1 lists the COBRA parameters and describes their physical link.

In the following, application of the modified COBRA model is presented for selected cases in order to highlight its particular suitability for HFETs as well as to demonstrate the significance of the modifications to the original model expression. Detailed drain current models (transfer- and output characteristics) including the model parameter values for all technologies investigated in this work are presented in Appendix C.

Self-heating

Parameter π_{eff}, which describes current reduction due to self-heating, allows for static current scaling (see scaling model in Appendix B). Fig. 3.4 shows static output characteristics of a $2\,\mathrm{x}\,20\,\mu$m GaAs PPH15 pHEMT, with the drain-source voltage ranging from the linear operating regime to the onset of drain-source breakthrough due to impact ionisation. The controlling gate-source voltage is swept from sub-threshold to the onset of gate conduction,

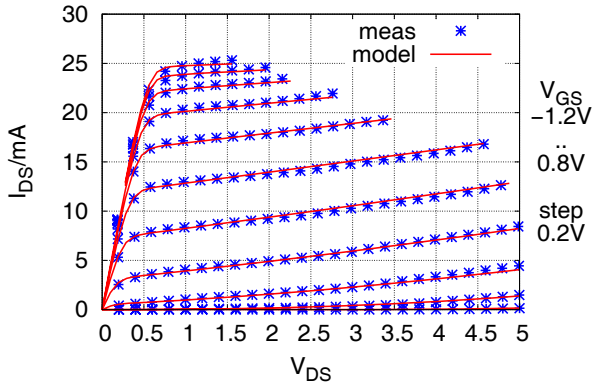

Figure 3.4: Static drain current output characteristics of a $2\,\mathrm{x}\,20\,\mu$m GaAs PPH15 pHEMT (dots) and application of the modified COBRA model (lines).

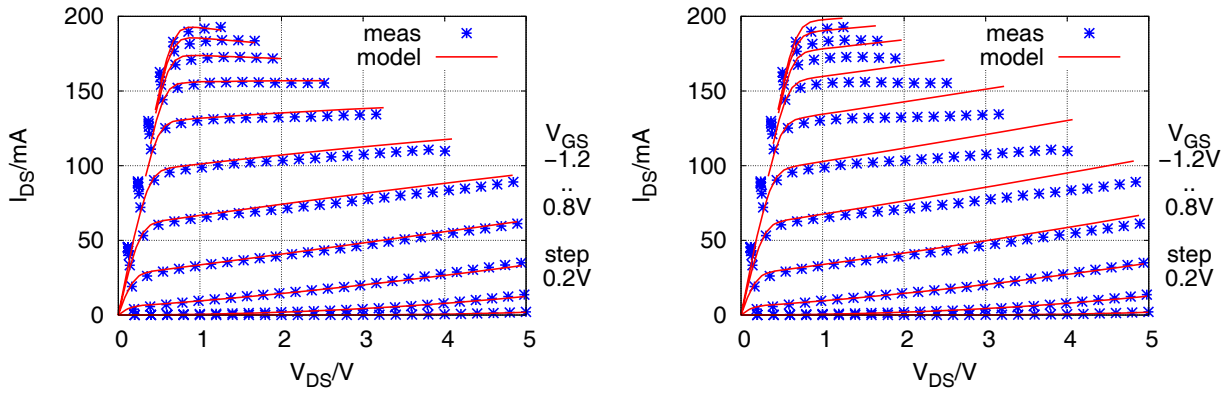

Figure 3.5: Application of the modified COBRA model to a $4\,\mathrm{x}\,75\,\mu$m device using linear current scaling of the $2\,\mathrm{x}\,20\,\mu$m parameter set. (left) using $\pi_{\mathrm{eff}} = 0.28$. (right) using $\pi_{\mathrm{eff}} = 0$.

thus covering the full range of transistor operation.

Applying a linear scaling model and the same set of model parameters to a much larger device ($4\,\mathrm{x}\,75\,\mu$m) shows the impact of self-heating on drain current (Fig. 3.5, left). One can clearly observe the thermal dispersion effect, which produces a reduction in current at high static power levels $P_{\mathrm{dc}} = I_{\mathrm{ds}} \cdot V_{\mathrm{ds}}$ due to self-heating of the device. This effect is accurately modelled by the introduction of (3.20) with a value of $\pi_{\mathrm{eff}} = 0.28$. The deviation between modelled and measured current at extremely high power levels (e.g. $V_{\mathrm{gs}} = -0.2\,\mathrm{V}$ and $V_{\mathrm{ds}} > 3.5\,\mathrm{V}$ in Fig. 3.5, left) indicates the missing temperature dependence of the employed self-heating formulation of equation (3.20). Neglecting self-heating by using $\pi_{\mathrm{eff}} = 0$ (Fig. 3.5, right) leads to a significant error in static current of large devices even under typical class A operating conditions. The static model is thus verified for a scaling range between $2\,\mathrm{x}\,20\,\mu$m and $4\,\mathrm{x}\,75\,\mu$m, corresponding to a current scaling ratio of 7.5. The same can be shown for the PH15 GaAs device, where π_{eff} also enables an accurate static current scaling model (Appendix C.2).

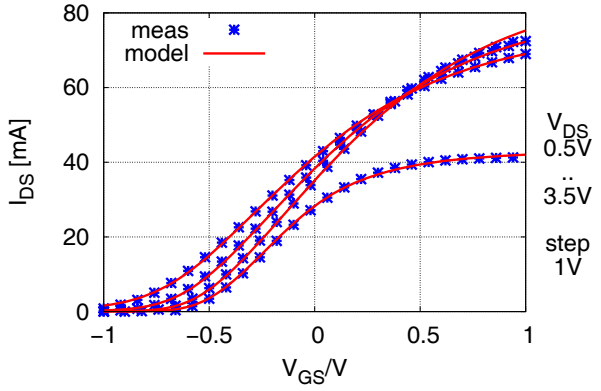

Figure 3.6: Measured and modelled transfer characteristics of a $2\,\mathrm{x}\,50\,\mu$m GaAs pHEMT (PH15) for drain-source voltages in the linear and saturated regime.

Transfer characteristics

HFET devices show particular nonlinearities of drain current with respect to the controlling gate-source-voltage V_{gs}. These are best observed in the transfer- and transconductance characteristics. Above threshold and in saturated operation, drain current increases approximately linearly with V_{gs}, resulting in a near constant transconductance over a wide voltage range. This is the ideal current characteristic due to linear control of charge density in the 2DEG, as derived in basic HEMT operating theory (e.g. [92, 3, 2]). The formation of parasitic MESFET-like channels, also referred to as three dimensional electron gas (3DEG), leads to a reduction of transconductance under forward bias. Additional effects like self-heating with increasing power levels are overlaid in the transfer characteristics of different drain-source voltages. Global modelling of the nonlinearities of transfer characteristics in HFET devices is particularly challenging, and represents the fundamental reason for employing empirical drain current expressions, detached from the complex underlying device physics. This is accounted for by the introduction of parameter η in the original COBRA model, allowing for a more flexible description of transconductance compression with increasing V_{gs}. Fig. 3.6 shows the transfer characteristics of a 2x50 μm GaAs pHEMT (PH15) for drain-source voltages ranging from linear- and weakly saturated to the strongly saturated regime. The modified COBRA model is capable of describing these characteristics globally. In this case, a value of $\eta = 0.88$ was used. Fig. 3.7 shows measured and modelled transconductance of the same device for the linear and saturated regime.

The partial derivatives of transconductance with respect to V_{gs} are of particular interest for evaluation of gain compression and creation of harmonic frequencies under large-signal operation of the devices (e.g. [98]). They represent the coefficients of the Taylor series expansion to transconductance. This is shown in Fig. 3.7 up to the third derivative of transconductance in the saturated region of the above device. Measured transconductance and its partial derivatives are obtained from numerical differentiation of drain current with

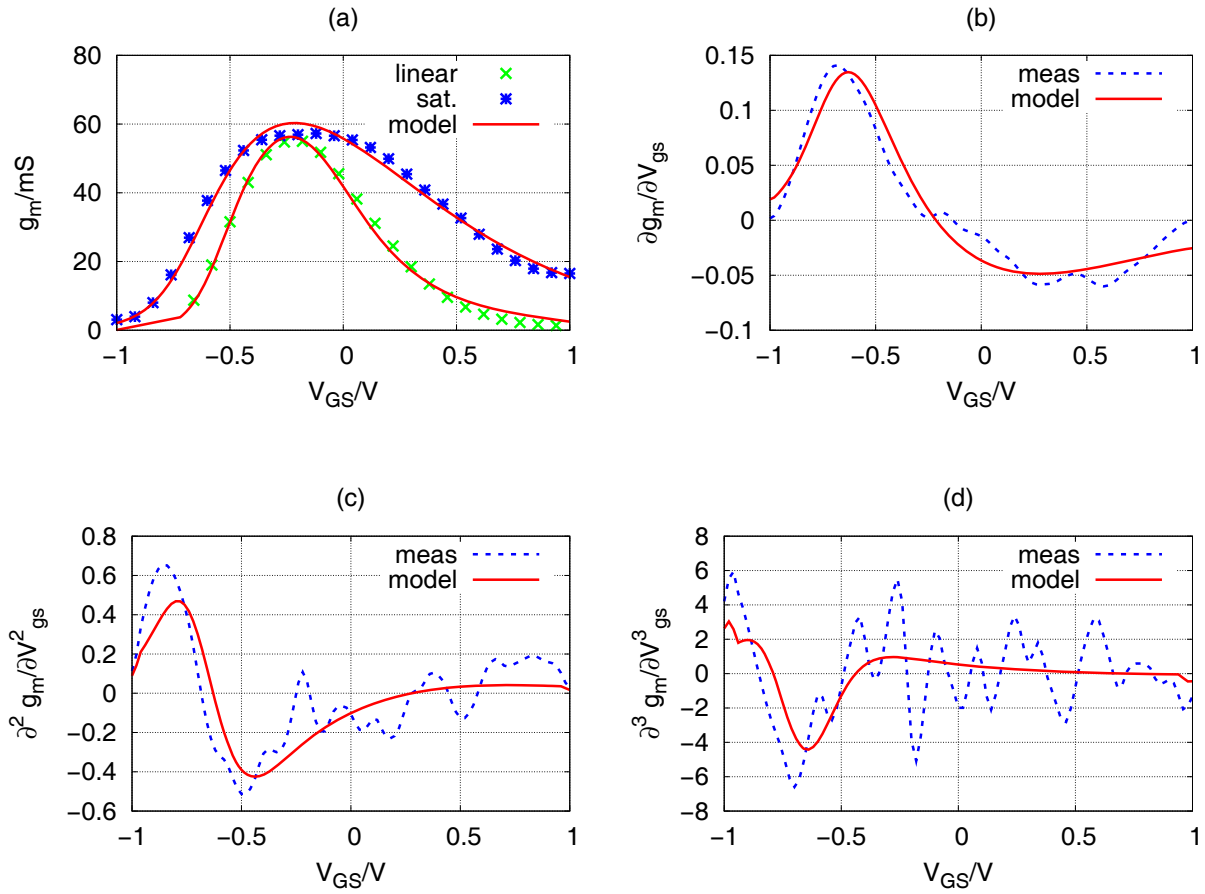

Figure 3.7: (a) Measured and modelled transconductance of a 2x50 μm GaAs pHEMT (PH15) in linear mode ($V_{ds} = 0.5\,V$) and in saturation ($V_{ds} = 2.5\,V$). (b)-(d) First, second and third partial derivatives of transconductance with respect to V_{gs} in saturation.

respect to V_{gs} using linear interpolation. Small fluctuations of the measured drain current result in ripples in the numerical derivatives. Nevertheless, it is possible to observe the excellent correspondence of the model with averaged measured values.

The globally accurate description of complex transfer characteristics demonstrates the modified COBRA model's suitability for HFET devices. It is responsible for the accurate modelling of gain compression and frequency intermodulation characteristics observed in one- and two-tone power measurements (see chapter 3.8).

3.2.2 Gate current model

The static gate current, as depicted in Fig. 3.3, is modelled via the diodes D_{gs} and D_{gd}. These use the well-known exponential diode current expression with its parameters I_s, the saturation current, and n_{id}, the ideality factor. A breakdown model is used for both diodes. Also, leakage current elements G_{lgs} and G_{lgd} are included, adding to the total static gate

current of:

$$I_{\mathrm{g}}(V_{\mathrm{gs}}, V_{\mathrm{gd}}) = I_{\mathrm{gs}}(V_{\mathrm{gs}}) + I_{\mathrm{gd}}(V_{\mathrm{gd}}) + I_{\mathrm{bgs}}(V_{\mathrm{gs}}) + I_{\mathrm{bgd}}(V_{\mathrm{gd}}) + G_{\mathrm{lgs}}V_{\mathrm{gs}} + G_{\mathrm{lgd}}V_{\mathrm{gd}} \tag{3.21}$$

$$I_{\mathrm{gs}}(V_{\mathrm{gs}}) = I_{\mathrm{sgs}}\left(e^{\frac{V_{\mathrm{gs}}}{n_{\mathrm{id}}\cdot V_{\mathrm{th}}}} - 1\right) \tag{3.22}$$

$$I_{\mathrm{gd}}(V_{\mathrm{gd}}) = I_{\mathrm{sgd}}\left(e^{\frac{V_{\mathrm{gd}}}{n_{\mathrm{id}}\cdot V_{\mathrm{th}}}} - 1\right) \tag{3.23}$$

where $V_{\mathrm{th}} = (\mathrm{k}T/\mathrm{q})$ is the thermal voltage of approximately 26 mV at room temperature.

For improved convergence behaviour of the gate current model, all exponential expressions employ the standard linearisation technique beyond a certain forward diode current I_{max}. All resulting equations are listed in Appendix B.

While under typical transistor operating conditions, breakdown will occur only in the gate-drain junction, e.g. for close-to-threshold biasing under high drain voltage conditions, an accurate gate current model may be useful when exploiting the transistor Schottky gate junction in circuits, e.g. for level-shifting or switching operation. The breakdown current model is similar to the EEsof HEMT1 model in Agilent ADS [70] by employing an exponential expression. While the ADS model requires partially defined equations and doesn't satisfy the condition for continuous derivatives, the breakdown model introduced is a single expression guaranteeing global continuity of the diode current characteristics and its derivatives. The model introduces the reverse breakdown voltage $V_{\mathrm{bv}} < 0$, breakdown current $I_{\mathrm{bv}} < 0$ and breakdown "ideality factor" n_{bv}:

$$I_{\mathrm{bgs}}(V_{\mathrm{gs}}) = I_{\mathrm{bv}}e^{\frac{-(V_{\mathrm{gs}}-V_{\mathrm{bv}})}{n_{\mathrm{bv}}V_{\mathrm{th}}}} \cdot \frac{V_{\mathrm{gs}}}{V_{\mathrm{bv}}} \tag{3.24}$$

$$I_{\mathrm{bgd}}(V_{\mathrm{gd}}) = I_{\mathrm{bv}}e^{\frac{-(V_{\mathrm{gd}}-V_{\mathrm{bv}})}{n_{\mathrm{bv}}V_{\mathrm{th}}}} \cdot \frac{V_{\mathrm{gd}}}{V_{\mathrm{bv}}} \tag{3.25}$$

The novelty here is the factor $(V_{\mathrm{d}}/V_{\mathrm{bv}})$, where V_{d} is the respective diode voltage. Its purpose is to assure that current becomes zero at zero diode voltage, but otherwise it doesn't significantly influence the qualitative and quantitative behaviour of the exponential breakdown current. The same linearisation technique as employed in the forward diode models is applied to the breakdown current.

Fig. 3.8(left) shows measured and simulated static gate current characteristics of a $2\,\mathrm{x}\,50\,\mu$m GaAs pHEMT (PH15). Current is plotted on a linear scale versus V_{gs}at zero V_{ds}. Reverse breakdown is observed and accurately modelled. Plotting gate current magnitude on a logarithmic scale reveals the impact of series resistance on the diode current, resulting in a degradation from the ideally linear forward current. This is shown in Fig. 3.8(right) for a $2\,\mathrm{x}\,40\,\mu$m InP device.

The gate current model completes the nonlinear static model of the HFET. For the complete nonlinear gate current model characteristics and parameter values of all technologies, refer to Appendix C.

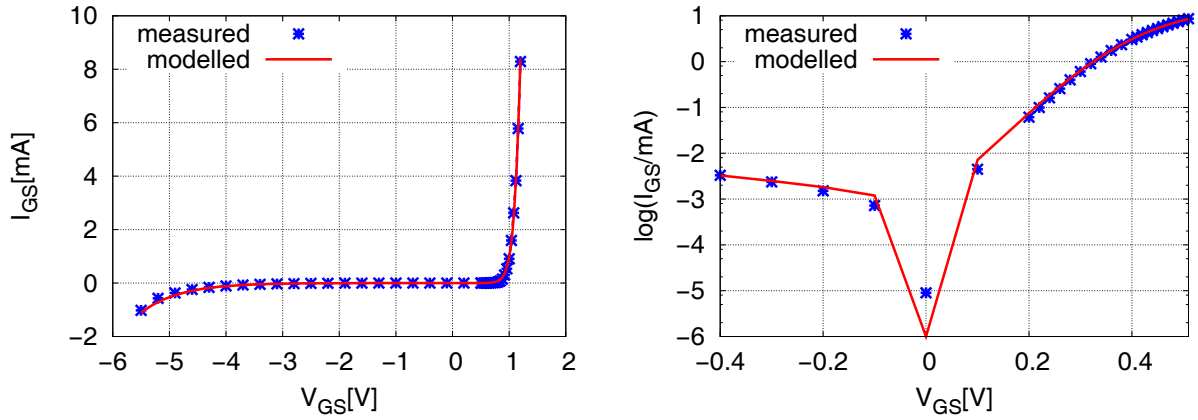

Figure 3.8: Static gate current in the 2 x 50 μm PH15 GaAs pHEMT device (left). Logarithmic plot of gate current in a 2 x 40 μm InP pHEMT (right).

3.3 Dynamic Model

The full large-signal model topology is shown in Fig. 3.9. Besides static nonlinearities, the dynamic model contains a nonlinear, multiple time constant dispersion model and a nonlinear gate capacitance model, both of them universally applicable to all HFET technologies.

3.3.1 Multi-Bias Small-Signal Model Extraction

Dynamic model extraction is based on small-signal device characterisation in the microwave frequency range. S-parameter measurements are carried out in an array of bias voltage conditions covering the complete operating regime of the DUT, i.e. gate bias conditions vary from subthreshold to onset of gate conduction, while drain bias is swept from the linear- and saturated regime to the onset of drain current breakthrough.

Applying the advanced de-embedding technique (chapter 3.1) to these measurements yields the intrinsic FET Y-parameters $[Y_i]_B$, where index B denotes the covered bias range. The small-signal equivalent circuit used to describe the intrinsic FET is shown in Fig. 3.10. The four complex Y-parameters are sufficient to deduce eight model parameters: dynamic transconductance g_m and time delay τ, dynamic output conductance g_{ds}, gate-source capacitance C_{gs}, gate-drain capacitance C_{gd}, drain-source capacitance C_{ds}, gate-source domain resistance R_{gsi} and gate-drain domain resistance R_{gdi}.

The circuit's Y-parameters have been calculated and solved for the model elements in [85]. All resulting equations are listed in Appendix A. The two gate conductance parameters g_{dgs} and g_{dgd} are also required. While [85] suggests to use fixed values deduced from gate leakage measurements, here the differential gate conductances $g_{dgs} = (\partial I_{gs}/\partial V_{gs})$ and $g_{dgd} = (\partial I_{gd}/\partial V_{gd})$, derived from the static model have been employed. Since the static model describes both reverse and forward gate conduction, including gate leakage and reverse breakdown (see chapter 3.2.2), this approach extends the validity range of the small-signal

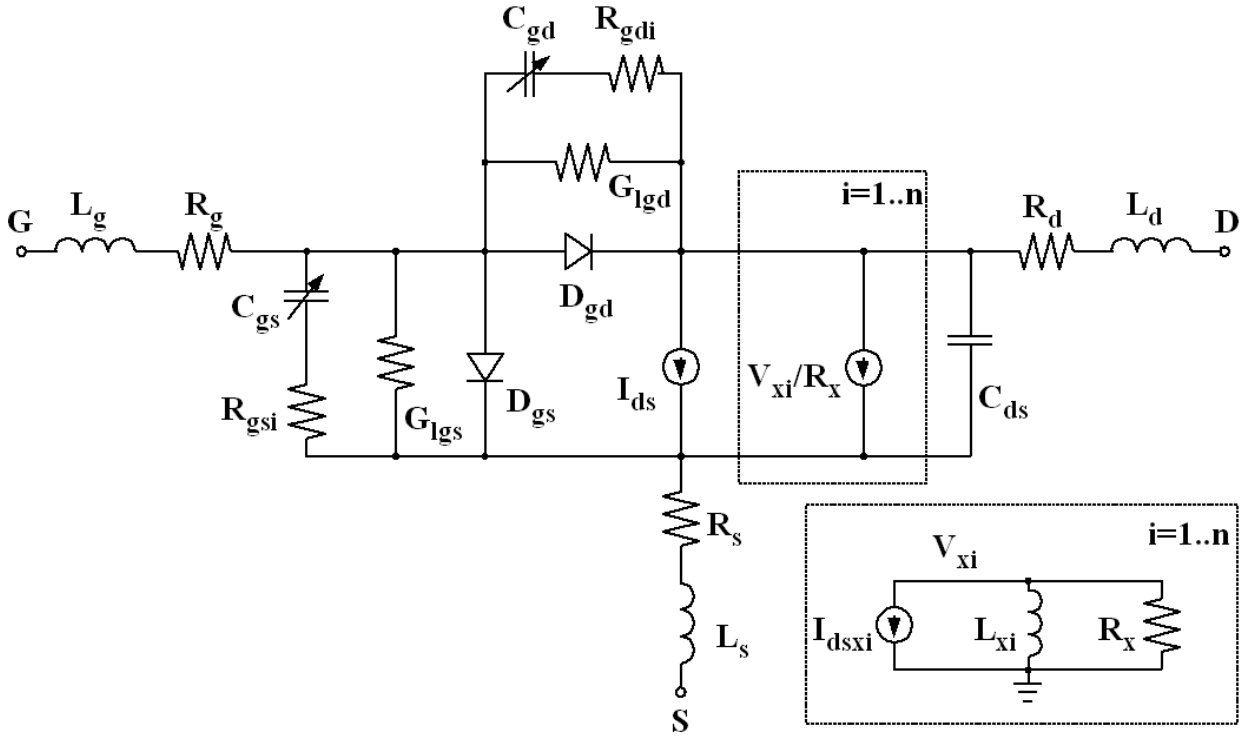

Figure 3.9: Full static and dynamic large-signal model topology.

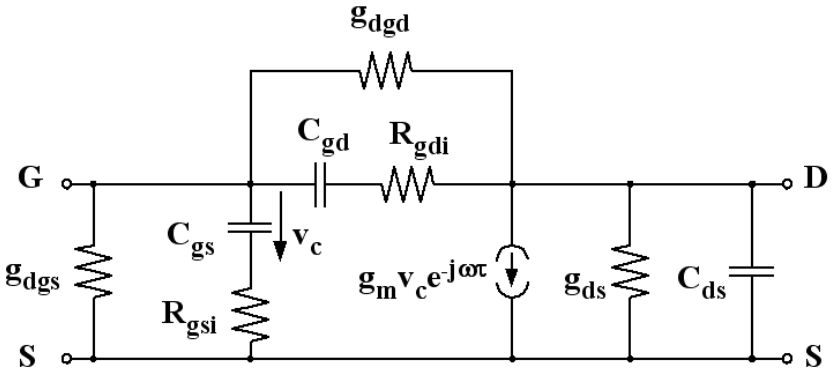

Figure 3.10: Intrinsic FET small-signal equivalent circuit.

model topology to the voltage regime of forward gate conduction at high gate potentials as well as gate-drain breakthrough under high drain potentials.

Since the Y-parameters of any particular bias point are measured over the whole range of frequencies, the model parameters also are obtained as a function of frequency. Ideally, of course, since both the model topology and the parameters should be frequency independent, the extracted parameter values should be constant versus frequency. Even in case of the dispersive parameters g_{m} and g_{ds} this assumption holds, since the Y-parameters are measured in the microwave frequency range, well above the corner frequencies of dispersion effects. The final values used in the small-signal model are obtained from averaging over a particular frequency range, where the parameter in question shows constant behaviour. The resulting multi bias small-signal model is applicable as a so-called table based model.

Up to this stage, parameter extraction is fully analytical. The extraction sequence comprising S-parameter import, de-embedding and solving of $[Y_{\mathrm{i}}]_{\mathrm{B}}$ for model parameters has been fully implemented into the extraction software FETfit described in chapter 3.6. In some cases, final parameter optimisation or -fitting may achieve improved small-signal model parameters. The software also provides this functionality by applying the Levenberg-Marquardt optimisation algorithm [99, 100] to minimise the difference between measured and simulated twoport parameters. The error function E, which the algorithm tries to minimise, can be adapted to suit the sensitivity of the extracted parameter(s). E is defined as follows:

$$E = \sum_{\mathrm{F}} \sum_{i=1}^{2} \sum_{j=1}^{2} \left(w_{ij} \left[w_{\mathrm{x}ij} X \left(\frac{P_{ij,\mathrm{model}} - P_{ij,\mathrm{meas}}}{P_{ij,\mathrm{meas}}} \right)^2 + w_{\mathrm{y}ij} Y \left(\frac{P_{ij,\mathrm{model}} - P_{ij,\mathrm{meas}}}{P_{ij,\mathrm{meas}}} \right)^2 \right] \right) \tag{3.26}$$

where F is the frequency range, P_{ij} is a twoport parameter (Y-, Z-, H- or S-parameter), $X\,()$ signifies either the real part or magnitude and $Y\,()$ either imaginary part or phase of the respective complex value. Individual contributions are weighted by w_{ij}, $w_{\mathrm{x}ij}$ and $w_{\mathrm{y}ij}$.

In the development of a large-signal model, the voltage dependencies of dynamic trans- and output conductance are used in the dispersion model part, while those of C_{gs} and C_{gd} are modelled by a charge-conservative nonlinear capacitance model as described in the following chapter. Although obtained in the extraction process, nonlinearities in all other model parameters are neglected and a typical value from the saturated regime is used in the model. Voltage dependencies of the non-quasi static elements τ and R_{gsi} have been investigated and modelled for the GaAs power pHEMT process (PPH15) in [101].

3.4 Nonlinear Capacitance Model

The voltage dependence of gate charge and capacitance constitutes the reactive nonlinearity in HFET devices, equal in importance to the conductive nonlinear contribution of drain current for the accurate description of dynamic device characteristics.

First, a unified formulation of charge-conservative capacitance expressions is developed.

A particular form of this general approach is then adopted to describe the nonlinearities of gate-source and gate-drain capacitance of all HEMT technologies investigated in this work.

3.4.1 A Unified Approach to Charge-Conservative Capacitance Modelling

In any field-effect transistor device, the charge density in the channel is opposed by charge of equal magnitude and opposite polarity on the gate terminal, forming the total gate charge $Q_{\mathrm{g}} = -Q_{\mathrm{channel}}$, which itself is a function of the junction voltages V_{gs} and V_{ds}:

$$Q_{\mathrm{g}}(V_{\mathrm{gs}}, V_{\mathrm{ds}}) \tag{3.27}$$

Physically, the channel charge is distributed across the transistor gate length L_{g}. In the equivalent circuit based modelling approach, the total gate charge is divided between and attributed to the gate-source- and gate-drain terminals. The entity extractable from device characterisation is capacitance between these terminals, together with their bias voltage dependencies:

$$C_{\mathrm{gs}}(V_{\mathrm{gs}}, V_{\mathrm{ds}}) \tag{3.28}$$

$$C_{\mathrm{gd}}(V_{\mathrm{gd}}, V_{\mathrm{ds}}) \tag{3.29}$$

In these expressions, the three junction voltages are of course related by

$$V_{\mathrm{ds}} = V_{\mathrm{gs}} - V_{\mathrm{gd}} \tag{3.30}$$

Typically, in the device characterisation process, the junction voltages V_{gs} and V_{ds} are treated as the two independent variables. For physical interpretation, however, it is more convenient to use the terminal voltages V_{gs} and V_{gd} as the independent entities in expressing the junction capacitance C_{gs} or C_{gd}.

For the capacitance data to stem from a single channel charge, i.e. for equation (3.31)

$$\begin{pmatrix} C_{\mathrm{gs}}(V_{\mathrm{gs}}, V_{\mathrm{gd}}) \\ C_{\mathrm{gd}}(V_{\mathrm{gs}}, V_{\mathrm{gd}}) \end{pmatrix} = \bigtriangledown(Q_{\mathrm{g}}(V_{\mathrm{gs}}, V_{\mathrm{gd}})) \tag{3.31}$$

to hold, the capacitance expressions need to satisfy the following condition, also known as charge-conservation criterion [102, 103, 104]:

$$\frac{\partial C_{\mathrm{gs}}}{\partial V_{\mathrm{gd}}} = \frac{\partial^2 Q_{\mathrm{g}}}{\partial V_{\mathrm{gs}} \partial V_{\mathrm{gd}}} = \frac{\partial^2 Q_{\mathrm{g}}}{\partial V_{\mathrm{gd}} \partial V_{\mathrm{gs}}} = \frac{\partial C_{\mathrm{gd}}}{\partial V_{\mathrm{gs}}} \tag{3.32}$$

Equation (3.32) states that the vector field $\mathbf{C} = (C_{\mathrm{gs}}, C_{\mathrm{gd}})$ is conservative, i.e. it forms the gradient of a scalar function Q_{g} according to (3.31). In other words, the curl of $\mathbf{C}$

vanishes: $\bigtriangledown \times \mathbf{C} = 0$ [105]. If this condition is not met in the model equations, not only the underlying device physics are violated, but the simulator may run into convergence problems.

While physical models like Statz-Pucel [106] and [107] have been proposed for FET charge and capacitance, they suffer from the same restrictions in terms of accuracy and global validity as the drain current models do. Especially in the case of advanced heterostructure devices such as the HEMTs investigated in this work, empirical models are resorted to for the development of models dedicated to circuit design. Typically, such nonlinear capacitance equations are made up of terms which depend only on the respective junction voltage and ones which contain both voltages.

$$C_{\mathrm{gs}} = F_1(V_{\mathrm{gs}}) + F_2(V_{\mathrm{gs}}, V_{\mathrm{gd}}) \tag{3.33}$$

$$C_{\mathrm{gd}} = G_1(V_{\mathrm{gd}}) + G_2(V_{\mathrm{gs}}, V_{\mathrm{gd}}) \tag{3.34}$$

The charge-conservation criteria apply only to the interdependent terms F_2 and G_2. A generalized form of charge-conservative interdependent capacitance equations can be written as

$$F_2 = C_{\mathrm{S}}(V_{\mathrm{gs}}) \cdot F_3(V_{\mathrm{gs}} - V_{\mathrm{gd}}) - \frac{\partial C_{\mathrm{S}}(V_{\mathrm{gs}})}{\partial V_{\mathrm{gs}}} \cdot \int F_3(V_{\mathrm{gs}} - V_{\mathrm{gd}}) \partial V_{\mathrm{gd}} \tag{3.35}$$

$$G_2 = -C_{\mathrm{S}}(V_{\mathrm{gs}}) \cdot F_3(V_{\mathrm{gs}} - V_{\mathrm{gd}}) \tag{3.36}$$

Charge-conservation is observed generally for any $C_{\mathrm{S}}(V_{\mathrm{gs}})$ and $F_3(V_{\mathrm{gs}} - V_{\mathrm{gd}}) = F_3(V_{\mathrm{ds}})$, since

$$\begin{array}{rcl} \frac{\partial C_{\mathrm{gs}}}{\partial V_{\mathrm{gd}}} & = & C_{\mathrm{S}}(V_{\mathrm{gs}}) \cdot (-1) \cdot \frac{\partial F_3(V_{\mathrm{gs}} - V_{\mathrm{gd}})}{\partial (-V_{\mathrm{gd}})} - \frac{\partial C_{\mathrm{S}}(V_{\mathrm{gs}})}{\partial V_{\mathrm{gs}}} \cdot F_3(V_{\mathrm{gs}} - V_{\mathrm{gd}}) \\ & = & -C_{\mathrm{S}}(V_{\mathrm{gs}}) \cdot \frac{\partial F_3(V_{\mathrm{gs}} - V_{\mathrm{gd}})}{\partial V_{\mathrm{gs}}} - \frac{\partial C_{\mathrm{S}}(V_{\mathrm{gs}})}{\partial V_{\mathrm{gs}}} \cdot F_3(V_{\mathrm{gs}} - V_{\mathrm{gd}}) \quad = \quad \frac{\partial C_{\mathrm{gd}}}{\partial V_{\mathrm{gs}}} \end{array} \tag{3.37}$$

Equations (3.38) and (3.39) represent a unified approach to the charge-conservative modelling of FET capacitance, allowing for a variety of expressions. The approach taken in this work to model the interdependent terms is similar to the basic empirical drain current equation of Curtice:

$$\begin{array}{rcl} F_2(V_{\mathrm{gs}}, V_{\mathrm{gd}}) & = & C_{\mathrm{S}}(V_{\mathrm{gs}}) \cdot (1 + \tanh(\iota [V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}])) \\ & & -\frac{\partial C_{\mathrm{S}}(V_{\mathrm{gs}})}{\partial V_{\mathrm{gs}}} \cdot \left(V_{\mathrm{gd}} - \frac{1}{\iota} \ln(\cosh[\iota (V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}})]) \right) \end{array} \tag{3.38}$$

$$G_2(V_{\mathrm{gs}}, V_{\mathrm{gd}}) = -C_{\mathrm{S}}(V_{\mathrm{gs}}) \cdot (1 + \tanh(\iota [V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}])) \tag{3.39}$$

The term C_{S} corresponds to the saturation current I_{S} in the Curtice model, itself being a function of V_{gs}. The expression employed for C_{S} follows closely the definition of saturation

current in the drain current model from equation (3.15):

$$C_{\mathrm{S}}(V_{\mathrm{gs}}) = C_3 \cdot V_{\mathrm{eff}}^{\psi} \tag{3.40}$$

where C_3 is a capacitance constant and $V_{\mathrm{eff}} = \frac{1}{2}\left(V_{\mathrm{gs}} - V_{\mathrm{t3}} + \sqrt{(V_{\mathrm{gs}} - V_{\mathrm{t3}})^2 + \theta^2}\right)$ corresponds to the "gate overtravel" derived from the threshold voltage V_{t3}.

The transition from the linear- to the saturated operating region in both C_{gs} and C_{gd} is described by a tanh() function:

$$F_3(V_{\mathrm{ds}}) = F_3(V_{\mathrm{gs}} - V_{\mathrm{gd}}) = 1 + \tanh\left(\iota\left[V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right]\right) \tag{3.41}$$

The charge-conservation criterion applied to the above equations yields

$$\begin{aligned} \frac{\partial C_{\mathrm{gs}}}{\partial V_{\mathrm{gd}}} &= -C_{\mathrm{S}}(V_{\mathrm{gs}}) \cdot \iota \cdot \operatorname{sech}^2\left(\iota\left[V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right]\right) - \frac{\partial C_{\mathrm{S}}(V_{\mathrm{gs}})}{\partial V_{\mathrm{gs}}} \cdot \left(1 + \tanh\left[\iota\left(V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right)\right]\right) \\ &= \frac{\partial C_{\mathrm{gd}}}{\partial V_{\mathrm{gs}}} \end{aligned} \tag{3.42}$$

$$\frac{\partial C_{\mathrm{S}}(V_{\mathrm{gs}})}{\partial V_{\mathrm{gs}}} = C_3 \cdot \psi V_{\mathrm{eff}}^{\psi-1} \frac{\partial V_{\mathrm{eff}}(V_{\mathrm{gs}})}{\partial V_{\mathrm{gs}}} \tag{3.43}$$

The full capacitance model based on the forgoing equations is discussed, applied and verified for the different HEMT technologies in the following chapter.

3.4.2 A Universal HFET Capacitance Model

The novel charge-conservative capacitance expressions (3.44) and (3.45) have been developed to accurately reflect the voltage-dependence of HFET gate-to-source and gate-to-drain capacitance characteristics. The same equations have been employed to describe each of the technologies through extraction of their respective capacitance parameter sets.

$$\begin{aligned} C_{\mathrm{gs}} &= C_{\mathrm{pgs}} + \frac{C_{\mathrm{gs1}}}{(1 - \frac{V_{\mathrm{gs}}}{V_{\mathrm{bi}}})^m} \\ &\quad + C_{\mathrm{gs2}}(1 + \tanh(\kappa(V_{\mathrm{gs}} - V_{\mathrm{t2}}))) \\ &\quad + C_{\mathrm{S}}(V_{\mathrm{gs}}) \cdot \left(1 + \tanh\left(\iota\left[V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right]\right)\right) \\ &\quad - \frac{\partial C_{\mathrm{S}}(V_{\mathrm{gs}})}{\partial V_{\mathrm{gs}}} \cdot \left(V_{\mathrm{gd}} - \frac{1}{\iota} \ln\left(\cosh\left[\iota\left(V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right)\right]\right)\right) \end{aligned} \tag{3.44}$$

$$\begin{aligned} C_{\mathrm{gd}} &= C_{\mathrm{pgd}} + \frac{C_{\mathrm{gd1}}}{(1 - \frac{V_{\mathrm{gd}}}{V_{\mathrm{bi}}})^m} \\ &\quad + C_{\mathrm{gd2}}(1 + \tanh(\kappa(V_{\mathrm{gd}} - V_{\mathrm{t5}}))) \\ &\quad - C_{\mathrm{S}}(V_{\mathrm{gs}}) \cdot \left(1 + \tanh\left(\iota\left[V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right]\right)\right) \end{aligned} \tag{3.45}$$

$$C_{\mathrm{S}}(V_{\mathrm{gs}}) = C_3 \cdot V_{\mathrm{eff}}^{\psi} \tag{3.46}$$

$$V_{\mathrm{eff}} = \frac{1}{2}\left(V_{\mathrm{gs}} - V_{\mathrm{t3}} + \sqrt{(V_{\mathrm{gs}} - V_{\mathrm{t3}})^2 + \theta^2}\right) \tag{3.47}$$

Equations (3.44) and (3.45) represent a generalized form of similar published capacitance expressions, such as [108][109] for an RF CMOS transistor technology.

In these capacitance equations, the fixed capacitance values C_{pgs} and C_{pgd} allow for a constant capacitance contribution, arising from geometrical overlap or so-called "fringing" capacitance between the contact terminals. While in MOS-like structures some small geometrical overlap between the gate/source- and gate/drain contacts is required for transistor operation, these terms are much smaller in HEMT-type transistors, where fixed capacitance merely arises from fringing electrical fields between the contact areas.

The second term in the above equations is the well-known expression for the diode junction capacitance, using the built-in voltage V_{bi}, an ideality factor m and the built-in junction capacitance C_{gs1} (C_{gd1}) as parameters.

The third term describes - in an empirical way - the contribution of the channel charge build-up to the respective terminal capacitance arising from a change in the terminal voltages V_{gs} and V_{gd}, i.e. the terminal capacitance at zero V_{ds}. The transition voltages V_{t2} and V_{t5} can, in a first-order approximation, be chosen slightly above the threshold voltage. Since no V_{ds}-dependence has been introduced in the expressions so far, the parameters of the capacitance terms up to now can be extracted from capacitance data at $V_{\mathrm{ds}} = 0\,\mathrm{V}$ and swept $V_{\mathrm{gs}} = V_{\mathrm{gd}}$. From a physical point of view, due to symmetry considerations in the devices' geometry, one would expect all corresponding gate-source and gate-drain parameters to be identical. However, the gate contact of a HEMT device may intentionally be placed closer to the source contact, thereby reducing the parasitic feedback series resistance R_{s} in the source path. In that case, C_{gs} and C_{gd} will not be identical even for zero drain bias.

The remaining terms of the capacitance model describe the V_{ds}-dependence of the gate capacitance. In terms of modelling, this is the crucial and most demanding part, since charge-conservation needs to be observed in the respective expressions as discussed in the previous section. Fig. 3.11 shows extracted and modelled capacitance of a $2\,\mathrm{x}\,50\,\mu$m GaAs device (PH15), both versus V_{gs}(transfer characteristics) and versus V_{ds}(output characteristics), covering the IV plane from sub-threshold to active regions and linear to saturated regimes. The same is shown in Fig. 3.12 for a $2\,\mathrm{x}\,20\,\mu$m PPH15 device. The extracted (measured) capacitance data is obtained from the multi-bias small-signal extraction process discussed in chapter 3.3.1.

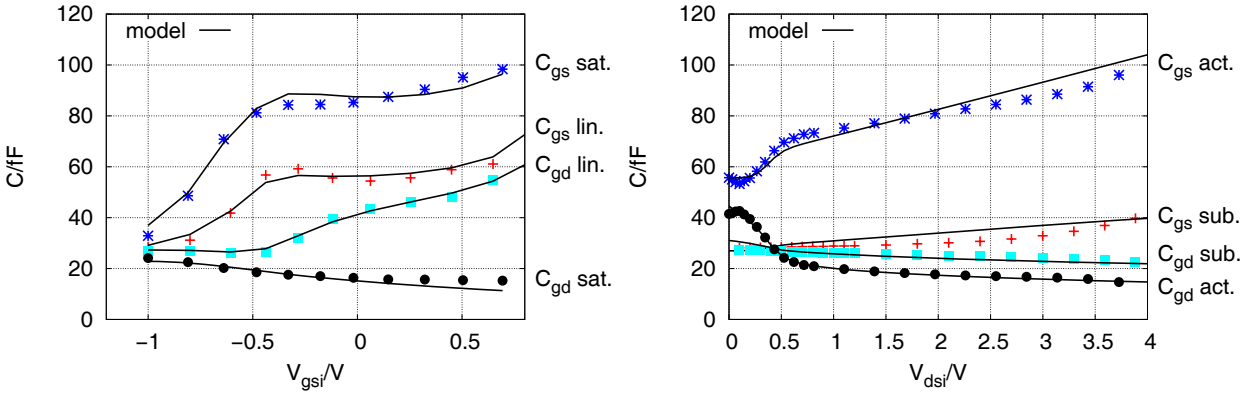

Figure 3.11: Extracted versus modelled capacitance in a $2\,\mathrm{x}\,50\,\mu$m GaAs PH15 device. Left: versus V_{gs} in linear ($V_{\mathrm{ds}} = 0.5\,\mathrm{V}$) and saturated ($V_{\mathrm{ds}} = 2.7\,\mathrm{V}$) region. Right: versus V_{ds} in sub-threshold ($V_{\mathrm{gs}} = -1\,\mathrm{V}$) and active ($V_{\mathrm{gs}} = 0\,\mathrm{V} \approx g_{\mathrm{m,max}}$) region.

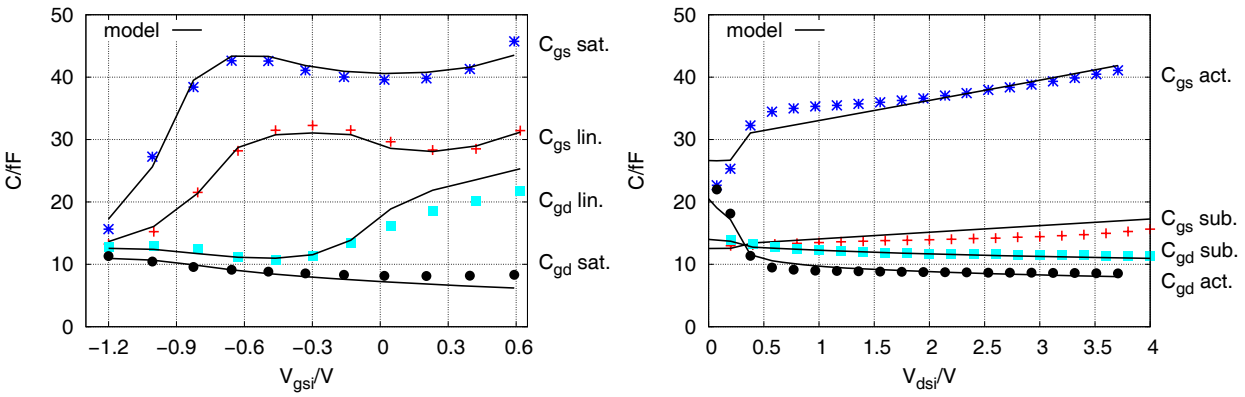

Figure 3.12: Extracted versus modelled capacitance in a $2\mathrm{x}20\,\mu$m GaAs PPH15 device. Left: versus V_{gs} in linear ($V_{\mathrm{ds}} = 0.6\,\mathrm{V}$) and saturated ($V_{\mathrm{ds}} = 3.6\,\mathrm{V}$) region. Right: versus V_{ds} in sub-threshold ($V_{\mathrm{gs}} = -1.2\,\mathrm{V}$) and active ($V_{\mathrm{gs}} = -0.2\,\mathrm{V} \approx g_{\mathrm{m,max}}$) region.

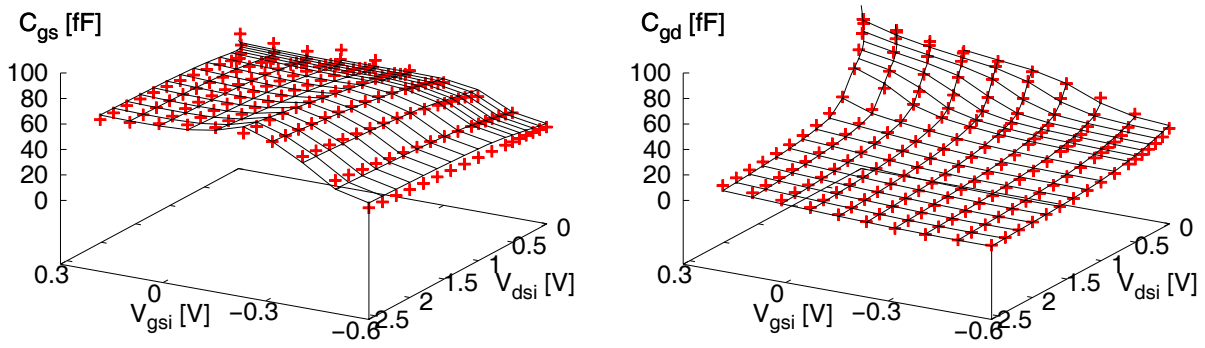

Figure 3.13: Nonlinear capacitance in a 2x50 μm strained-Si/SiGe mHEMT versus static internal junction voltages. Multi-bias extraction (points) and model (lines) for C_{gs} (left) and C_{gd} (right).

Particularity of HEMT capacitance characteristics

Of particular interest is the observation of a local minimum of C_{gs}, when plotted versus V_{gs}. After reaching a maximum at the V_{gs} of maximum gain[3], C_{gs} drops before increasing again towards high V_{gs} due to the Schottky gate capacitance approaching forward bias. These characteristics are observed in all HEMT technologies, which has given rise to questioning their physical origin. One reason for an intermediate drop in C_{gs} with rising V_{gs} can be the formation of charge in the supply layer above the channel, but unconnected to the source- and drain implantation regions. This effectively would lead to a series combination of capacitance between gate and channel and hence reduce the overall capacitance. A suggested correlation between the capacitance characteristics and static gate current measurements [110] could not be confirmed. An interesting approach is taken in [111], which divides total capacitance of a MODFET gate structure into individual contribution from the 2DEG and the Schottky junction. With increasing V_{gs}, the 2DEG capacitance actually drops, since the carrier concentration in the 2DEG reaches an equilibrium and is no longer modulated by the gate potential due to the onset of carrier accumulation in the parasitic MESFET channel of the supply layer.

Finally, in order to demonstrate the universal suitability of the nonlinear capacitance model, Fig. 3.13 shows its application to the strained-Si/SiGe mHEMT device over the full IV plane. The model accurately and globally describes these capacitance nonlinearities.

Parameter values and capacitance data for all HFET technologies are listed in Appendix C. Nonlinear capacitance has been directly implemented in the model topology, requiring the use of an auxiliary circuit as described in 3.7.1.

[3]note that capacitance is plotted against internal voltages V_{gsi} and V_{dsi}, which are reduced by the voltage drop across the series terminal resistances compared to the respective externally applied voltages V_{gs} and V_{ds}.

3.5 Multiple Time-Constant Dispersion Model

With all of the modelled HEMT technologies showing frequency dispersive effects, an accurate dispersion model is required to enhance the model's validity range from DC and low-frequency to the microwave regime. The new approach to dispersion modelling is discussed here in terms of topology, linear and nonlinear equations and parameter extraction. Its advantages over the various state-of-the-art dispersion models are

- the inclusion of multiple dispersion effects and their respective time constants,
- an accurate description of the transition between dispersive regimes in the time- and frequency domain,
- the model topology contains only standard electrical elements which can easily be implemented into simulation environments,
- a clear model parameter extraction procedure based on standard measurement techniques (S-parameters and pulsed-IV),
- high computational efficiency and
- global model validity.

3.5.1 Physical Motivation

The basis of the dispersion circuit topology is the assumption that individual dispersion effects introduce an exponentially decaying time domain characteristic to channel carrier density n_s and, due to the proportionality between carrier density and current, to the resulting drain-source current I_ds. Applying a step change in either one of the controlling voltages V_gs and V_ds at time $t = 0$, will result in a step response of the carrier density and the drain current of the form

$$n_\mathrm{s}(t) \sim I_\mathrm{ds}(t) = I_0 + (I_1 - I_0)\, e^{-\frac{t}{\tau_1}} \tag{3.48}$$

where τ_1 is the time constant associated with one particular dispersion effect, I_1 is the current flowing immediately after the voltage change when a particular physical condition responsible for dispersion, e.g. channel temperature, trap occupation etc., is still in the state of condition $t < 0$. Finally, I_0 is the drain current under the new voltage conditions when the dispersion effect has adapted to the new voltage regime.

The assumption of an exponentially decaying step response due to a single dispersion effect is well founded in the case of thermal dispersion as well as trapping/de-trapping effects. The frequency dependence introduced by impact ionisation to the small-signal characteristics of InP-based HFETs has been shown to obey the same principle [55].

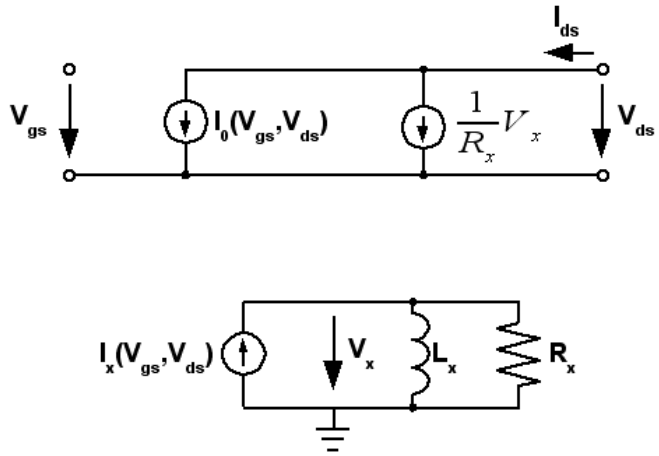

Figure 3.14: Large-signal equivalent circuit of a single dispersion effect. Dispersion part only.

Introducing the Heaviside function $s\,(t)$, the step response $a\,(t)$ of the drain current can be written as

$$a\,(t) = s\,(t)\left(I_0 + (I_1 - I_0)\,e^{-\frac{t}{\tau_1}}\right) \tag{3.49}$$

Equation (3.49) has the well-known form of a single-pole or first-order system transfer function. Since drain current is a nonlinear function of two independent controlling voltages $V_{\rm gs}$ and $V_{\rm ds}$, the step response to a change in one of the controlling voltages is found by partial differentiation of (3.49), yielding $a_{\rm gs}(t) = (\partial a(t)/\partial V_{\rm gs})$ and $a_{\rm ds}(t) = (\partial a(t)/\partial V_{\rm ds})$. Differentiation in time domain results in the pulse responses $h_{\rm gs}\,(t) = (\partial a_{\rm gs}\,(t)\,/\partial t)$ and $h_{\rm ds}\,(t) = (\partial a_{\rm ds}\,(t)\,/\partial t)$. Making use of the Dirac pulse function $\delta\,(t)$and its sifting property, they can be written as:

$$h_{\rm gs}\,(t) = \delta\,(t)\,\frac{\partial I_1}{\partial V_{\rm gs}} - \frac{s\,(t)}{\tau_1}\left(\frac{\partial I_1}{\partial V_{\rm gs}} - \frac{\partial I_0}{\partial V_{\rm gs}}\right)e^{-\frac{t}{\tau_1}} \tag{3.50}$$

$$h_{\rm ds}\,(t) = \delta\,(t)\,\frac{\partial I_1}{\partial V_{\rm ds}} - \frac{s\,(t)}{\tau_1}\left(\frac{\partial I_1}{\partial V_{\rm ds}} - \frac{\partial I_0}{\partial V_{\rm ds}}\right)e^{-\frac{t}{\tau_1}} \tag{3.51}$$

3.5.2 Single Time-Constant Dispersion Model

The model circuit used to obtain the assumed dispersive drain current characteristics is shown in Fig. 3.14.

In parallel to the static current source I_0, an additional dispersion current is advantageously formed by a voltage-controlled current source $(V_{\rm x}/R_{\rm x})$, which translates a nonlinear voltage $V_{\rm x}$, obtained from a parallel L-R circuit, into current. The total drain current $I_{\rm ds}$ of the proposed topology can then be written as

$$I_{\rm ds} = I_0 + \frac{1}{R_{\rm x}}V_{\rm x} = I_0 + I_{\rm x}\frac{j\omega L_{\rm x}}{R_{\rm x} + j\omega L_{\rm x}} \tag{3.52}$$

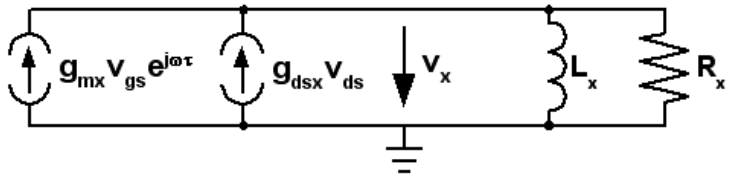

Figure 3.15: Linearisation of the dispersion model. Dispersion part only.

where I_0 and I_x are controlled by two voltages:

$$I_0, I_\mathrm{x} = f\left(V_\mathrm{gs}, V_\mathrm{ds}\right) \tag{3.53}$$

The dispersion current source is set to

$$I_\mathrm{x} = I_1 - I_0 \tag{3.54}$$

The linearised small-signal representation of the dispersion model is shown in Fig. 3.15. Output related Y-parameters of the circuit are found to be

$$\begin{aligned} Y_{21} &= \frac{\partial I_0}{\partial V_\mathrm{gs}} + \frac{1}{R_\mathrm{x}}\frac{\partial V_\mathrm{x}}{\partial V_\mathrm{gs}} \\ &= g_\mathrm{m0} + g_\mathrm{mx} - g_\mathrm{mx}\frac{R_\mathrm{x}}{L_\mathrm{x}} \cdot \frac{1}{\frac{R_\mathrm{x}}{L_\mathrm{x}} + j\omega} \end{aligned} \tag{3.55}$$

$$\begin{aligned} Y_{22} &= \frac{\partial I_0}{\partial V_\mathrm{ds}} + \frac{1}{R_\mathrm{x}}\frac{\partial V_\mathrm{x}}{\partial V_\mathrm{ds}} \\ &= g_\mathrm{ds0} + g_\mathrm{dsx} - g_\mathrm{dsx}\frac{R_\mathrm{x}}{L_\mathrm{x}} \cdot \frac{1}{\frac{R_\mathrm{x}}{L_\mathrm{x}} + j\omega} \end{aligned} \tag{3.56}$$

Equation (3.55) neglects the non-quasi static effect of drain current time delay τ, which only has an impact at microwave frequencies (see chapter 3.3.1). The right-hand terms in (3.55) and (3.56) can easily be transformed into time domain using Fourier transformation and the Dirac pulse function $\delta(t)$. The resulting pulse responses $h_\mathrm{Y21}(t)$ and $h_\mathrm{Y22}(t)$ of the linearised drain current due to a change in controlling voltages are:

$$h_\mathrm{Y21}(t) = \delta(t)\left(g_\mathrm{m0} + g_\mathrm{mx}\right) - s(t)\left(g_\mathrm{mx}\frac{R_\mathrm{x}}{L_\mathrm{x}}\right) e^{-\frac{t}{L_\mathrm{x}/R_\mathrm{x}}} \tag{3.57}$$

$$h_\mathrm{Y22}(t) = \delta(t)\left(g_\mathrm{ds0} + g_\mathrm{dsx}\right) - s(t)\left(g_\mathrm{dsx}\frac{R_\mathrm{x}}{L_\mathrm{x}}\right) e^{-\frac{t}{L_\mathrm{x}/R_\mathrm{x}}} \tag{3.58}$$

The equivalent circuit satisfies the initial assumption of a single-pole circuit response, i. e. equations (3.57) and (3.58) equal equations (3.50) and (3.51) for $(\partial I_1/\partial V_\mathrm{gs}) = g_\mathrm{m0} + g_\mathrm{mx}$, $(\partial I_0/\partial V_\mathrm{gs}) = g_\mathrm{m0}$, $(\partial I_1/\partial V_\mathrm{ds}) = g_\mathrm{ds0} + g_\mathrm{dsx}$, $(\partial I_0/\partial V_\mathrm{ds}) = g_\mathrm{ds0}$ and $\tau_1 = (1/\omega_1) = (L_\mathrm{x}/R_\mathrm{x})$. Here, $\omega_1 = 2\pi f_1$ can be defined as the corner frequency of the dispersion effect. The dispersion time constant can therefore be controlled by an appropriate choice of $(L_\mathrm{x}/R_\mathrm{x})$.

Compared to the conventional approach, which combines static and dynamic sources via

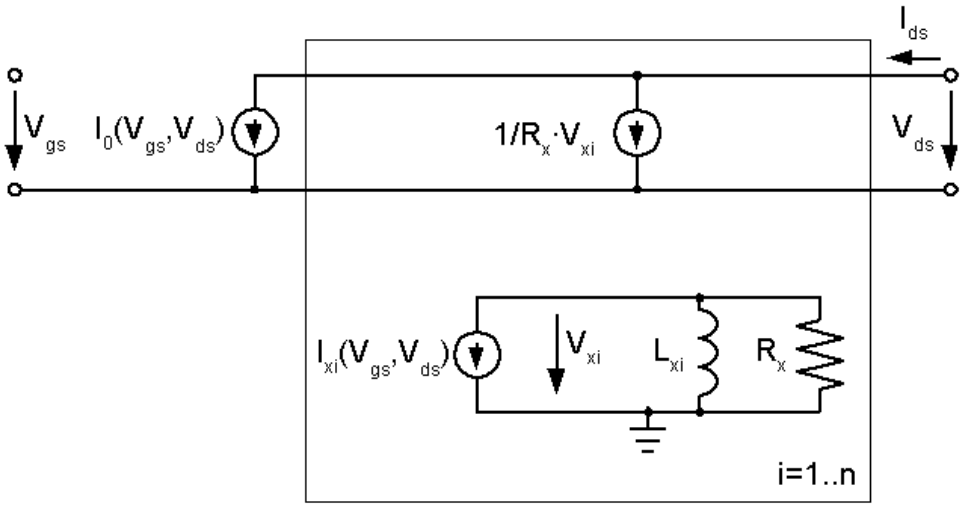

Figure 3.16: Incorporation of several dispersion sources within the model topology.

an R-C circuit topology (see chapter 2.3.2 and Fig. 2.5), this model offers higher accuracy and computational efficiency. The R-C type model requires a conductance G_x to assure convergence. This is eliminated in the new model. Additionally, G_x in the conventional model introduces an error to output conductance:

$$Y_{22} = g_{\mathrm{ds0}} + (g_{\mathrm{dsx}} + G_\mathrm{x}) \cdot \frac{j\omega}{\frac{G_\mathrm{x}}{C_\mathrm{x}} + j\omega} \tag{3.59}$$

Above the corner frequency $\omega = (G_\mathrm{x}/C_\mathrm{x})$, when C_x represents a short circuit, G_x adds to the total output conductance.

3.5.3 Multiple Time-Constants

Individual dispersion effects with different time constants can be incorporated in the model by using several dispersion sources in parallel, as shown in Fig. 3.16.

The total drain current now is

$$I_{ds} = I_0 + \sum_{i=1..\mathrm{n}} I_{\mathrm{x}i} \frac{j\omega L_{\mathrm{x}i}}{R_\mathrm{x} + j\omega L_{\mathrm{x}i}} \tag{3.60}$$

where n is the number of dispersion sources and

$$I_{\mathrm{x}i} = I_i - I_{i-1},\ i = 1..\mathrm{n} \tag{3.61}$$

is the current attributed to dispersion source i. The choice of $(L_{\mathrm{x}i}/R_\mathrm{x})$ leads to the respective time constants of dispersion source i. For simplicity's sake, all dispersion sources use a constant value of $R_\mathrm{x} = 1\,\Omega$, while the inductor value sets the time constant. Trans-

and output conductance of the circuit now become

$$Y_{21} = g_{\mathrm{m}} + \sum_{i=1..\mathrm{n}} g_{\mathrm{mx}i} \frac{j\omega L_{\mathrm{x}i}}{R_{\mathrm{x}} + j\omega L_{\mathrm{x}i}} \tag{3.62}$$

$$Y_{22} = g_{\mathrm{ds}} + \sum_{i=1..\mathrm{n}} g_{\mathrm{dsx}i} \frac{j\omega L_{\mathrm{x}i}}{R_{\mathrm{x}} + j\omega L_{\mathrm{x}i}} \tag{3.63}$$

The parallel placement of several dispersion sources and the current definition of (3.61) will lead to a total drain current in the frequency domain of I_i for $\omega_i < \omega < \omega_{i+1}$, where $\omega_i = (L_{\mathrm{x}i}/R_{\mathrm{x}})^{-1}$ are the corner frequencies of the individual dispersion sources as deduced above. The dispersion sources are numbered with increasing corner frequency: $\omega_i > \omega_{i-1}$, that means $L_{\mathrm{x}i} < L_{\mathrm{x},i-1}$. Small-signal conductances of the circuit result accordingly.

3.5.4 Determination of Dispersion Time Constants

The current sources I_i in the multiple time constant model represent the nonlinear IV characteristics under different dynamic conditions. While I_0 describes static conditions, where all dispersion effects adapt to every voltage condition, the dynamic sources $I_{1..\mathrm{n}}$ describe characteristics which comprise dispersion effects with certain high corner frequencies, but exclude others with lower corner frequency. For example, the first dispersion source I_1, with associated time constant τ_1, differs from the static one by eliminating dispersion effects with time constant τ_1, but still containing all other effects with a smaller associated $\tau_{i>1}$ and higher corner frequencies.

In the following, the methods to obtain the different dynamic IV characteristics I_i are described. Also, by using the obtained model in simulation, it is shown that the proposed model accurately reflects the measured dispersion characteristics.

Time-Domain Characterisation

Pulsed-IV measurements, as described in chapter 2.5.1, are carried out with varying pulse width. Plotting the drain current in a certain voltage point A versus pulse width yields the transient step response of the device. This is shown in Fig. 3.17 for a $2\,\mathrm{x}\,20\,\mu$m GaAs device (PH15) being pulsed from a saturated quiescent condition $Q = (0\,V_{\mathrm{gs}},\, 2\,V_{\mathrm{ds}})$ to $A1 = (0.8\,V_{\mathrm{gs}},\, 3.5\,V_{\mathrm{ds}})$ and $A2 = (0.2\,V_{\mathrm{gs}},\, 0.6\,V_{\mathrm{ds}})$.

One observes a current response corresponding to two exponentially decaying functions with time constants $\tau_1 = 200\,\mu$s and $\tau_2 = 1\,\mu$s. The function used to describe this transient characteristic is

$$I_{\mathrm{ds}}(t) = I_0 + (I_1 - I_0)\, e^{-\frac{t}{\tau_1}} + (I_2 - I_1)\, e^{-\frac{t}{\tau_2}} \tag{3.64}$$

Applying this function over the whole IV plane results in the two nonlinear dynamic current sources I_1 and I_2.

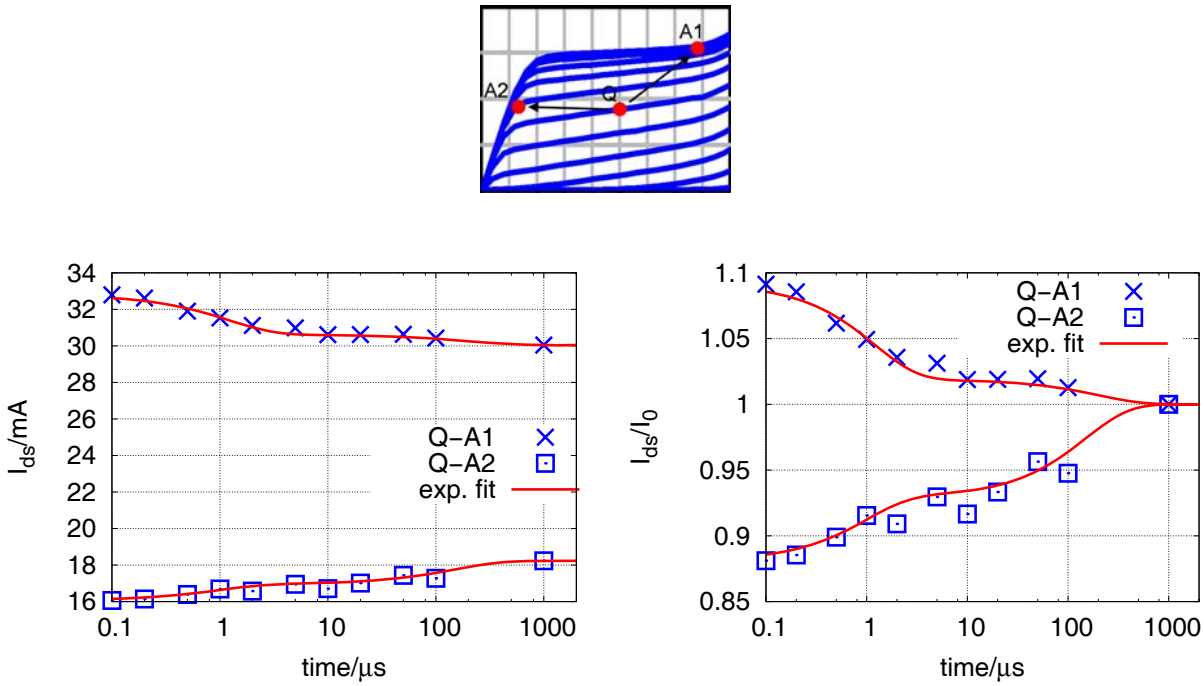

Figure 3.17: $2\,\mathrm{x}\,20\,\mu$m GaAs pHEMT. Left: Measured drain current pulse response for pulses from $Q = (0\,V_{\mathrm{gs}},\, 2\,V_{\mathrm{ds}})$ to $A1 = (0.8\,V_{\mathrm{gs}},\, 3.5\,V_{\mathrm{ds}})$ and $A2 = (0.2\,V_{\mathrm{gs}},\, 0.6\,V_{\mathrm{ds}})$. Right: Normalized to static current I_0. Lines: fit using two exponentially decaying functions.

Trapping- and de-trapping effects are mainly associated with the short time constant dispersion, whereas the large time constant effects are usually associated with thermal dispersion. Since the two time constants are separated by about two orders of magnitude, it is also possible to directly attribute a medium pulse width IV characteristic to the dynamic I_1 in the model, instead of using equation (3.64). Here, the dispersion effect(s) responsible for the fast change in current have adapted and allowed the current to settle at the intermediate value before the final with a larger time constant. In the case of the GaAs pHEMT, this is true for pulse widths of $t_{\mathrm{pulse}} \approx 2\,\mu$s:

$$I_1 \approx I_{\mathrm{ds,ac}}|_{t_{\mathrm{pulse}}=2\,\mu\mathrm{s}} \tag{3.65}$$

The second dispersion source describes the current characteristics obtained with minimum pulse widths:

$$I_2 \approx I_{\mathrm{ds,ac}}|_{t_{\mathrm{pulse}}=0.1\,\mu\mathrm{s}} \tag{3.66}$$

Both current characteristics are now modelled by an individual set of parameters for the modified COBRA drain current equation. The model is extracted from and will be valid under a “hot”, i.e. conducting and saturated quiescent condition, corresponding to a class A operation of the device. The resulting IV characteristics for I_1 and I_2 of a $2\,\mathrm{x}\,20\,\mu$m PH15 transistor are shown in Fig. 3.18 together with the static curves.

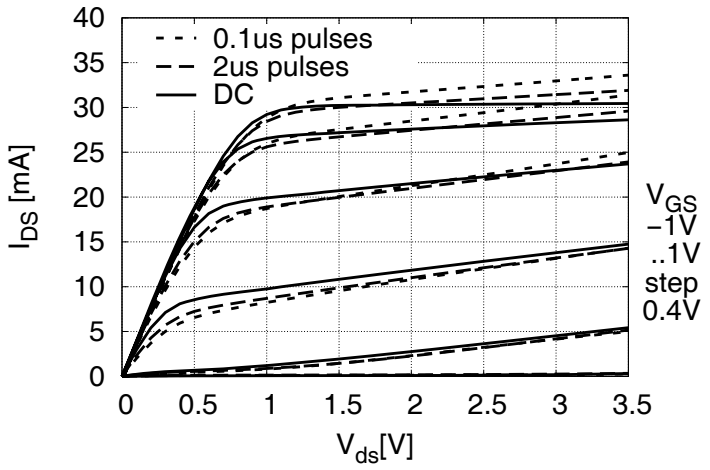

Figure 3.18: The three modelled dynamic IV characteristics of a $2\,\mathrm{x}\,20\,\mu$m GaAs pHEMT (PH15) based on pulsed measurements with different pulse widths.

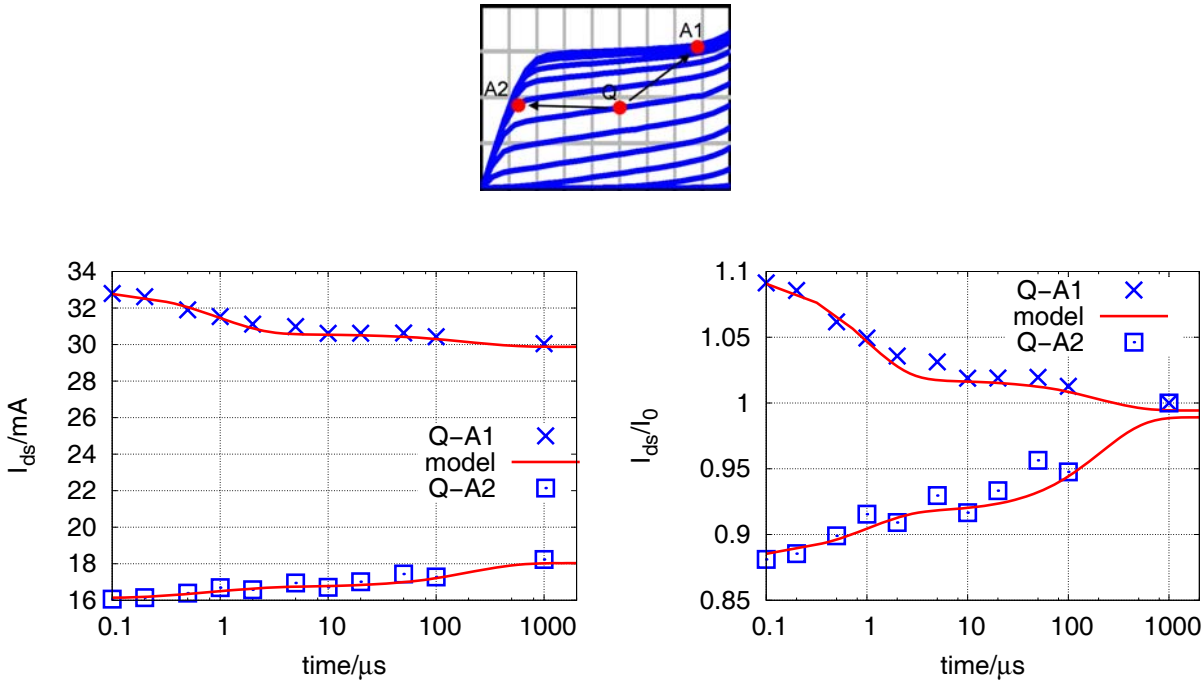

Figure 3.19: Transient step response of drain current when stepping from $Q = (0\,V_{\mathrm{gs}},\, 2\,V_{\mathrm{ds}})$ to $A1 = (0.8\,V_{\mathrm{gs}},\, 3.5\,V_{\mathrm{ds}})$ and $A2 = (0.2\,V_{\mathrm{gs}},\, 0.6\,V_{\mathrm{ds}})$. Measurement (dots) and modelled values (lines).

The model in its fully implemented form (see chapter 3.7) may now be used in a transient analysis to simulate the step response of the drain current, similar to the transient measurement technique presented above. The result is shown in Fig. 3.19 for the $2\,\mathrm{x}\,20\,\mu$m PH15 device. As derived in the modelling approach, the drain current answers with exponentially decaying characteristics in the time domain, of which two are visible on the μs time scale. Comparison to the measured values shows good agreement. In qualitative terms, this confirms the modelling approach and the assumption of exponential dispersion characteristics. In quantitative terms, the agreement between measurement and model confirms the suitability of the employed nonlinear current expression.

Frequency-Domain Characterisation

The use of pulsed IV measurements allows for the exclusion of dispersion effects with time constants larger than the minimum pulse length. Some dispersion effects, however, like e. g. impact ionisation current, show time constant orders of magnitude smaller, with corresponding cutoff frequencies lying well in the GHz-range.

The method employed for describing dynamic IV characteristics in the microwave regime therefore is that of numerical integration of transconductance g_m and output conductance g_ds as described in chapter 2.5.2. Since, even at microwave frequencies, g_m and g_ds result from linearisation of a nonlinear drain-source current in the transistor (compare equation (2.9)), it makes sense to describe this current by the same analytical expression used for modelling static and pulsed-IV characteristics, i.e. by a set of parameters for the nonlinear COBRA expression.

In chapter 2.5.2, the resulting IV characteristics were shown for the SiGe mHEMT. Here, this method is applied to a 2x40 μm InP- and 2x20 μm PH15 device, leading to the IV characteristics shown in Fig. 3.20.

Both in the GaAs- and InP device, a significant difference between the dynamic IV obtained from pulsed measurements with minimum pulse width and those obtained from numerical integration is observed. In the GaAs pHEMT, the main effect can clearly be linked to the onset of impact ionisation, which has disappeared in the numerically integrated characteristics. The InP device also shows reduced output conductance in the numerically integrated characteristics. However, here the responsible physical effect might be impact ionisation or the formation of parasitic channels in the device. Being of empirical nature, the presented modelling method allows for physical interpretation only in the sense of interpreting the impact of dispersion effects with different time constants on drain current characteristics, e.g. the reduction of output conductance. The physical nature of individual dispersion effects is not considered.

The model is also used for simulating S-parameters and comparing them to measurements. For both the GaAs-based and the InP-based device, bias conditions are chosen where the impact of high frequency dispersion is important. Dispersion effects show up noticeably in S_{21} and S_{22}. Fig. 3.21 shows the GaAs pHEMT biased in $Q = (0.2\,V_\mathrm{gs},\, 3.9\,V_\mathrm{ds})$. Fig. 3.22

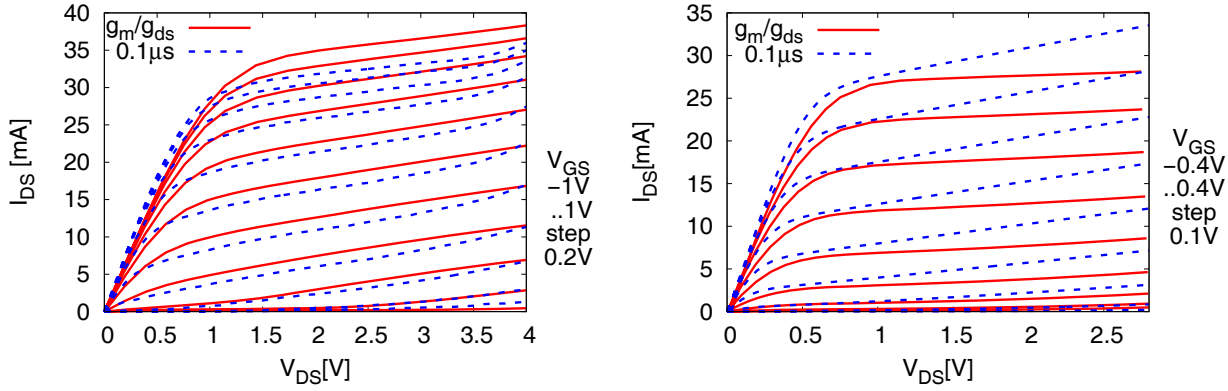

Figure 3.20: Modelled dynamic IV obtained from numerical integration of multi-bias transconductance and output conductance information for frequencies beyond 5GHz. Left: 2 x 20 μm PH15. Right: 2 x 40 μm InP pHEMT. Comparison to pulsed-IV with 0.1 μs pulse width.

is for the InP device biased in a more typical point $Q = (0.1\,V_{\rm gs},\ 2.8\,V_{\rm ds})$ which corresponds approximately to maximum gain $g_{\rm m,max}$. Effects of dispersion on S_{21} and S_{22} are enlarged.

In addition to the dispersion model, the simulation results obtained from non-dispersive models are included. Here, the dispersion part of the drain current model has been disabled, and the current source I_0 models either the purely static (DC) or the purely dynamic (from $g_{\rm m}/g_{\rm ds}$ integration) IV characteristics (see chapter 3.7.2).

The S-parameter characteristics, when translated into Y-parameters, correspond to the frequency response derived in (3.55) and (3.56), confirming the exponential character even of those dispersion effects with very small time constants. Fig. 3.23 shows the output conductance ($\approx \Re(Y_{22})$) and transconductance ($\approx \Re(Y_{21})$) at moderate frequencies. The corner frequency of the third dispersion source which describes the microwave frequency IV characteristics is derived from the Y-parameters and found to be

$$f_{3,\rm GaAs} = (2\pi\tau_{3,\rm GaAs})^{-1} = 560\,\rm MHz \tag{3.67}$$

$$f_{3,\rm InP} = (2\pi\tau_{3,\rm InP})^{-1} = 270\,\rm MHz \tag{3.68}$$

The difference between the measured and modelled twoport parameters stems from the fact that a linearised large-signal model will never be as accurate as the corresponding small-signal model in a particular bias point. In fact, using the small-signal model, one can perfectly match the model to the measured S-parameters.

Nonlinear Drain Current Models

Finally, all dynamic IV characteristics are modelled via a separate parameter set for the modified COBRA model. Based on the extraction methods described above, a full dispersion

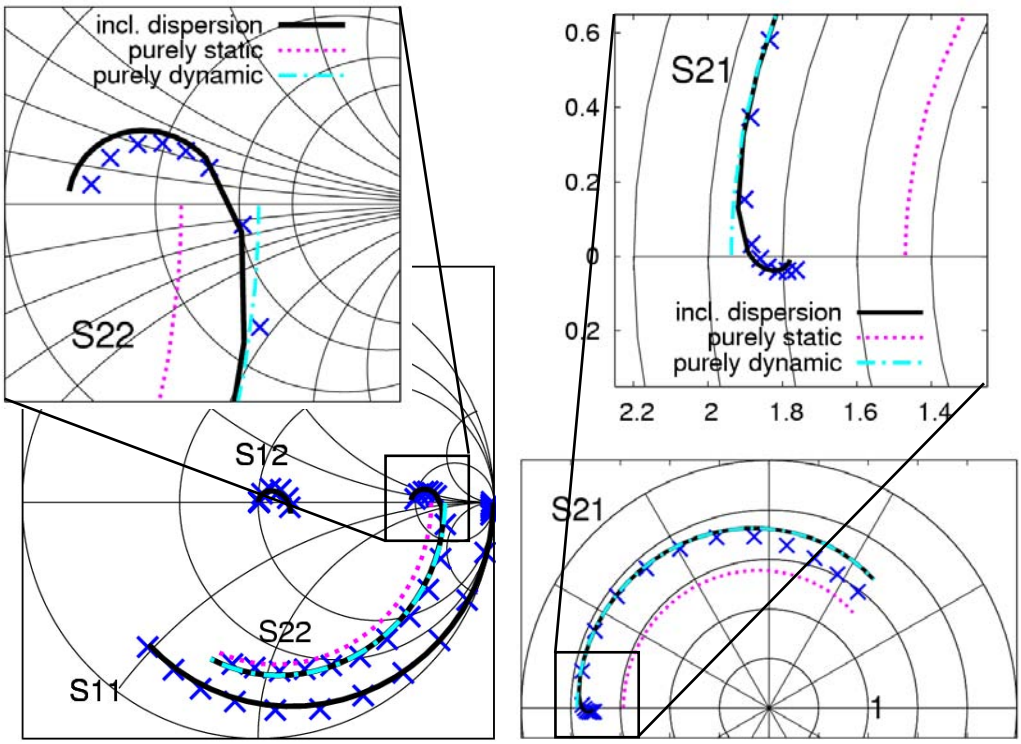

Figure 3.21: S-parameters (50 MHz - 50 GHz) of a $2 \times 20\,\mu$m GaAs pHEMT (PH15) under bias conditions $Q = (0.2\,V_{\mathrm{gs}},\ 3.9\,V_{\mathrm{ds}})$. Measurements (symbols) and model (lines).

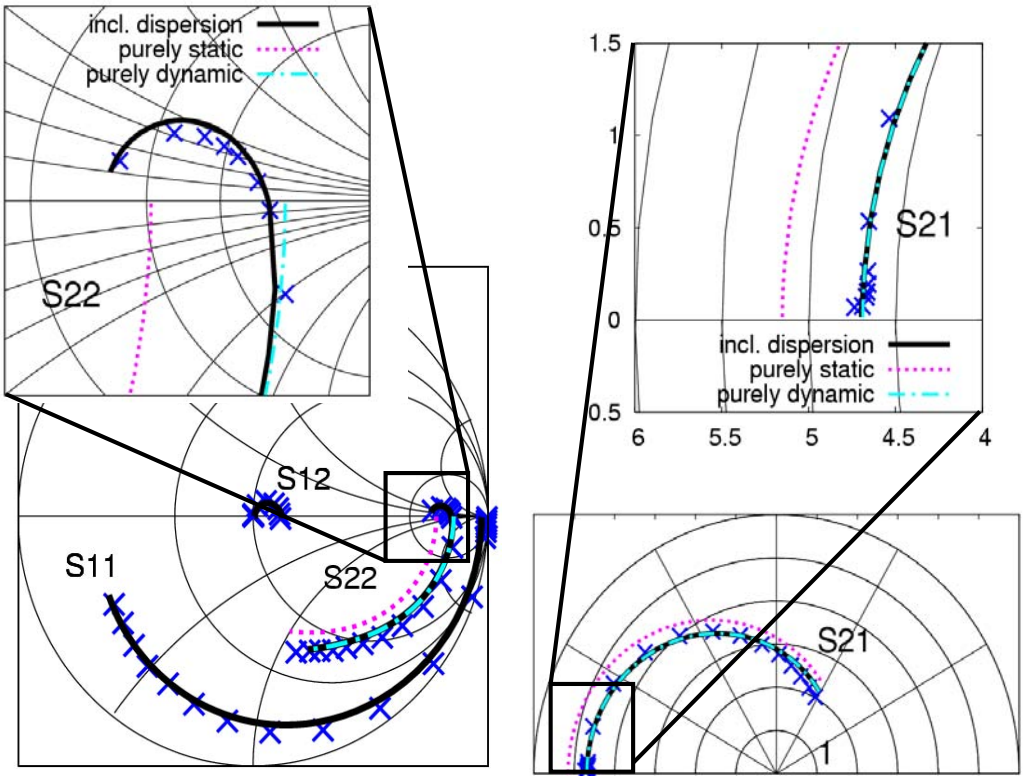

Figure 3.22: S-parameters (50 MHz - 50 GHz) of a $2 \times 40\,\mu$m InP pHEMT under bias conditions $Q = (0.1\,V_{\mathrm{gs}},\ 2.8\,V_{\mathrm{ds}})$. Measurements (symbols) and model (lines).

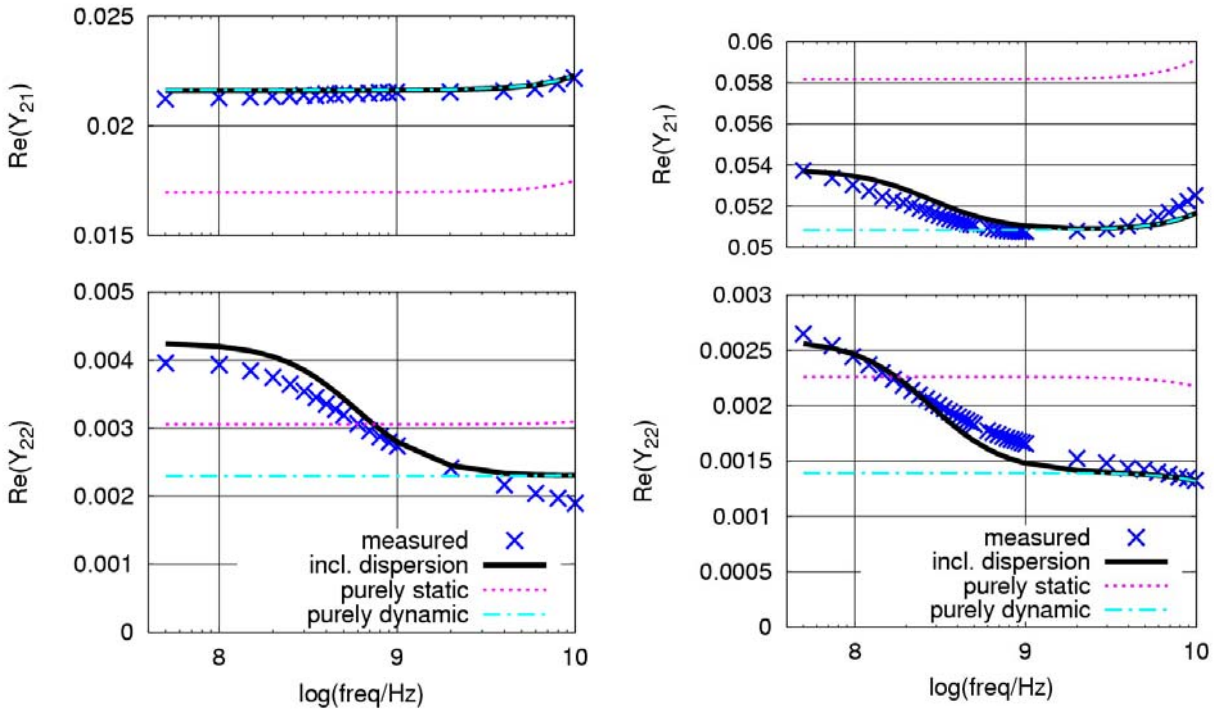

Figure 3.23: The frequency dependence of the output related Y-parameters reveals the corner frequency in the microwave range. Left: 2x20 μm GaAs pHEMT device (PH15) under bias conditions $Q = (0.2\,V_{\mathrm{gs}},\ 3.9\,V_{\mathrm{ds}})$. Right: 2x40 μm InP pHEMT with bias conditions $Q = (0.1\,V_{\mathrm{gs}},\ 2.8\,V_{\mathrm{ds}})$.

Parameter	I_{ds}	I_{dsac1}	I_{dsac2}	I_{dsac3}
τ_i	-	200 μs	1 μs	284 ps
f_i	-	800 Hz	160 kHz	560 MHz
β	$2.75 \cdot 10^{-2}$	$2.72 \cdot 10^{-2}$	$2.83 \cdot 10^{-2}$	$3.06 \cdot 10^{-2}$
V_{to}	-0.54	-0.47	-0.44	-0.45
λ	1.22	1.10	1.13	0.94
α	7.32	5.23	4.62	2.80
μ	$-7.50 \cdot 10^{-3}$	$-7.56 \cdot 10^{-3}$	$-1.90 \cdot 10^{-2}$	$-1.47 \cdot 10^{-2}$
γ	$1.16 \cdot 10^{-1}$	$1.25 \cdot 10^{-1}$	$1.45 \cdot 10^{-1}$	$1.25 \cdot 10^{-1}$
δ	$1.01 \cdot 10^{-1}$	$1.03 \cdot 10^{-1}$	$1.14 \cdot 10^{-1}$	$8.50 \cdot 10^{-2}$
ξ	1.64	1.69	1.73	0.83
ζ	$-3.18 \cdot 10^{-1}$	$-1.94 \cdot 10^{-1}$	$-1.91 \cdot 10^{-1}$	$-1.48 \cdot 10^{-1}$
η	1.50	1.50	1.59	1.22
π_{eff}^{-1}	0.81	0	0	0

Table 3.2: Dispersion drain current model parameters of the 2 x 20 μm PH15 GaAs pHEMT.

model can contain three dynamic sources: two pulsed-IV characteristics obtained with short and long pulses, and a third derived from dynamic $g_{\mathrm{m}}/g_{\mathrm{ds}}$ integration. A simplified model, making use of fewer dispersion sources, may also be used. For example, the model may be built entirely on static and pulsed-IV characteristics, avoiding the error introduced in the numerical integration process (see chapter 2.5.2), but sacrificing the inclusion of sub-μs dispersion time constants. Also, the two time constants in pulsed-IV may not be clearly distinguishable, for example due to insignificant thermal dispersion in the device. Then, a single pulsed-IV characteristic, e.g. with minimal pulse width, can be employed.

Detailed dynamic drain current models and parameter values for all technologies are listed in Appendix C. As an example, table 3.2 shows the drain current parameter sets of a 2 x 20 μm PH15 transistor: static and three dispersion sources with their respective dispersion time constants. The impact of dispersion on the device's drain current is reflected in the evolution of the model parameters. For example, consistent with HEMT theory [32], the threshold voltage (parameter V_{to}) is reduced in the dynamic case. The difference in the linear operating region is taken into account mainly by parameter α, which decreases with increasing corner frequency. The reduced output conductance of static characteristics, mainly associated with the self-heating effect, is contained in a smaller value of γ in the static parameter set when compared to the dynamic ones.

It should be noted that the proposed concept allows for the inclusion of nonlinearities, i.e. voltage dependencies, of individual dispersion time constants. In time domain characterisation, this is done by fitting equation (3.64) over the whole IV plane, thereby obtaining voltage dependencies of τ_1 and τ_2 in addition to those of current. In frequency domain characterisation, one extracts different values of f_3 under different bias conditions. Such a nonlinearity of time constants could then be described in the model by using nonlinear capacitors $C_{\mathrm{x}i} = f\left(V_{\mathrm{gs}}, V_{\mathrm{ds}}\right)$. None of the devices investigated in this work, however, revealed

significant variations of time constants with voltage, and this additional nonlinearity wasn't pursued further.

3.6 Parameter Extraction Software FETfit

The software package "FETfit" has been developed in the course of this work to assist in parameter extraction of the full custom model. It consists of a combination of linear- and nonlinear FET circuit simulators and a parameter optimization tool. The software was built based on original code developed at University College Dublin [112] and developed into a multi-functional parameter extraction tool. A graphical user interface (GUI) allows for control of all relevant parameters during the model extraction process.

Fig. 3.24 shows a flowchart of the FETfit main program as well as major input- and output files. Three major blocks, "nonlinear DC", "multi-bias linear AC" and "nonlinear AC" are run sequentially. Each block performs the following:

- default simulation based on initial model parameter settings
- input of measured data and table-based small-signal model data
- optimisation of individual parameters or groups of parameters, i.e. fitting of simulated to measured data.

Parameter optimisation uses an implementation of the Marquardt-Levenberg algorithm [99, 100] to find an optimum set of parameters for minimizing an error function, defined by the user.

Additional program features include the automatic generation of table-based small-signal model files based on the advanced de-embedding technique (chapter 3.1) and analytical calculation of internal Y-parameters (chapter 3.3.1). This file may serve directly as input to the nonlinear AC optimisation part or as initial solutions to the multi-bias linear AC block. Fig. 3.25 shows a screenshot of the FETfit GUI.

FETfit has been contributed to the TARGET network of excellence (NoE) design software pool [113], including a complete documentation of the software. In addition to the SiGe-, GaAs- and InP HEMTs investigated in this work, the software assisted in extracting the model parameters for diamond-based FETs [114, 115, 116] as well as RF-CMOS transistors [117].

3.7 Model Implementation

In order to use the model in the design of integrated circuits, it needs to be incorporated into a circuit simulation environment. Therefore, the presented custom FET model, including all of its nonlinear static-, dynamic-, frequency dispersion- and scaling features, has been implemented into the Agilent Advanced Design System (ADS) simulator.

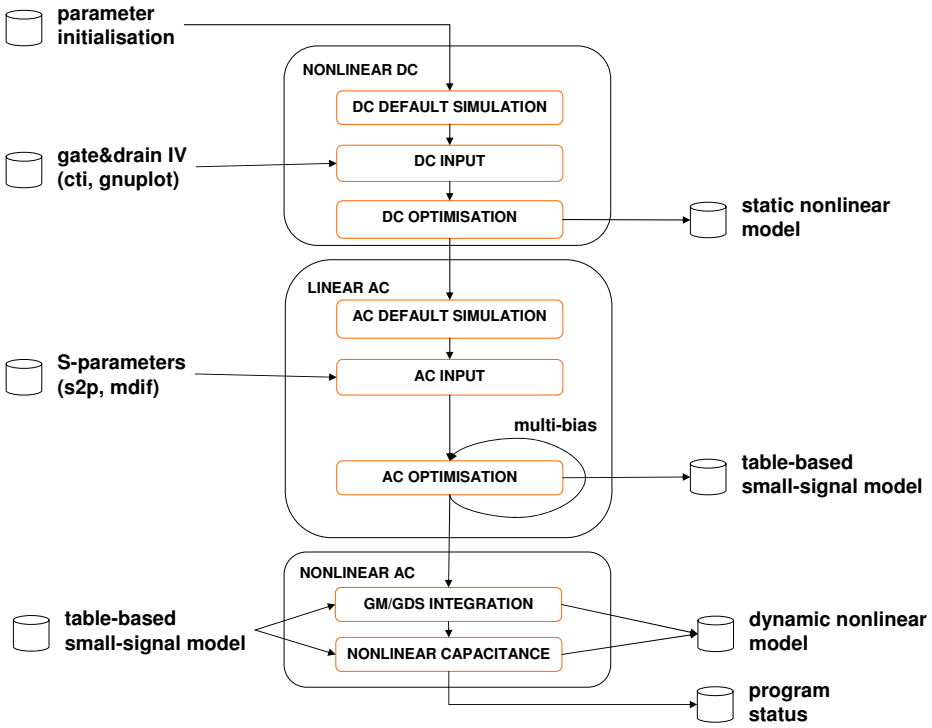

Figure 3.24: FETfit flowchart and major input- and output files.

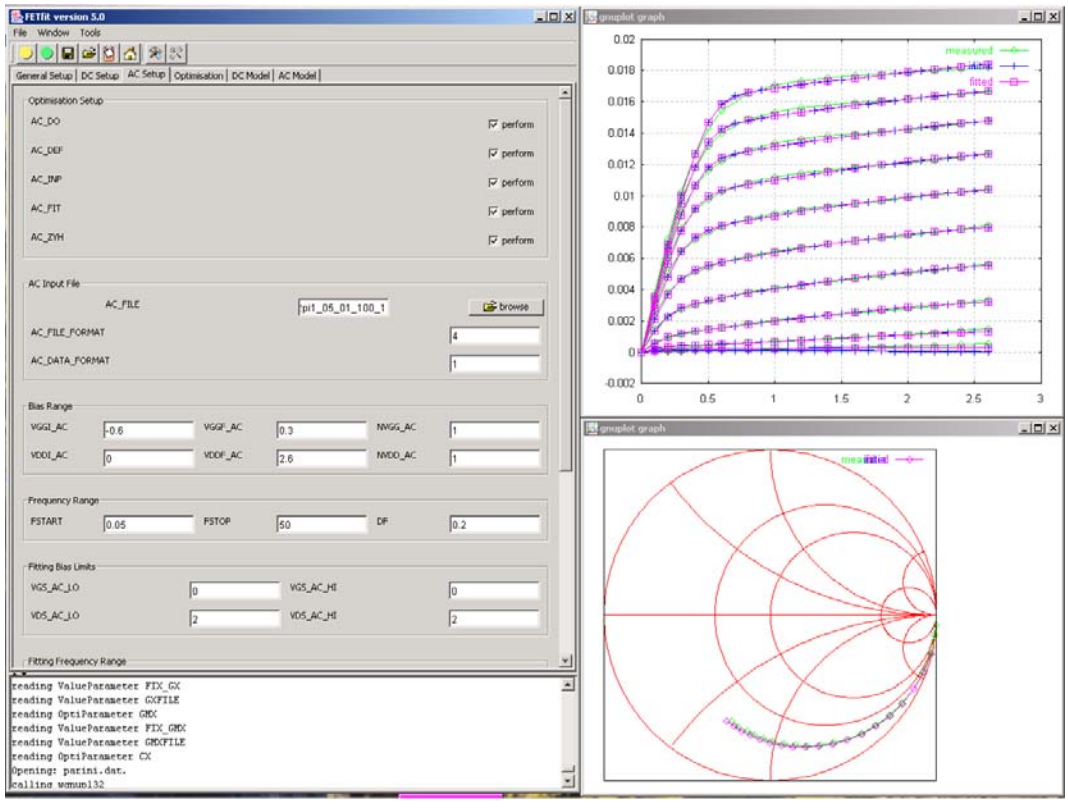

Figure 3.25: Parameter extraction software FETfit. Screenshot of the GUI.

The implementation is carried out in "user-compiled" form [118]. Here, the model topology and nonlinear equations are implemented in the C programming language using ADS interface routines. Such a model type can provide full simulation functionality, i.e. it can implement linear and nonlinear time- and frequency domain models. Compared to the "symbolically-defined device" (SDD) model frequently encountered in custom models, the user-compiled model type offers full control over the model behaviour in simulation. It is also found to be computationally more efficient and more stable with respect to convergence under nonlinear conditions.

With the exception of noise simulations, all circuit analysis techniques in the time- and frequency domain can be performed by the model in its present form. Among its non-standard implementation features are:

- Nonlinear capacitance description realised by an equivalent-circuit topology (see chapter 3.7.1). The standard charge-oriented implementation can be enabled by a schematic level parameter.

- Implementation of drain current time delay τ in transient analysis, adopting the approach taken in [119]. During transient analysis, the model saves the controlling gate voltage of individual time steps in a linked-list data structure. The delayed voltage may then be recalled and interpolated to calculate $I_{\mathrm{ds}}\left(V_{\mathrm{gs}}\left(t-\tau\right), V_{\mathrm{ds}}\right)$.

- The dispersion model may be enabled or disabled by appropriate choice of a schematic level parameter. Purely static and purely dynamic model characteristics can thus be obtained.

By default, a simple linear scaling measure is employed to provide simulation capability for different gate widths and varying number of gate fingers. Scaling rules for resistance, nonlinear current and nonlinear capacitance are listed in Appendix B.

3.7.1 Implementation of nonlinear capacitance

In SPICE-like model implementations - and ADS follows that philosophy, too - nonlinear capacitance is implemented in terms of voltage-dependent charge between two terminals. As a consequence, one has to go to extreme lengths to use this approach for implementing the gate charge or the combination of C_{gs} and C_{gd} of a transistor. The reason is that the gate charge expression, physically arising from a single channel charge, has to be divided into two charge expressions Q_{gs} and Q_{gd}, which will be attributed to the gate-source and gate-drain terminals, respectively. One can avoid this tedious and physically unintentional process by replacing the nonlinear capacitors by an equivalent circuit consisting of nonlinear, voltage-controlled current sources and a linear inductor, i.e. a gyrator principle. While this equivalent circuit can easily be implemented in the simulator, one must be aware that

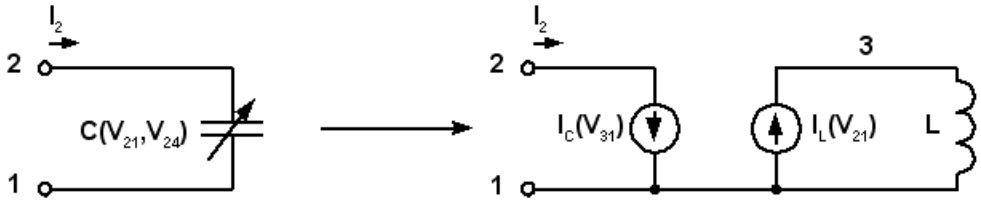

Figure 3.26: Equivalent Circuit for Nonlinear Capacitors.

- An additional nonlinear circuit node is required. This node is of "virtual" nature, i.e. it cannot be traced back to the device geometry.
- Since no charge expression is required anymore for implementing the nonlinear capacitors, one needs to make sure that the capacitance expressions employed satisfy the charge-conservation criterion. The model will compile without problem, but the simulator might not converge during large-signal simulations due to the violation of charge conservation.
- The use of nonlinear, voltage-controlled current sources requires implementation of its transconductance elements. This will lead to the computation of the partial derivatives of the nonlinear capacitor against its controlling voltages (see below).

Fig. 3.26 shows the equivalent circuit employed in the model.

The required electrical behaviour between nodes 2 and 1 is

$$I_2 = j\omega C(V_{21},\, V_{24}) \cdot V_{21} \tag{3.69}$$

where V_{21} and V_{24} are the two controlling voltages of the nonlinear capacitor. In the case of the gate-source capacitor, for instance, node 2 would be the gate terminal, node 1 and 4 the source- and drain terminals, respectively. Node 3 is the virtual node for the calculation. Node 4 is not shown in Fig. 3.26. This can be achieved by attributing the following characteristics to the nonlinear voltage-controlled current sources:

$$I_{\mathrm{C}}(V_{31}) = C^*(V_{21}, V_{24}) \cdot V_{31} \tag{3.70}$$

$$I_{\mathrm{L}}(V_{21}) = \frac{1}{L^*} \cdot V_{21} \tag{3.71}$$

where $C^* = C/1\,\mathrm{s}$ and $L^* = L/1\,\mathrm{s}$ to guarantee conformity of units. Equations (3.78) and (3.79) form the basic assumptions for the equivalent circuit with a constant inductor L.

Then,

$$V_{31} = j\omega L \cdot I_{\mathrm{L}} = j\omega L \cdot \frac{1}{L^*} V_{21} = j\omega \cdot 1\,\mathrm{s} \cdot V_{21} \tag{3.72}$$

$$I_2 = I_\mathrm{C} = C^*(V_{21},\, V_{24}) \cdot j\omega \cdot 1\,\mathrm{s} \cdot V_{21} = j\omega C(V_{21},\, V_{24}) \cdot V_{21} \tag{3.73}$$

In this case, transconductances of the nonlinear current sources become:

$$\frac{\partial I_\mathrm{C}}{\partial V_{31}} = C^*(V_{21},\, V_{24}) \tag{3.74}$$

$$\frac{\partial I_\mathrm{C}}{\partial V_{21}} = V_{31} \cdot \frac{\partial C^*(V_{21},\, V_{24})}{\partial V_{21}} \tag{3.75}$$

$$\frac{\partial I_\mathrm{C}}{\partial V_{24}} = V_{31} \cdot \frac{\partial C^*(V_{21},\, V_{24})}{\partial V_{24}} \tag{3.76}$$

$$\frac{\partial I_\mathrm{L}}{\partial V_{21}} = \frac{1}{L^*} \tag{3.77}$$

This way of implementing a nonlinear capacitor therefore requires calculation of the partial derivatives of the capacitor against its two controlling voltages. An alternative implementation resulting in the same nodal behaviour can be:

$$I_\mathrm{C}(V_{31}) = \frac{1}{L^*} \cdot V_{31} \tag{3.78}$$

$$I_\mathrm{L}(V_{21}) = C^*(V_{21},\, V_{24}) \cdot V_{21} \tag{3.79}$$

Now,

$$V_{31} = j\omega L \cdot C^*(V_{21},\, V_{24}) \cdot V_{21} \tag{3.80}$$

$$I_2 = I_\mathrm{C} = \frac{1}{L^*} \cdot j\omega L \cdot C^*(V_{21},\, V_{24}) \cdot V_{21} = j\omega C(V_{21},\, V_{24}) \cdot V_{21} \tag{3.81}$$

The required transconductanes now are:

$$\frac{\partial I_\mathrm{C}}{\partial V_{31}} = \frac{1}{L^*} \tag{3.82}$$

$$\frac{\partial I_\mathrm{L}}{\partial V_{21}} = C^*(V_{21},\, V_{24}) + \frac{\partial C^*(V_{21},\, V_{24})}{\partial V_{21}} \cdot V_{21} \tag{3.83}$$

$$\frac{\partial I_\mathrm{L}}{\partial V_{24}} = V_{21} \cdot \frac{\partial C^*(V_{21},\, V_{24})}{\partial V_{24}} \tag{3.84}$$

While this implementation also requires the partial derivatives of the capacitor, only three transconductance elements are required.

Both solutions result in the desired electrical behaviour for the nonlinear capacitor. Since no significant reduction of computational speed can be expected from the latter, both approaches can be considered to be equivalent.

Parameter	Description
TAMB	ambient temperature [K]
WU	unit width of gate finger [μm]
N	number of gate fingers
VIA	via hole, for microstrip technologies with backside metallisation
FET	identifier of FET model parameter set
TR_TIME_DELAY	enable/disable transient time delay model
DISPMODEL	enable/disable dispersion model
CAPMODEL	enable/disable nonlinear capacitance model

Table 3.3: Schematic level parameters of the model implementation in Agilent ADS.

3.7.2 Schematic level parameters

The fully implemented HFET model can now be used in all types of circuit analysis, both in the frequency- and time domain. In the following, it is used for linear- and nonlinear model verification as well as the design of MMIC applications.

The model is made available in ADS through a design kit according to [120]. Fig. 3.27 shows a screenshot of an ADS schematic window, including the design kit and model symbols as well as the available design parameters editable from the schematic. While this version of the model uses a single schematic level parameter "FET" to identify a set of model parameters for a particular technology, another model version has been implemented which gives access to all model parameters on the schematic level. This model can be given to third parties who can provide their own parameter sets. A screenshot of this version is also shown in Fig. 3.27. The latter version has been contributed to the TARGET NoE model software pool.

Both the nonlinear capacitance- and dispersion part can be disabled by setting the appropriate parameter to zero. Notably, the "DISPMODEL" parameter allows to disable the dispersion part entirely and attribute purely static (DISPMODEL=0) or dynamic (DISPMODEL>0) drain current characteristics to the non-dispersive current source I_{ds0}. It is then possible to evaluate the error introduced to circuit design by neglecting frequency dispersion. This is shown in chapter 4 in the comparison of measured and simulated characteristics of the developed MMIC applications. An in-depth investigation of frequency dispersion on circuit design has been carried out in [121]. Disabling the nonlinear capacitance model (CAPMODEL=0) will assume typical capacitance values for C_{gs} and C_{gd} from the saturated maximum gain voltage condition. The implementation then follows the standard charge-oriented approach. This setting speeds up simulator convergence and can be useful in the design of complex circuits at moderate operating frequencies, such as mixed-signal circuits or intermediate frequency components in receiver systems.

Schematic level parameters are listed and explained in table 3.3.

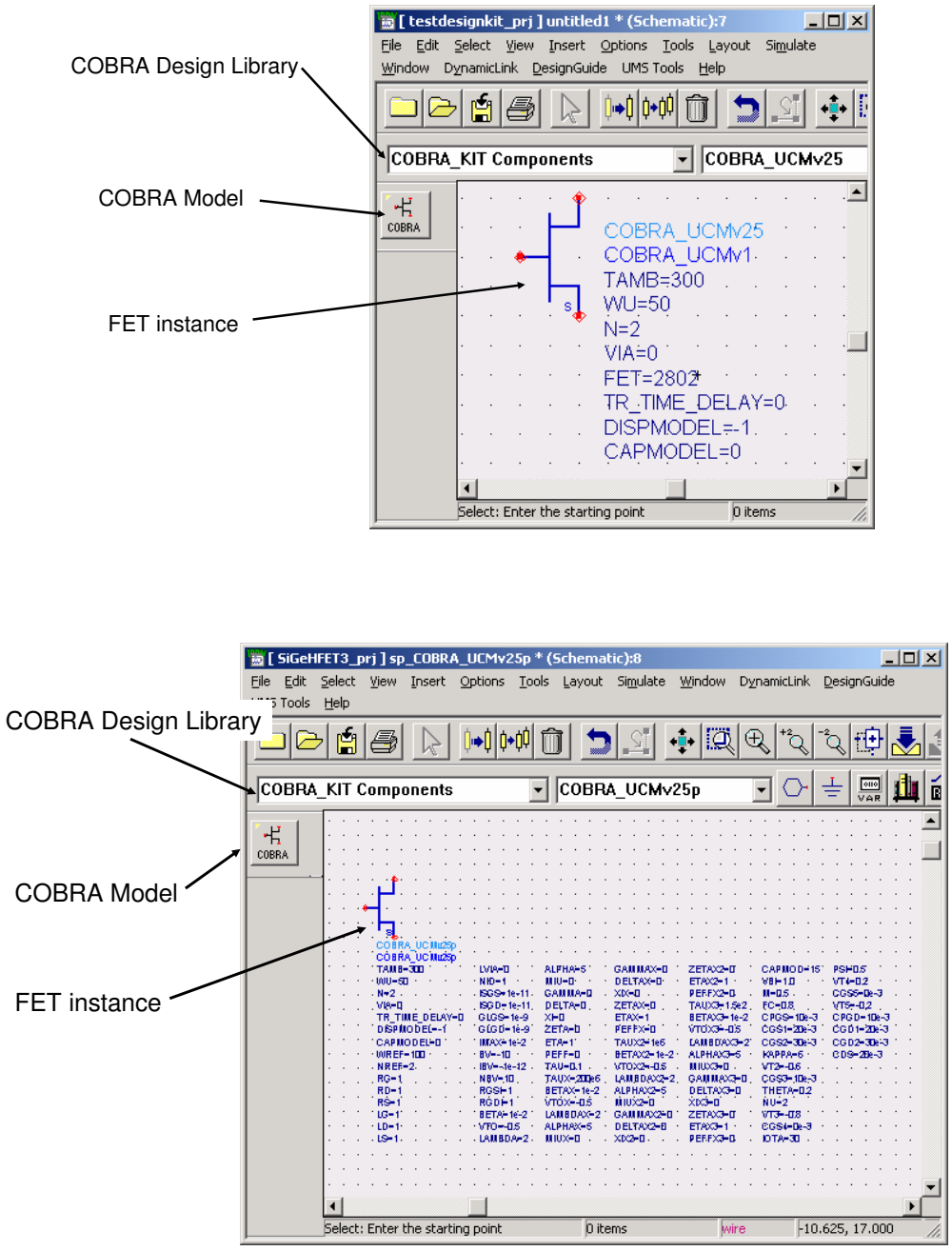

Figure 3.27: Top: the model is made available in ADS via a design kit, consisting of the COBRA design library and its FET model. The FET instance shows default schematic level parameters. A particular technology is identified by a single parameter "FET". A second version (below) gives access to all model parameters.

3.8 Small- and Large-Signal Model Verification

In the process of deducing and illustrating the model topology and its nonlinear equations, various verification data, i.e. a comparison of measured and modelled characteristics, has been presented up to now, such as

- Static gate current characteristics
- Static drain current transfer- and output IV characteristics
- Dynamic drain current characteristics obtained from pulsed-IV measurements
- S-parameter verification under bias conditions of high drain-source voltage to show the impact of dispersion effects with GHz time constants
- Turn-on transient drain current responses
- Nonlinear gate-source- and gate-drain capacitance[4].

Additional small- and large-signal verification can be carried out with the fully implemented model and the ADS simulation environment. Fig. 3.28 shows the S-parameter simulation of a $2\,\mathrm{x}\,30\,\mu$m GaAs pHEMT (PPH15), biased in the saturation-, knee- and linear operating region and within a frequency range of 50 MHz to 50 GHz. Excellent agreement between the linearised large-signal model and the measurement is reached under all operating conditions, proving the model's global validity and microwave frequency quality.

The large-signal quality is typically evaluated in one- and two-tone power measurements, where the power level of the sinusoidal input tone(s) is swept and the evolution of intermodulation frequencies is observed at the output. The one-tone measurement allows for the investigation of gain compression, i.e. the deviation from the linear relationship between in- and output power at the fundamental frequency, quantified by the 1dB compression point $P_{\mathrm{in,1dB}}$ (input-related). Also, higher order harmonics of the fundamental frequency start to occur at the output as a direct consequence of nonlinear operation. Here, the third-order intercept point $IP_{3,\mathrm{1tone}}$ [5] describes the interception of the linear extension of fundamental- and 3^{rd} order harmonic output power.

The two-tone measurements use two sinusoidal input tones f_1 and f_2 with small frequency spacing and of equal power level at the input, and evaluate the output power at the fundamental and in-band third-order intermodulation frequencies $2f_1 - f_2$ and $2f_2 - f_1$. The linear extension of both spectral components intersect at the third-order intercept point IP_3. In a diagram of logarithmic output power versus logarithmic input power, the linear part of first order spectral components have a slope of one, while third-order components rise with

[4] Strictly speaking, this is not a verification technique, since capacitance data is not obtained from direct measurement, but deduced from S-parameters.

[5] in the literature, this is sometimes also referred to as the third-order intercept point TOI.

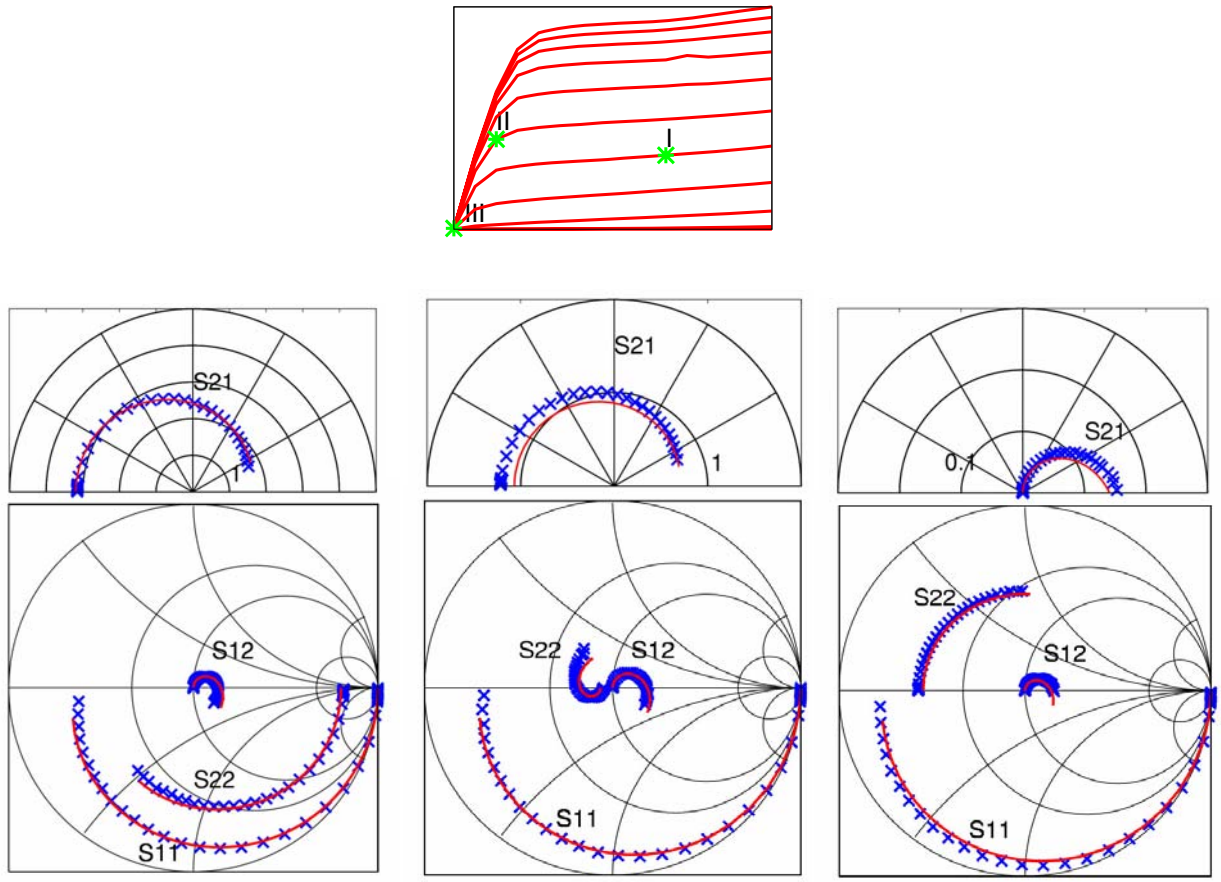

Figure 3.28: S-parameters (50 MHz-50 GHz) of a $2\,\mathrm{x}\,30\,\mu$m PPH15 GaAs pHEMT in three different bias points. Left: saturation region I. Middle: knee region II. Right: Linear region III. Measurement (symbols) and model (lines).

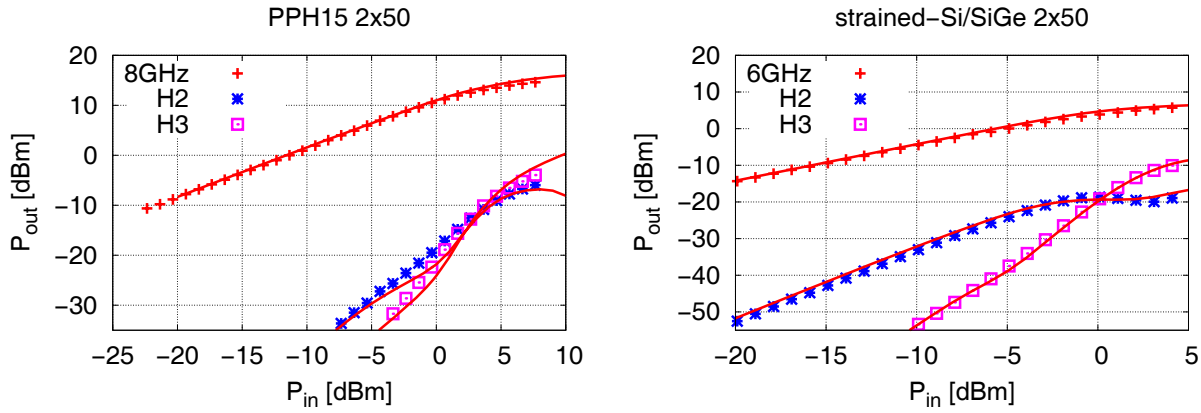

Figure 3.29: One-tone measurement. Measured and simulated gain compression and creation of harmonics H2 and H3 in a $2\,\mathrm{x}\,50\,\mu$m GaAs PPH15 device (left) and a $2\,\mathrm{x}\,50\,\mu$m strained-Si/SiGe device (right).

a slope of three. The input related (IIP_3) and output related (OIP_3) intercept points may therefore be calculated from

$$\mathrm{IIP}_3 = \frac{1}{2}\left(P_{\mathrm{out},1} - P_{\mathrm{out},3} + 2 \cdot P_{\mathrm{in}}\right) \tag{3.85}$$

$$\mathrm{OIP}_3 = \mathrm{IIP}_3 + \left(P_{\mathrm{out},1} - P_{\mathrm{in},1}\right) \tag{3.86}$$

where P_{in} is the input power level. $P_{\mathrm{out},1}$ and $P_{\mathrm{out},3}$ are the fundamental- and third order output power levels.

For all power measurements, the transistors are biased for maximum gain in their respective saturated region. As in the case of the S-parameter measurements, the devices are operated in common-source configuration and in a $50\,\Omega$ source- and load impedance environment.

Fig. 3.29 shows the measured and simulated one-tone results for a $2\,\mathrm{x}\,50\,\mu$m GaAs PPH15 device and a $2\,\mathrm{x}\,50\,\mu$m SiGe device at the fundamental frequency of 6 GHz. Table 3.4 lists input and output related gain compression- as well as third-order intercept points for all four HEMT types.

Two-tone measurements and their respective simulations are shown in Fig. 3.30 for a $2\,\mathrm{x}\,50\,\mu$m GaAs PH15 transistor as well as a $2\,\mathrm{x}\,40\,\mu$m InP device. The comparison of measured and modelled extrapolated two-tone IP_3's of all technologies are listed in table 3.5. Both gain compression and the evolution of higher order harmonics and intermodulation products are accurately predicted by the model for all transistor types, highlighting its universal applicability and high quality in the nonlinear microwave regime [122, 123].

The complete verification data of all modelled devices is listed in Appendix C. Ultimate model verification as well as demonstration of its suitability to being employed in complex circuit topologies are carried out in the comparison of simulation and measurement of full MMIC characteristics, discussed in the following chapter.

Device	Fund	$P_{\mathrm{in,1dB}}$/dBm		$P_{\mathrm{out,1dB}}$/dBm		$\mathrm{IIP}_{3,1tone}$/dBm		$\mathrm{OIP}_{3,1tone}$/dBm	
		meas	simu	meas	simu	meas	simu	meas	simu
2 x 40 μm InP	8 GHz	-6.5	-5.1	5.7	7.0	10.5	9.8	23.5	22.8
2 x 50 μm GaAs PH15	8 GHz	-1.3	-1.2	10.8	11.6	13.9	14.3	27.0	27.8
2 x 50 μm GaAs PPH15	8 GHz	1.4	1.5	13.1	12.2	17.4	17.4	29.7	28.6
2 x 50 μm strained-Si/SiGe	6 GHz	-2.2	-0.3	2.4	4.5	14.6	14.7	20.0	20.5

Table 3.4: One-tone measurement. Measured and simulated compression points and third-order intercept points (input- and output related) for all four HEMT types.

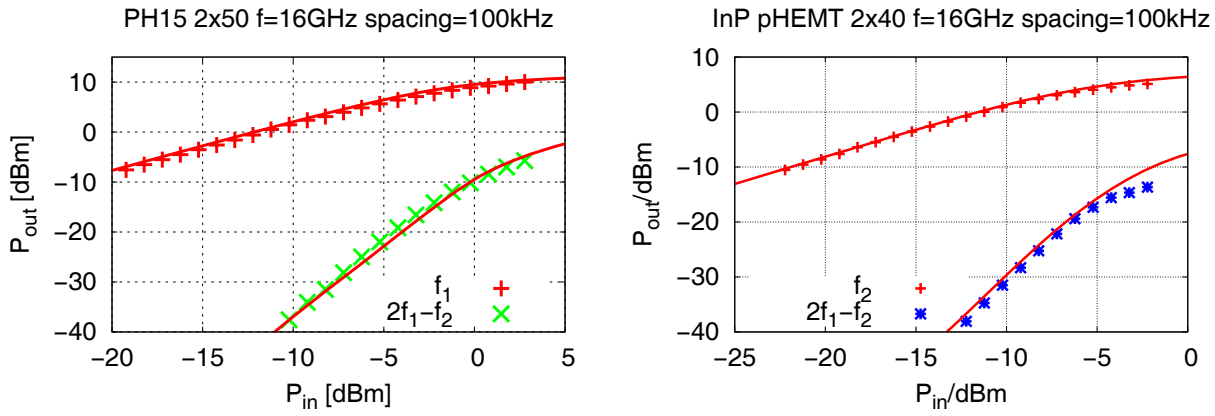

Figure 3.30: Two-tone measurement at 16 GHz fundamental frequency and 100 kHz tone spacing. Measured and simulated third-order intermodulation products in a 2 x 50 μm GaAs PH15 device (left) and a 2 x 40 μm InP device (right).

Device	Fund	IIP_3/dBm		OIP_3/dBm	
		meas	simu	meas	simu
2 x 40 μm InP	16 GHz	6.6	6.1	17.8	17.9
2 x 50 μm GaAs PH15	16 GHz	9.3	9.5	21.0	21.5
2 x 50 μm GaAs PPH15	20 GHz	13.3	13.7	20.9	20.4
2 x 50 μm strained-Si/SiGe	16 GHz	6.9	7.9	13.2	13.5

Table 3.5: Two-tone measurement. Measured and simulated third-order intercept points (input and output related) of all four HEMT technologies.

Chapter 4

MMIC Applications

This chapter presents the MMIC applications which were designed and realised based on the model introduced in the previous chapters.

For the SiGe mHEMTs, the developed model has for the first time allowed to design and realise integrated circuits with this new technology. Here, two travelling-wave amplifiers, one using common-source active stages, the other employing cascode stages, will be described. Additionally, the model has been used in the design and realisation of a single-balanced mixer MMIC [124] as well as basic logic gate blocks [125].

In case of the UMS GaAs pHEMT technologies, the model with its accuracy under all operating conditions merges several foundry design kit models in one (see chapter 1.2) and improves them by adding the frequency dispersion part and nonlinear capacitance as discussed in chapter 1.2. A travelling-wave MMIC, using an innovative circuit concept which offers operation both as mixer and variable gain amplifier, has been developed in PPH15 technology.

Each circuit is first discussed in terms of the applied circuit topology and its physical layout. Then, measured small- and large-signal performance is compared to the simulation results. Where possible, a special focus is applied to the model's capability of including the impact of frequency dispersion effects [126]. It should be noted that in all cases circuits are measured and simulated under identical bias conditions.

As final results in a development chain ranging from device characterisation and modelling to the design of circuit applications, the fabricated MMICs allow for verification of the custom FET model, whose declared purpose is the efficient and accurate microwave circuit design.

4.1 SiGe mHEMT Travelling-Wave Amplifiers

The first Si/SiGe mHEMT MMICs have successfully been fabricated in a cooperation between University of Ulm, DaimlerChrysler Research and the HMOS consortium in the United Kingdom [127, 128, 39]. The travelling-wave amplifiers were included on a multi project wafer (MPW) using the 0.1 μm gate length technology introduced in chapter 1.1.

In addition to the development of the CAD model for active devices, particular challenges

needed to be addressed. For the realisation of MMIC applications, the existing process had to be extended to accommodate a two-metal layer topology. Primarily, this allows for the realisation of MIM type integrated capacitors and the required cross-overs in the transmission lines carried out as coplanar waveguides (CPW). Details are included in Appendix D. The additional modelling effort towards the full MMIC design is discussed next.

4.1.1 Transmission Line- and Active Device Models

The characteristic elements of travelling-wave circuits are inductive transmission lines, which compensate for the capacitive load presented by the in- and output impedances of active stages. Travelling-wave amplifiers combine the phase-match condition for constructive wave interference of a sequence of amplifying stages with the power match condition at all terminals. Hence, an accurate line model is required during the design phase. Based on test structures, a CPW line model was extracted [129]. Within the measured frequency range of up to 50 GHz, very good simulation accuracy was achieved by using the built-in CPW line model of ADS and defining and extracting the parameters of a substrate model. The substrate uses multiple dielectric layers to reflect the graded buffer layer of the technology's actual layer stack.

Special care was taken in the modelling of underpaths. Due to the thin dielectric layer between the signal line on metal 2 and the underpath on metal 1, they introduce high capacitive coupling and therefore losses to wave propagation. To minimise this effect, the signal line was tapered when crossing an underpath. This measure, however, produces a discontinuity to the line's characteristic impedance, and hence to wave propagation. The model used to account for the effects of underpaths is shown in Fig. 4.1 (left). The series inductance is responsible for the discontinuity in characteristic impedance, while a series RC combination reflects capacitive coupling. Model parameters were again extracted from test structures and found to be $L = 2.25\,\mathrm{pH}$, $C = 9.4\,\mathrm{fF}$ and $R = 1.5\,\Omega$ for the CPWs used in the circuit's gate- and drainlines. Fig. 4.1 shows a microphotograph of a T-junction in a coplanar transmission line. It illustrates the use of underpaths with signal line tapering to reduce capacitive coupling. The round shapes along the signal line are ties (oxide openings) between metal 1 and metal 2.

When measuring S-parameters of single transistors on the wafers containing the MMIC circuits, a peculiar frequency dependence was observed in the lower GHz range, predominantly in the parameters related to forward transmission (S_{21}) and input reflection ($S_{11} \approx \Gamma_1$). The magnitude of S_{11} increases slightly beyond one, indicating a positive feedback effect. Also, below about 8 GHz, the magnitude of S_{21} deviates significantly from the expected values. It decreases and settles at a much reduced value at low frequencies (compare Fig. 4.2). Both effects can be explained by the formation of oxide patches covering parts of the source- and drain implantation regions, a parasitic effect occurring during the manufacturing process of the ohmic contacts [130].

The model used to account for this additional capacitance between the implanted contact

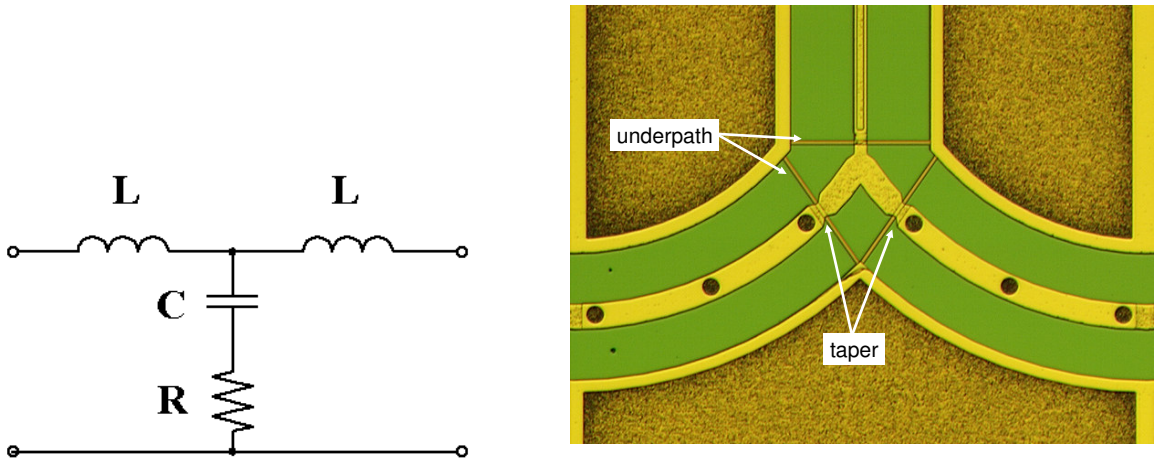

Figure 4.1: Left: Equivalent circuit employed to model the effect of underpaths in CPW lines. Right: Coplanar transmission lines include underpaths and line tapering at cross-overs.

areas and metal 1 consists of a parallel RC network in series to all drain and source terminals of the FETs (Fig. 4.2). Resistor R_{MI} describes the increase in contact resistance at low frequencies before being short-circuited by the oxide patch capacitance C_{MI}. Extracted values are $R_{\mathrm{MI}} = 22\,\Omega$ and $C_{\mathrm{MI}} = 3\,\mathrm{pF}$. A linear scaling model is assumed for both elements. With this modification, the measured S-parameters could accurately be reflected by the FET model (Fig. 4.2), notably the effect on S_{21} and S_{11} as depicted in more detail in Fig. 4.3.

The deviation in the magnitude of S_{21} is due to the intrinsic transistor model having been extracted from measurements on a different wafer. The strained-Si/SiGe mHEMT technology, although having reached a state of impressive maturity, still suffers from significant wafer-to-wafer and cross-wafer variations of device performance. Under typical saturation bias conditions, the model predicts too much gain. This is also observed in the gain measurements of the travelling-wave amplifiers (chapters 4.1.2 and 4.1.3).

A similar frequency dependence was observed in transmission measurements of an integrated resistor which uses the drain/source implantation layer as contacts. It showed the intended resistance at high frequencies, but significantly increased DC resistance due to the additional low frequency contact resistance. The same modification to the ideal resistor model is capable of describing the effect.

4.1.2 Common-Source Stage Distributed Amplifier

The well-known travelling-wave amplifier (TWA) or distributed amplifier (DA) concept achieves bandwidth enhancement by using inductive transmission lines to absorb the in- and output capacitance of active devices. Signal waves travel along the resulting loaded (or "artificial") transmission lines, with the gain of cascaded amplifying stages ideally adding up. The TWA principle is shown in Fig. 4.4. Forward travelling waves on the input gate line as

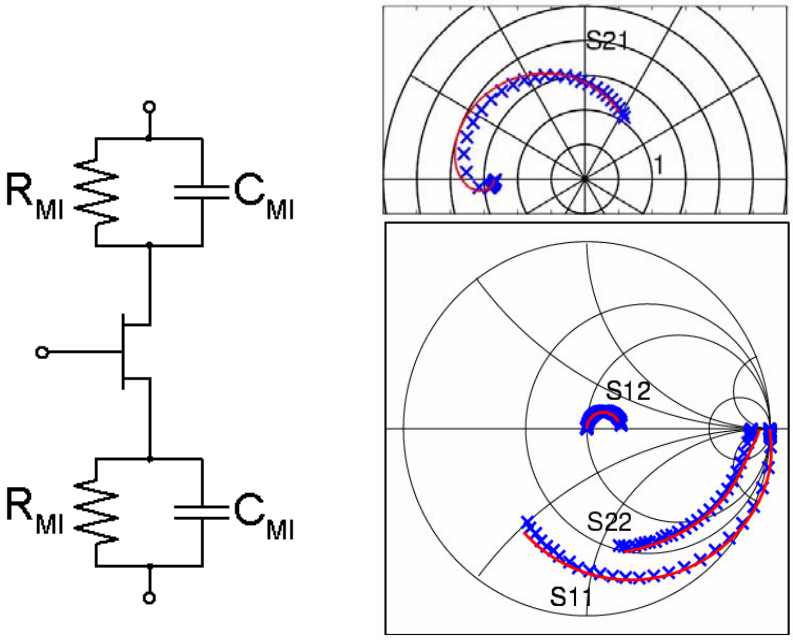

Figure 4.2: Left: Modified FET model, accounting for the effect of parasitic oxide patches on the drain- and source contacts. Right: Measured (symbols) and modelled (lines) S-parameters between 50 MHz and 50 GHz of a 2x50 μm single device in saturated operation with maximum gain.

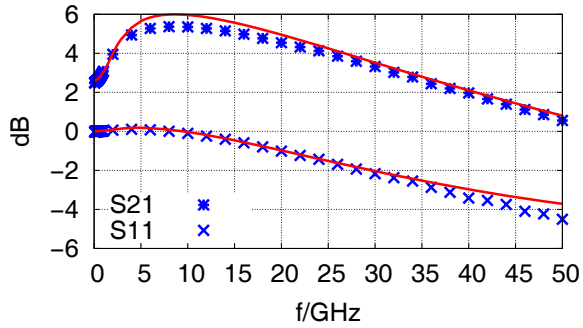

Figure 4.3: Effect of oxide patches at the drain- and source contacts on the magnitude of forward transmission (S_{21}) and input reflection (S_{11}) .

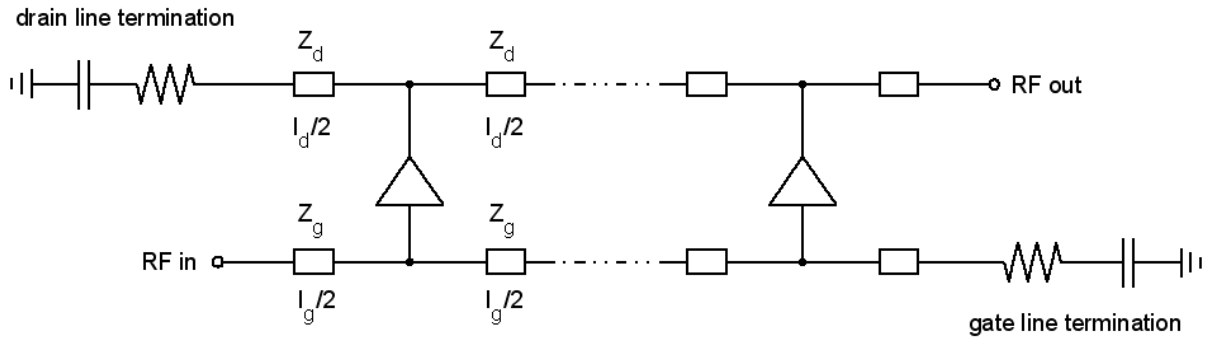

Figure 4.4: Travelling-wave amplifier principle.

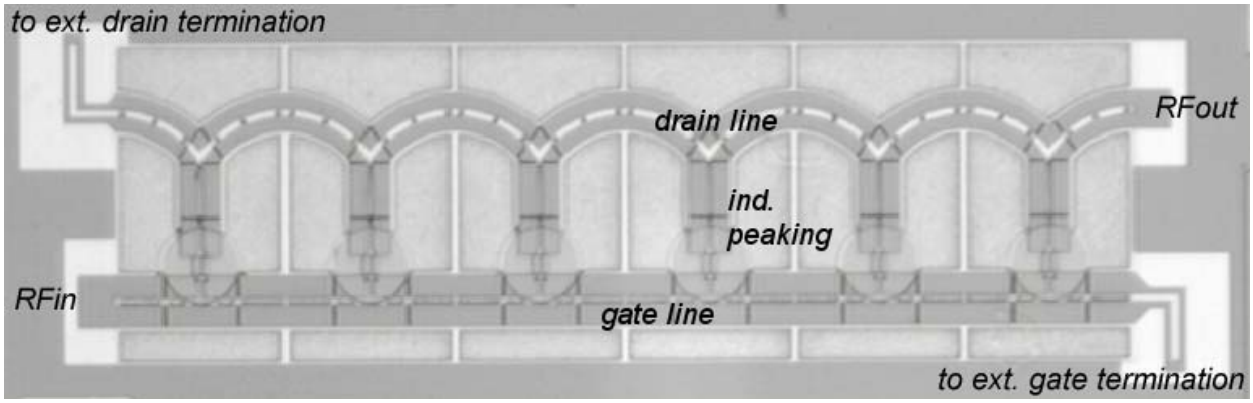

Figure 4.5: Microphotograph of a 6-stage common-source TWA in Si/SiGe mHEMT technology. Chip dimensions are $3.2 \times 1.0\,\mathrm{mm}^2$

well as reverse travelling waves on the output drain line are terminated into $50\,\Omega$ to avoid reflections. The two design conditions to be met for TWA operation are [131]:

- Constructive wave interference on the drain line (phase-match condition):

$$\beta_1 l_\mathrm{g} = \beta_2 l_\mathrm{d} \tag{4.1}$$

- In- and output power match:

$$Z_1 = Z_2 = Z_0 = 50\,\Omega \tag{4.2}$$

where β_1/β_2 and Z_1/Z_2 are the propagation constant and characteristic impedance of the loaded gate/drain transmission line, respectively.

Fig. 4.5 shows the layout of a 6-stage TWA, realised for the first time in strained-Si/SiGe mHEMT technology. Its individual amplifying stages consist of $2\,\mathrm{x}\,50\,\mu$m wide, π-gate transistors connected in common-source configuration. The power- and phase match conditions dictate the dimensioning of the CPW lines, resulting in $l_\mathrm{g} = 450\,\mu$m, $l_\mathrm{d} = 530\,\mu$m and a

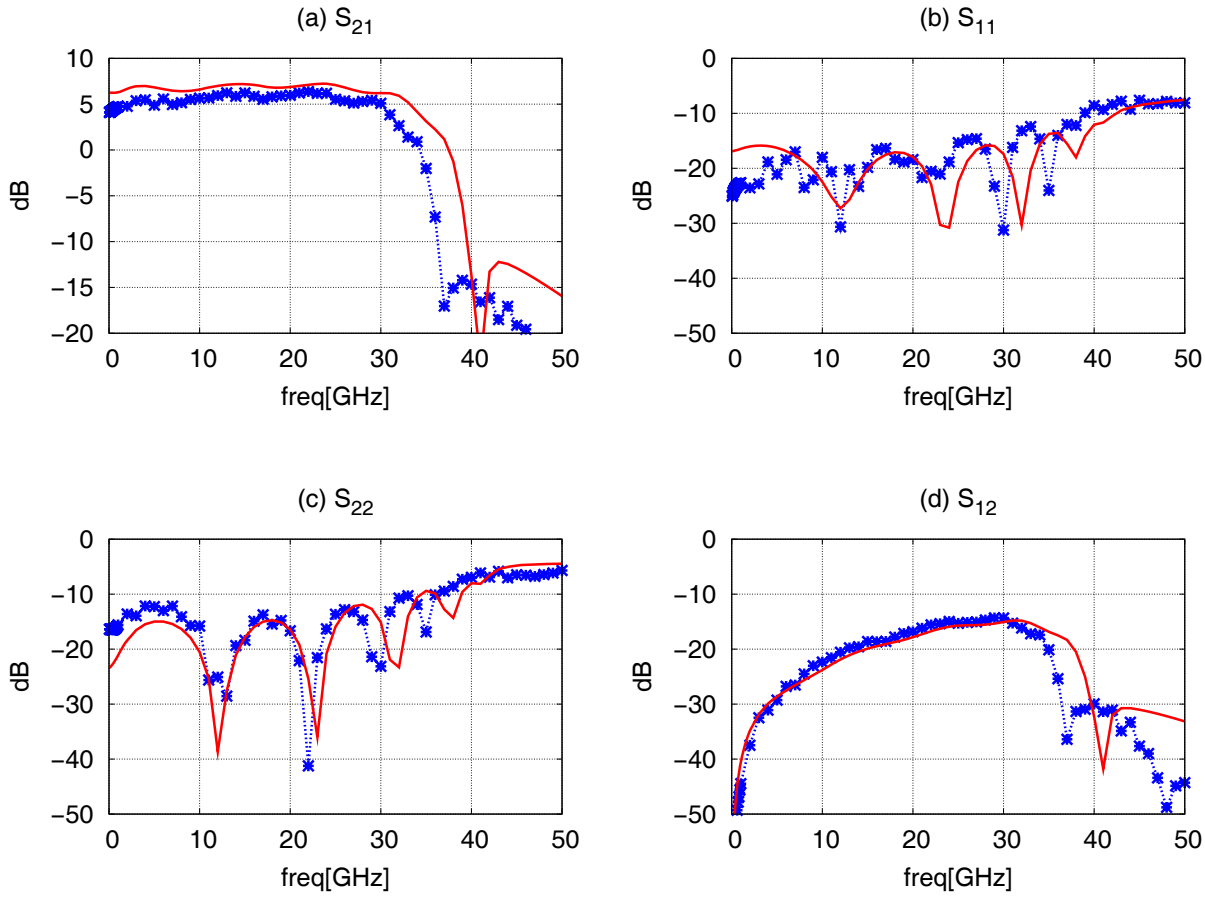

Figure 4.6: Comparison of measured (points) and modelled (solid lines) S-parameters of the 6-stage SiGe mHEMT common-source TWA.

line spacing of $s_g = 60\,\mu$m and $s_d = 40\,\mu$m for the gate and drain lines, respectively. An inductive peaking effect is included in the amplifying stages by an additional line element in series to the FET drain terminals.

The MMIC is measured on-wafer with external gate- and drain terminations. Bias conditions are $V_{G1} = -0.1\,$V and $V_{DD} = 2\,$V for maximum gain. Fig. 4.6(a)-(d) shows the comparison of measured and modelled S-parameters for the SiGe TWA. The amplifier achieves a measured gain of 5.6 dB with a gain ripple of 0.8 dB within a bandwidth of 2...32 GHz. Towards lower frequencies, the gain drops slightly due to the effect of the parasitic oxide patches as discussed above. Input and output matching is better than 13 dB and 10 dB, respectively, within the amplifier bandwidth. Reverse isolation degrades to 14 dB at the upper cutoff frequency.

Good agreement between measurement and model is met for all parameters, with the model overestimating the gain by 1.2 dB and the bandwidth by 2 GHz. The reason for this deviation lies in the experimental technology's well known wafer-to-wafer and cross-wafer variation, and the fact that the transistor model was extracted from devices on a different wafer than the MMICs. All simulations, including small-signal analysis, are carried out with

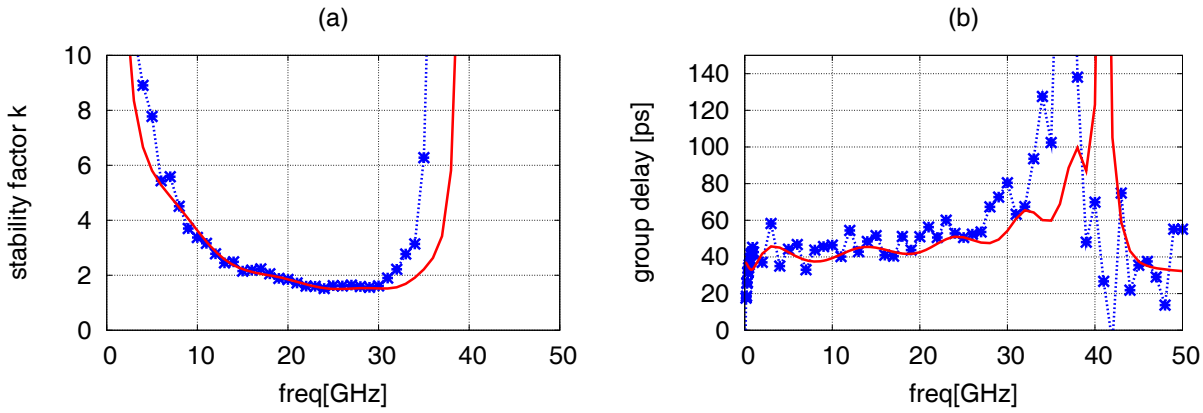

Figure 4.7: Comparison of measurement (points) and simulation (solid lines) of stability factor k (a) and group delay (b) in the SiGe mHEMT common-source TWA.

the full nonlinear model introduced in the previous chapters. Detailed model parameters are listed in Appendix C.1.

Two crucial parameters in the design of TWAs are

- the stability factor k as main indicator to amplifier stability, with stability being the major problem in practical TWA design, notably when employing potentially unstable amplifying stages like cascodes.
- the group delay (τ_{gr}) ripple, indicating the amplifier's capability of transmitting arbitrary waveforms without signal distortion. For instance, this constitutes the crucial performance parameter in optical transmission systems, where distortion of transmitted pulses degrades the eye diagram opening and hence increases the bit error rate.

Both parameters are deduced from S-parameters and shown in Fig. 4.7. Again, excellent agreement with simulation is met, with measured group delay being $56.5 \pm 23.5\,\mathrm{ps}$ within the 2...32 GHz bandwidth. The correct analysis of group delay in particular demonstrates the model's suitability in the microwave regime. Group delay is defined as the negative derivative of the phase of the complex transfer function with respect to frequency:

$$\tau_{\mathrm{gr}} = -\frac{1}{360^\circ}\frac{\partial\phi}{\partial f} \tag{4.3}$$

Group delay is therefore governed predominantly by the reactive, i.e. capacitive model elements.

The circuit consumes a DC power of 94 mW ($I_{\mathrm{DD}} = 47\,\mathrm{mA}$ at $V_{\mathrm{DD}} = 2\,\mathrm{V}$). Simulation predicted 37 mA, i.e. 74 mW. A stringent interpretation of static analysis is hindered by the strong wafer-to-wafer variation as well as the stochastic component in the formation of the parasitic oxide patches (see chapter 4.1.1), which introduces a variation to internal transistor voltages due to the static voltage drops across R_{MI}.

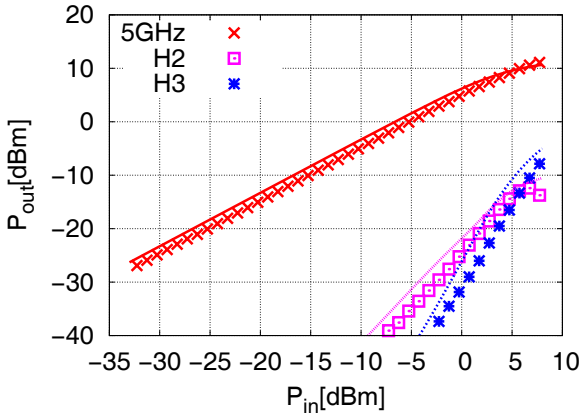

Figure 4.8: one-tone measurement and simulation at 5 GHz fundamental frequency.

Parameter	Unit	measured	modelled
Gain (S_{21})	dB	5.6 ± 0.8	6.8 ± 0.4
Bandwidth	GHz	2-32	2-34
Input match (S_{11})	dB	<-13.1	<-14.5
Output match (S_{22})	dB	<-10.7	<-9.7
Reverse isolation (S_{12})	dB	<-14.3	<-15.3
Group delay	ps	56.5 ± 23.5	51.0 ± 13.0
Stability factor	1	>1.5	>1.5
$P_{\text{in,1dB}}$	dBm	4.7	2.5
$P_{\text{out,1dB}}$	dBm	9.1	8.1
P_{DC}	mW	94	74

Table 4.1: Summary of measured and modelled performance of the SiGe mHEMT common-source TWA.

In order to evaluate the large-signal accuracy of the model, one-tone power measurements were performed on the circuit. Fig. 4.8 shows gain compression and creation of harmonics for a fundamental frequency of 5 GHz, with all power levels being referenced to the MMIC in- and output planes. The measurement reveals an output power of 9.1 dBm in 1 dB compression, with the simulation predicting 8.1 dBm. While the model is too conservative in terms of gain compression, its level of accuracy in predicting harmonics in the output spectrum is adequate.

Table 4.1 summarises measured and modelled performance of the SiGe mHEMT common-source TWA, demonstrating the model's very satisfactory degree of accuracy, in small-signal- as well as static and dynamic large-signal analysis.

4.1.3 Cascode Stage Distributed Amplifier

In another version of the SiGe TWA, the amplifying cells are replaced by cascodes. Fig. 4.9 shows the corresponding layout of the full 6-stage TWA as well as a detailed photograph of a single stage. The common-gate transistor in the cascode stage requires an additional gate bias. At the same time, the gate of the upper transistor is HF-grounded via sections of MIM stacks between neighbouring stages, acting as plate capacitors. Bias conditions for maximum gain here are $V_{G1} = -0.1\,\mathrm{V}$, $V_{DD} = 3.4\,\mathrm{V}$ and $V_{G2} = 1.8\,\mathrm{V}$, where V_{G1} and V_{G2} are the gate voltages for the common source- and common-gate transistors, respectively.

By using cascode amplifying stages, one anticipates the following qualitative effects on TWA performance:

- An increased reverse isolation, due to the disruption of the feedback path by the grounded gate of the common-gate transistor in cascodes.
- The significant decrease in output conductance of cascodes compared to common-source stages will lead to an increase in gain in TWAs. This is due to less attenuation on the drain line.
- Both the decreased output admittance and increased gain lead to potential instability of the cascode cell. In particular, with the cascode's real part of output admittance potentially becoming negative at high frequencies [132], instability typically occurs close to the upper cutoff frequency in TWAs.

The comparison of measured and modelled S-parameters is shown in Fig. 4.10. This amplifier achieves a measured gain of $4.4 \pm 0.5\,\mathrm{dB}$ within a bandwidth of 2...40.5 GHz, while the simulation predicts a gain of $7.3 \pm 0.5\,\mathrm{dB}$ within 2...40.5 GHz. While bandwidth is correct, above about 1 GHz the measured gain is lower than predicted. This correlates to the reverse isolation, which is found to deviate significantly from simulation at frequencies between approx. 1 GHz to 20 GHz. A possible coupling mechanism, not included in the simulation, which reduces both gain and reverse isolation, lies in the non-ideal ground plane of the MMIC. The ground plane of the circuit is situated on the thin metal 1 layer and is externally connected via the coplanar GSG probes. A fraction of the signal power will therefore be present on this non-ideal ground node and will couple on the upper transistor gate via the very big MIM capacitance between stages. A redesign measure for improved circuit performance therefore should consist in the reduction of the MIM capacitance grounding the cascode gate, as well as the improvement of the ground plane by including more metal 2 area on the ground node. Power matching is accurately predicted, with the simulation of S_{11} being too conservative.

It is interesting to note that the cascode version shows critical stability behaviour (as anticipated) at the upper cutoff frequency, manifested by a large ripple in gain and a degradation of output matching. The model actually predicts possible instability (k $<$ 1 and

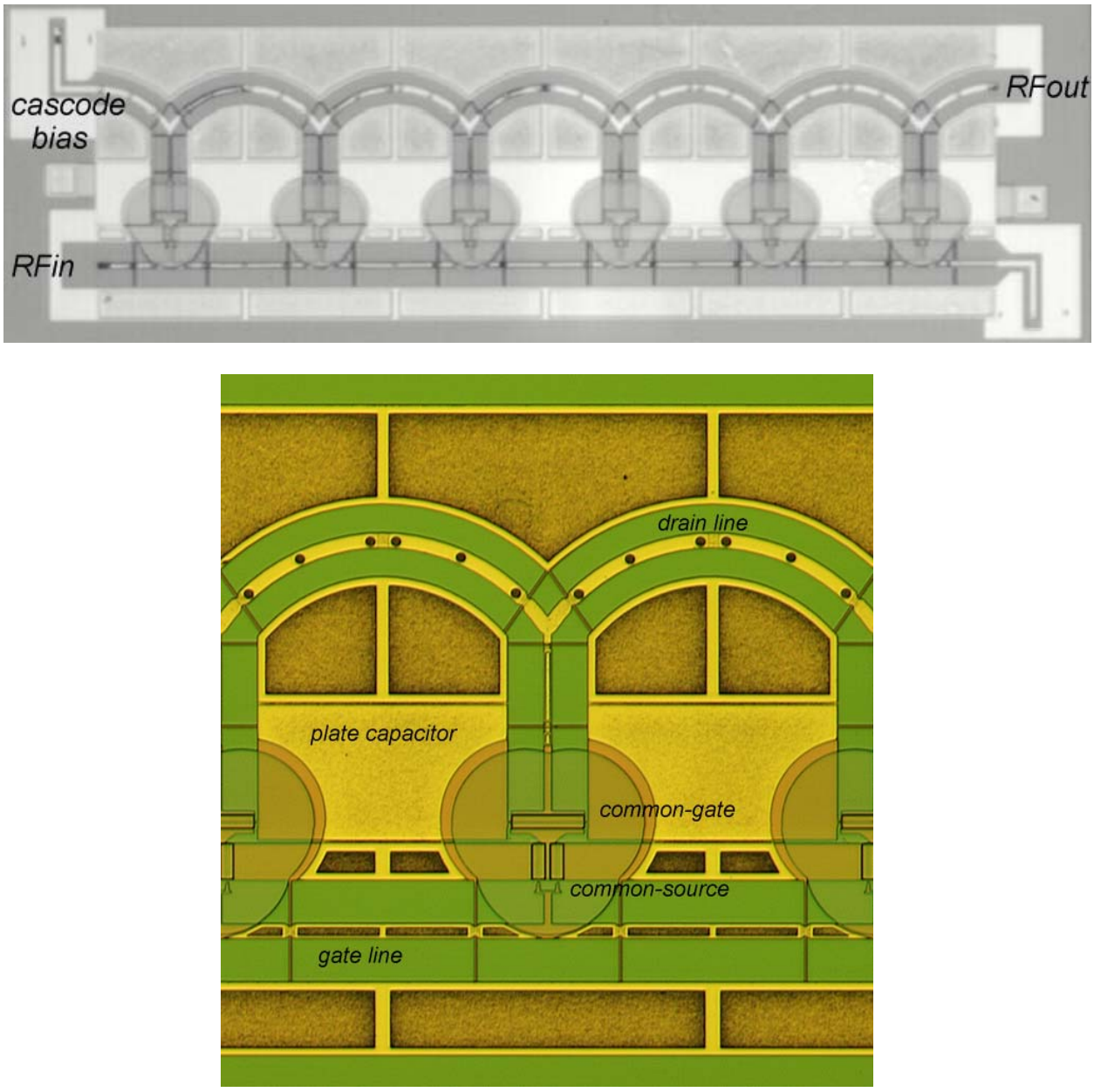

Figure 4.9: Microphotographs of the SiGe mHEMT cascode TWA. Top: full 6-stage TWA with chip dimensions of $3.2 \times 0.9\,\mathrm{mm}^2$. Bottom: single stage detail.

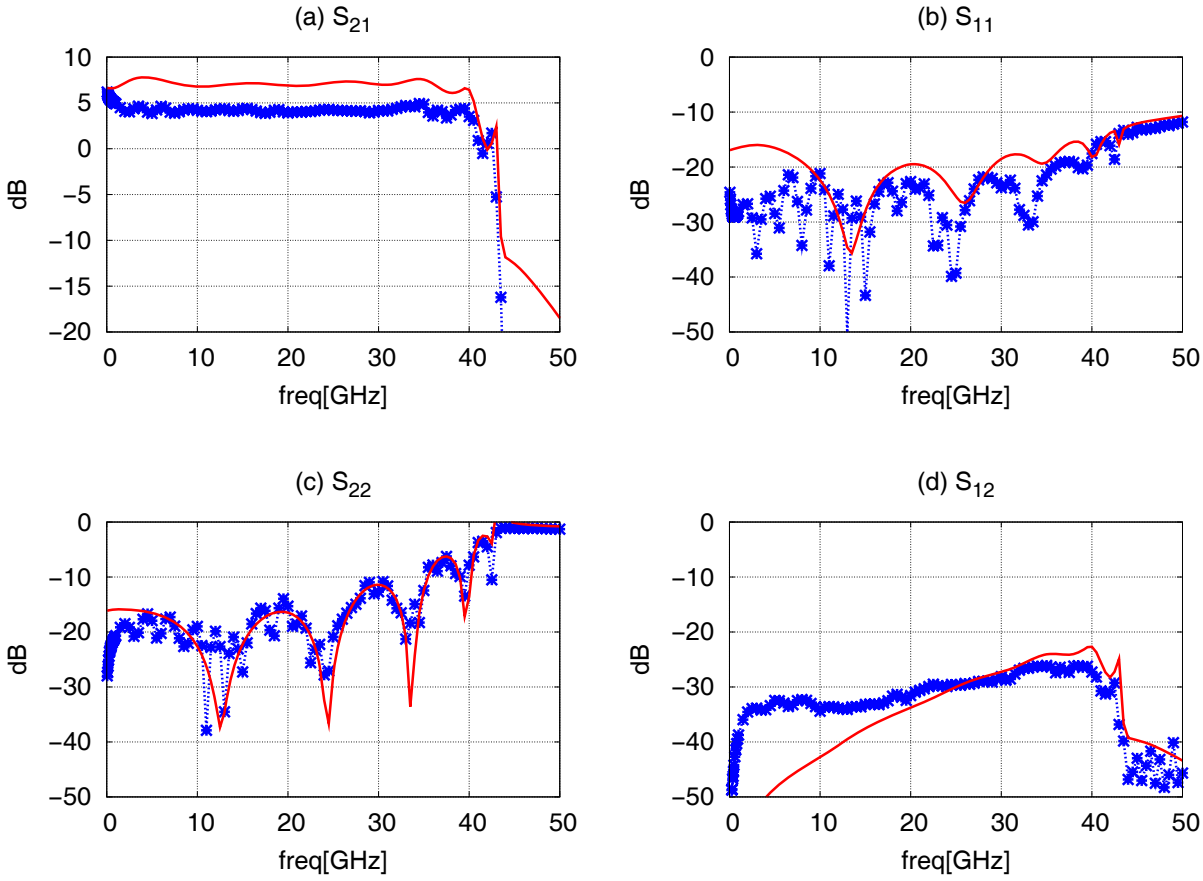

Figure 4.10: Comparison of measured (points) and modelled (solid lines) S-parameters of the 6-stage SiGe mHEMT cascode TWA.

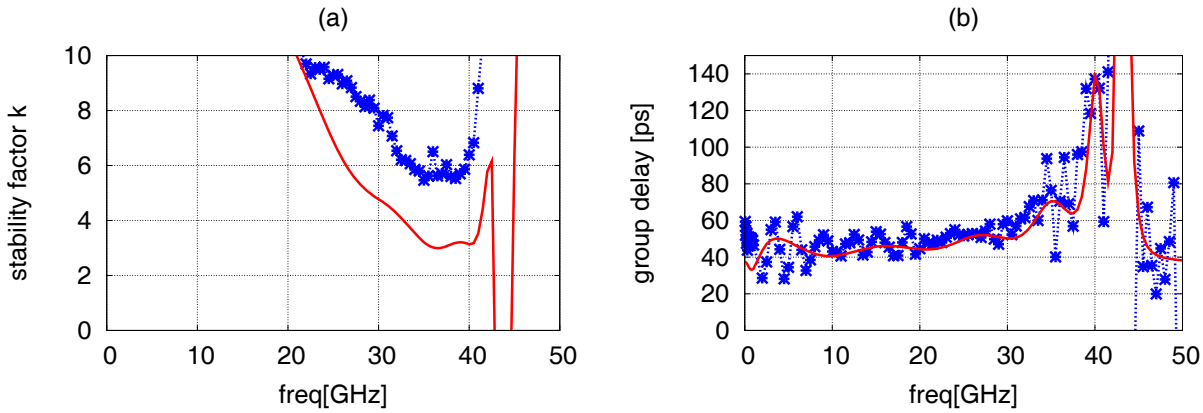

Figure 4.11: Comparison of measurement (points) and simulation (solid lines) of stability factor k (a) and group delay (b) in the SiGe mHEMT cascode TWA.

$|S_{22}| > 1$). Fig. 4.11 shows the comparison of simulated and measured stability factor and group delay for this cascode version.

4.2 GaAs pHEMT Travelling-Wave Mixer and Variable Gain Amplifier

In the following, a new distributed circuit concept, offering multi-decade mixing and variable gain amplification in a single MMIC is introduced [133]. Typical applications for such an ultra-broadband mixer include Electronic Surveillance Measures (ESM) and microwave instrumentation. In addition to its dual functionality, the circuit concept features an inherently high linearity performance under mixer operation, surpassing all other distributed mixer concepts to-date.

The MMIC was fabricated in the power variant of the $0.15\,\mu m$ GaAs pHEMT technology (PPH15, see chapter 1.2), in the frame of a MPW run of the UMS foundry.

4.2.1 Unit Cell Topology and Operation Principle

The travelling-wave concept is applied here to a current-voltage feedback circuit, as a variant of FET mixer topologies (e.g. [134]). The unit cell of the mixer is shown in Fig. 4.12. It consists of a cascode amplifying stage (T_1 and T_2), which undergoes variable feedback from a source transistor T_3 biased in its linear operating region. For that purpose, T_3 is scaled to twice the size of the cascode transistors. Its output conductance and with it the feedback effect can be controlled by a variation of the gate potential. On one hand, this results in amplifier gain being dependent on the controlling gate bias and therefore allows for VGA operation. More importantly however, by applying an LO drive signal to the feedback transistor gate, the RF input signal is multiplied with a gain which varies with the LO frequency and therefore generates the intermediate frequency (IF) mixing component at the output.

Other published distributed mixer concepts (Fig. 4.13) use a transconductance topology [135, 136], a dual-gate configuration [137, 138] or a drain configuration [139]. All of them inherently must suffer from poor linearity performance, since in all cases transistors are operating in a non class A condition, resulting in an early onset of gain compression .

The transconductance- or g_m-mixer uses a combiner to apply both the RF- and LO signals to the FET's gate terminal [140]. The transistor needs to be biased in a close-to-threshold condition to avoid excessive LO drive power requirements. The drain mixer uses the LO power to switch the transistor between linear- and saturated operating regimes, thereby modulating both g_m and g_{ds} to obtain the frequency translation effect. The same effect is used in the dual-gate approach, where the LO signal drives the gate of an upper transistor in a pseudo-cascode configuration to switch the lower transistor between the two operating regions. In both cases, the IF-generating device is biased in the knee region to minimise LO

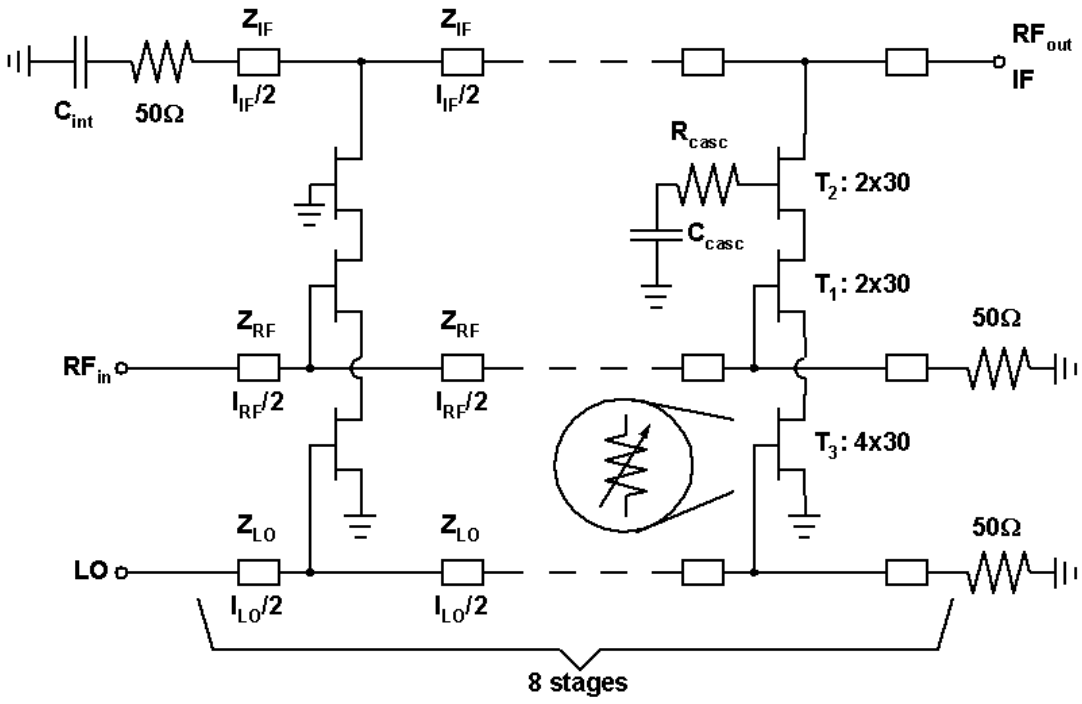

Figure 4.12: Unit cell topology of the distributed mixer/VGA. Cascode amplifying stages with resistive source feedback are embedded into artificial transmission lines.

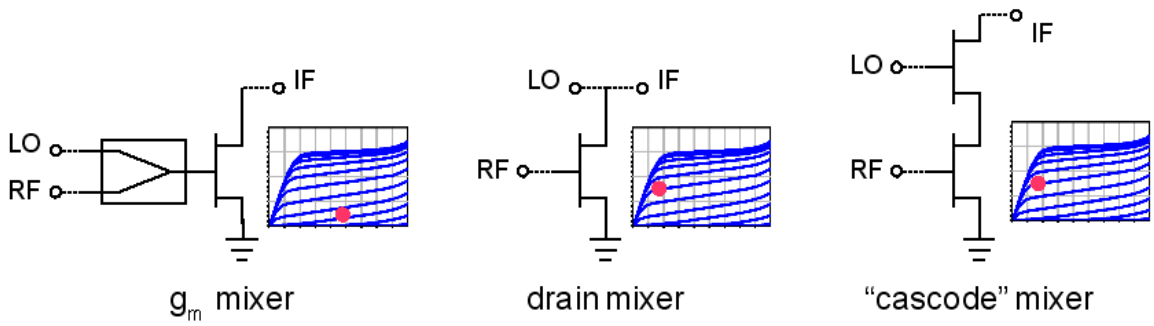

Figure 4.13: Other published distributed mixing concepts use active devices operating under non-ideal linearity conditions.

power.

The proposed current-voltage feedback topology uses an amplifying stage biased for class A operation, and therefore provides inherently high linearity. A comparison of measured performance of all mixer concepts is drawn in chapter 4.2.4.

4.2.2 Circuit Design and Layout

In order to obtain the bandwidth enhancing effect of the travelling-wave principle, the capacitive impedance of all three ports of the unit cell is compensated by inductive microstrip transmission lines, forming artificial phase- and power matched lines [131]. Forward travelling waves on the input lines (RF and LO) and the reverse travelling wave on the output line (IF) are terminated by an on-chip 50 Ω impedance. On the drain line, this requires a DC blocking on-chip capacitor C_{int} which introduces a lower cutoff frequency, here at approximately 2 GHz.

Constructive wave interference at the IF frequency mandates ([135])

$$\beta_{\mathrm{RF}} \cdot l_{\mathrm{RF}} - \beta_{\mathrm{LO}} \cdot l_{\mathrm{LO}} = \beta_{\mathrm{IF}} \cdot l_{\mathrm{IF}} \tag{4.4}$$

where

$$\beta_{\mathrm{RF}} = \omega_{\mathrm{RF}} \sqrt{L'_{\mathrm{RF}} \left(C'_{\mathrm{RF}} + \frac{C_{\mathrm{in,Casc}}}{l_{\mathrm{RF}}} \right)} \tag{4.5}$$

is the propagation constant of the RF gate line, loaded with the input impedance of the cascode stages and neglecting losses due to the series gate resistance of the transistor. l_{RF} is the length of a transmission line segment on the RF gate line. Indices "LO" and "IF" refer to the LO gate- and IF drain lines, respectively. For non-dispersive lines, equation (4.4) reduces to the well-known phase match condition for distributed amplifier operation. Neglecting the low dispersion on microstrip lines, a travelling-wave mixer may therefore be employed as amplifier without requiring a change in transmission line dimensioning.

In addition to being phase matched, the transmission line of the LO signal has to be power matched:

$$Z^*_{\mathrm{LO}} = \sqrt{\frac{L'_{\mathrm{LO}}}{C'_{\mathrm{LO}} + \frac{C_{\mathrm{in,T3}}}{l_{\mathrm{LO}}}}} = Z_0 = 50\,\Omega \tag{4.6}$$

As the lower transistors, connected to the LO line, are scaled to twice the size of the cascode transistors, the LO gate line is more inductive with a characteristic impedance of $Z_{\mathrm{LO}} = 82\,\Omega$, while the RF- and IF lines result in $Z_{\mathrm{RF}} = 76\,\Omega$ and $Z_{\mathrm{IF}} = 65\,\Omega$, due to their respective capacitive loading with the cascode stages' in- and output impedances.

Fig. 4.14 shows the layout of the designed and realised MMIC. The very compact layout uses a shared-via arrangement of individual stages, i.e. the feedback- and common-gate cascode transistors of neighbouring stages share the same via holes. Special care has been taken in circuit design to guarantee stability considering parasitic via hole inductance. This is revealed in the unit cell detail in Fig. 4.14 by the small resistors placed in series to the via

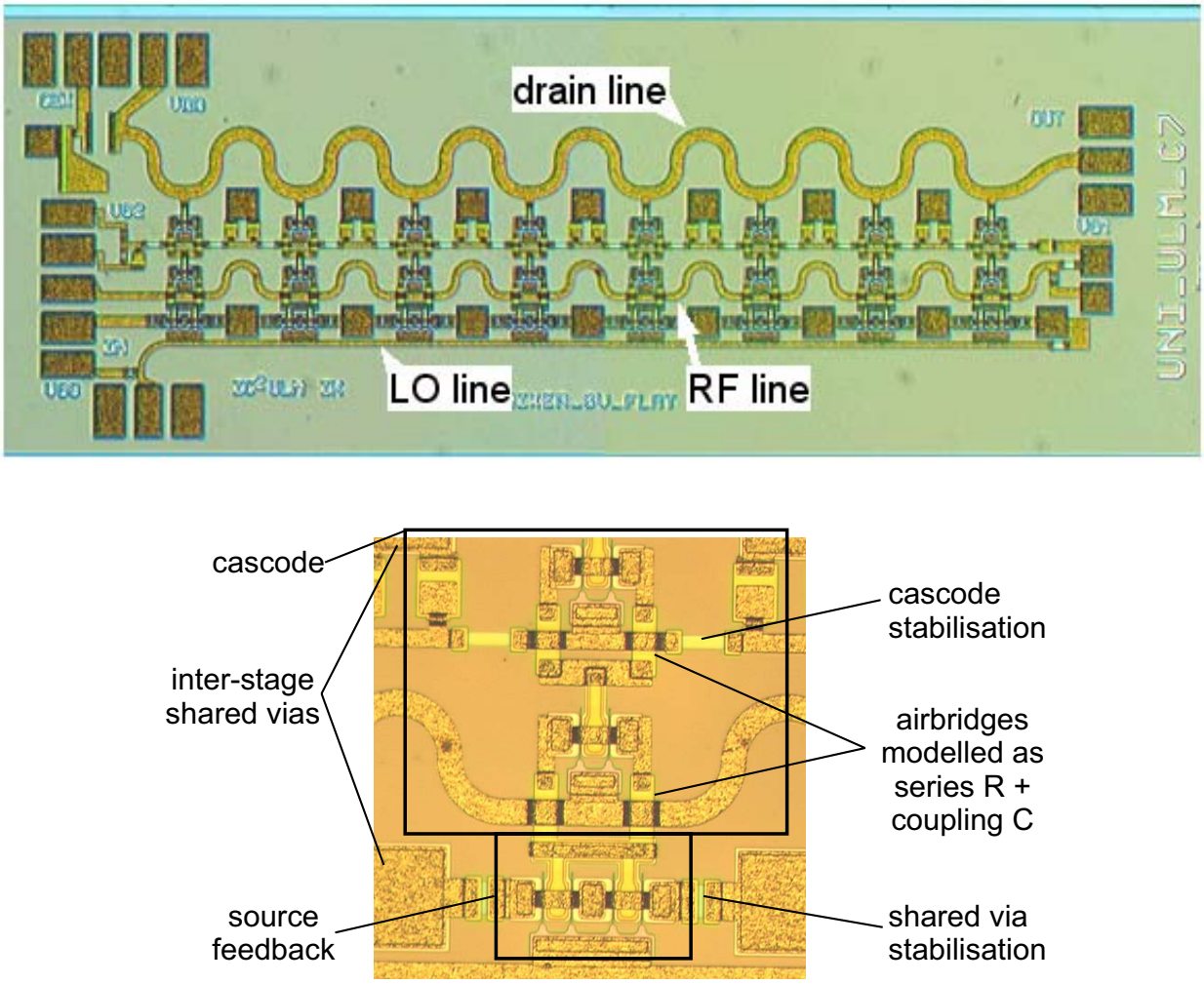

Figure 4.14: Microphotograph of the eight-stage distributed current-voltage feedback mixer and VGA, realised in the 0.15 μm GaAs pHEMT (PPH15) technology. Chip dimensions are $3.0 \times 1.1\,\mathrm{mm}^2$. Bottom: unit cell detail.

holes. The upper transistor in the cascode stage is grounded via a series R-C combination to ensure stability according to [132].

The MMIC is designed for both on-wafer characterisation using coplanar probes and for mounting on a test board in order to include external low-frequency termination- and bias networks.

4.2.3 VGA Operation

All measurements of the MMIC are carried out on-wafer, employing appropriate coplanar GSG and PGSGP probes to supply signals and bias voltages. Fig. 4.15 shows a photograph of the on-wafer measurement.

Bias conditions for maximum gain are $V_{\mathrm{G1}} = -0.15\,\mathrm{V}$, $V_{\mathrm{G2}} = 3\,\mathrm{V}$, $V_{\mathrm{G3}} = 0\,\mathrm{V}$ and $V_{\mathrm{DD}} = 6\,\mathrm{V}$, with $V_{\mathrm{G}i}$ representing the gate bias of transistor T_i. The model of the feedback

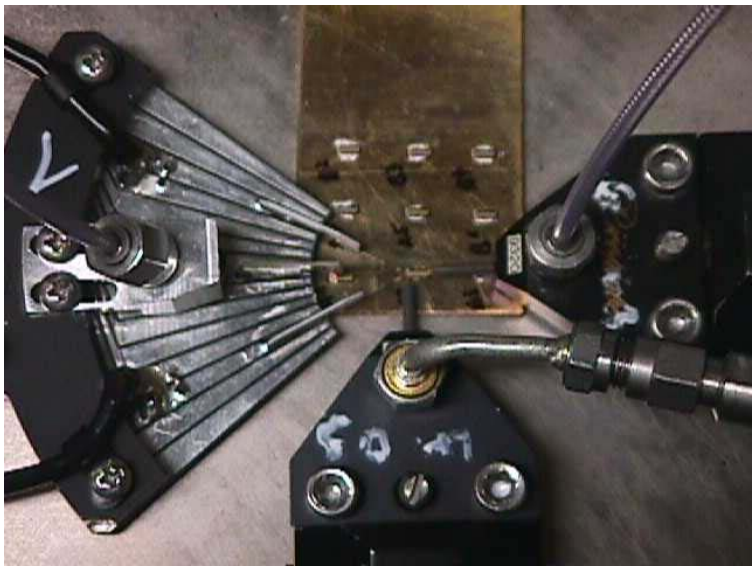

Figure 4.15: On-wafer measurements of the GaAs pHEMT distributed mixer/VGA are carried out with coplanar GSG and PGSGP probes.

FET	analysis type	I_{ds0}	I_{ds1}	I_{ds2}	I_{ds3}
$T_{1,2}$	small-signal	DC-IV	2 μs pulses	0.1 μs pulses	g_m/g_{ds}int.
	large-signal	DC-IV	2 μs pulses	0.1 μs pulses	not used
T_3	any	DC-IV	2 μs pulses	0.1 μs pulses	not used

Table 4.2: Drain current model composition for the GaAs pHEMT distributed mixer/VGA.

FET T_3 uses pulsed-IV with minimum pulse width (see chapter 2.5.1) in the dynamic part in order to increase its validity range to the full IV plane. As described in chapter 2.5.2, a dynamic IV characteristic derived by numerical integration of g_m/g_{ds} data deviates in regions close to threshold and for small V_{ds}. For small-signal analysis, the cascode transistors $T_{1/2}$ employ dynamic IV derived from integration of g_m/g_{ds}, while for large-signal analysis types, dynamic IV characteristics use pulsed-IV with minimum pulse width. Table 4.2 illustrates this model composition.

Small-Signal Gain

The measured maximum gain of the circuit is 11.8 ± 0.4 dB in a bandwidth of 3...43 GHz (Fig. 4.16). The lower bandwidth limitation is due to the relatively small capacitance of the on-chip drain line termination. The model over-estimates the gain by 1.3 dB and predicts an upper bandwidth of 42 GHz. Compared to the simulation with the nonlinear foundry model, however, significant improvement is achieved in the upper frequency range.

By varying the bias voltage of the feedback transistor, the gain can be controlled within roughly 5...12 dB without significant loss of bandwidth (Fig. 4.17, left). Simulation accurately reflects the gain dependence on the control voltage. This is shown in Fig. 4.17 for

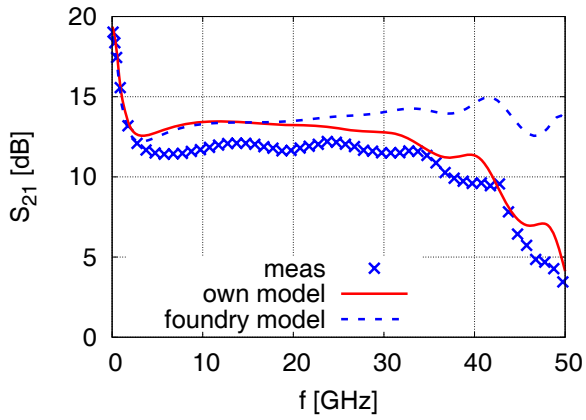

Figure 4.16: Measured and modelled small-signal gain under maximum gain conditions. The foundry large-signal model (PPH15NHF) is significantly less accurate both in gain and bandwidth prediction.

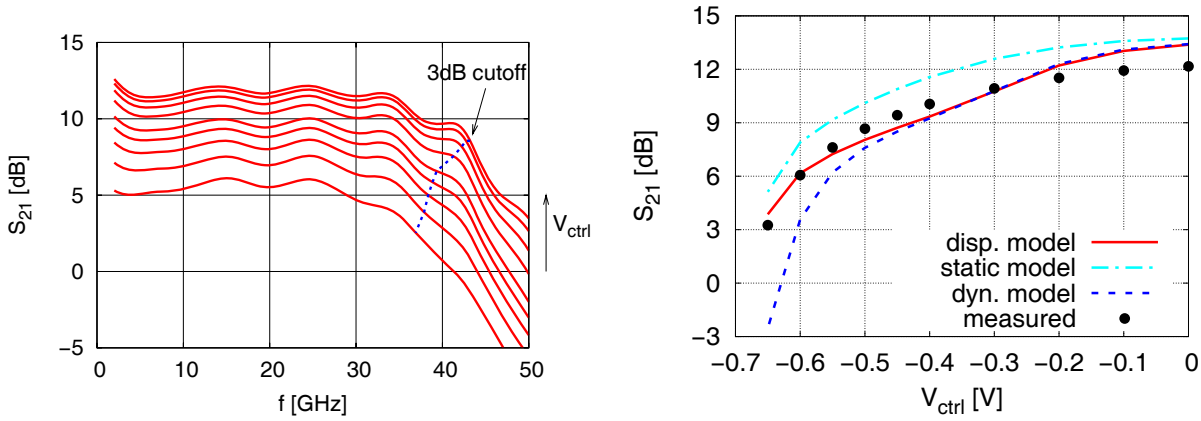

Figure 4.17: Measured gain versus control voltage (left). Model prediction at 25 GHz (right). Both the purely static and purely dynamic models result in less accuracy.

a frequency of 25 GHz. Making use of the model's capability of employing purely static drain current characteristics (by setting the schematic level parameter DISPMODEL=0, see chapter 3.7.2) and purely dynamic ones (DISPMODEL=3), the simulation error introduced by neglecting frequency dispersion can be evaluated. Both introduce a reduction in accuracy due to inherent model deviations: the purely static model accurately predicts the gain reduction, but is inaccurate in the analysis of absolute gain under all voltage conditions. A drain current model based on purely dynamic characteristics, however, must deviate from measured characteristics in the low gain region, since it wrongly predicts the bias situation in the feedback transistor.

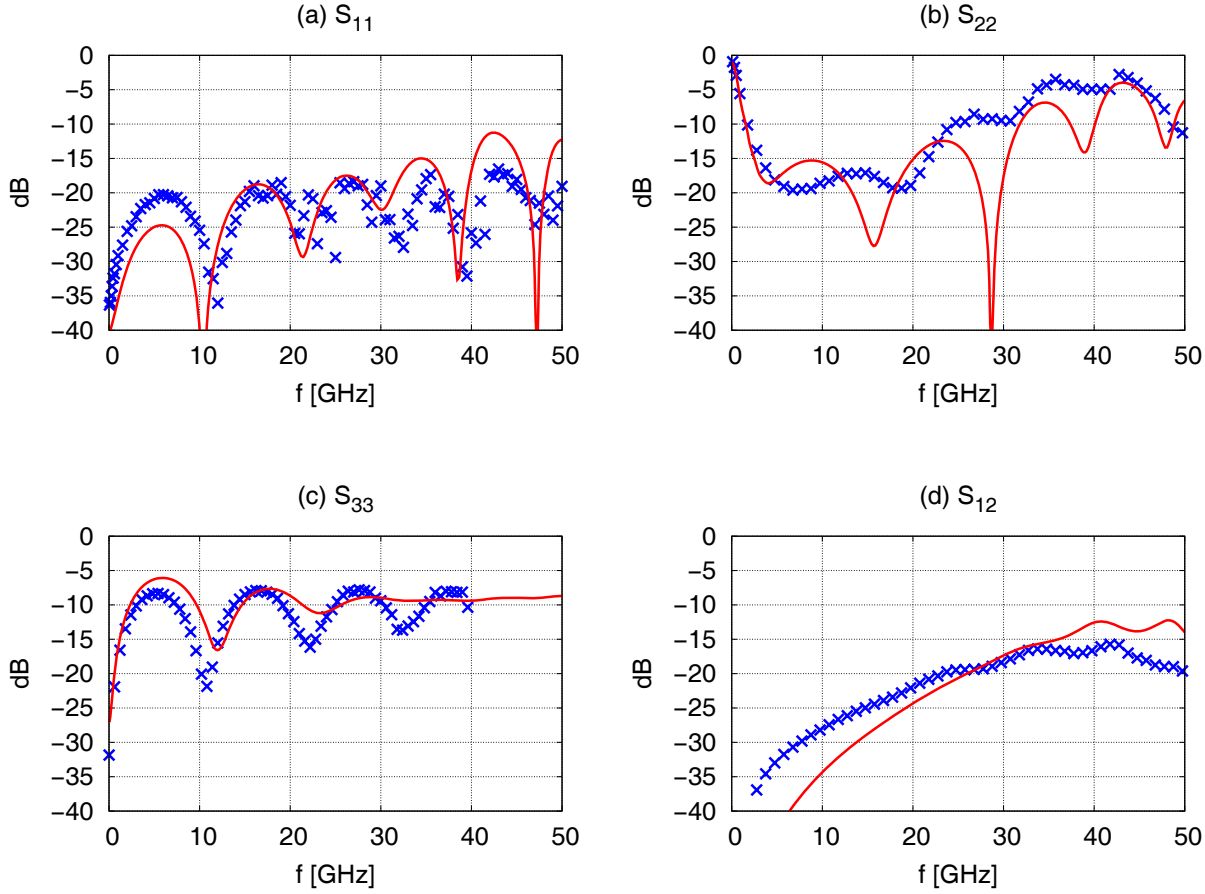

Figure 4.18: Measured (points) and modelled (lines) port matching and reverse isolation. RF port (S_{11}), IF port (S_{22}), LO port (S_{33}) and IF to RF reverse isolation (S_{12}).

Port Matching and Reverse Isolation

Fig. 4.18 shows measured and modelled port matching and reverse isolation. In accordance with the travelling-wave principle, good power matching is achieved across the whole bandwidth. Best matching is achieved at the RF input port, better than 18 dB across the whole bandwidth. The output port achieves more than 15 dB matching up to 22 GHz and stays better than 5 dB up to 50 GHz. The LO port achieves better than 8 dB matching up to 40 GHz. Model prediction of all values, including the reverse isolation S_{12} is adequate.

Noise

The VGA's 50 Ω noise figure (NF_{50}) has been measured using an NP5 noise figure meter for frequencies up to 26 GHz and a Rohde&Schwarz ZVK network analyser up to 40 GHz (Fig. 4.19). NF_{50} is as low as 3.6 dB at 8 GHz and ramps up to 9 dB at 38 GHz, before the gain starts to drop. For several reasons, of course, noise must be expected to be significantly degraded in this configuration. Besides the fact that the PPH15 technology is optimised for power, not for noise, the circuit is not operated under minimum noise bias conditions.

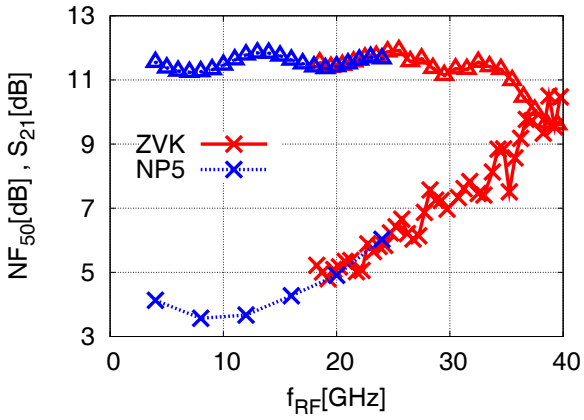

Figure 4.19: Measured NF_{50} of the distributed mixer/VGA MMIC.

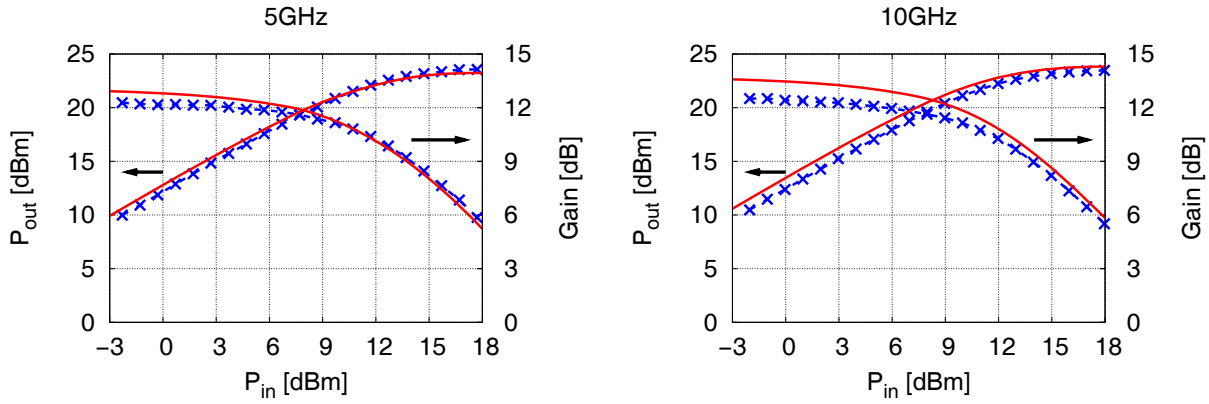

Figure 4.20: One-tone power measurement (symbols) and simulation (lines) for frequencies of 5 GHz (left) and 10 GHz (right).

Mostly however, the feedback transistor reduces both maximum gain and minimum noise of the cascode amplifying stages.

One-tone power

Amplifier linearity is evaluated in a one-tone power measurement and for maximum gain conditions. Output power together with the DC supply current is recorded as a function of input power. All power levels are calibrated to the circuit's in- and output reference planes. Besides gain compression, this data forms the basis of the self-biasing effect as well as PAE.

Fig. 4.20 shows the comparison of measured and simulated output power and gain for fundamental frequencies of 5 GHz and 10 GHz. In 1 dB compression, the circuit is capable of delivering 20 dBm into a 50 Ω load. Despite over-estimating the gain, the model accurately predicts saturated output power (see table 4.3).

The self-biasing effect arises from non-symmetrical signal compression in the time domain

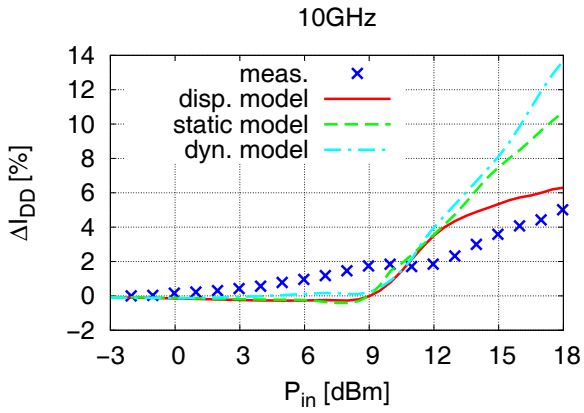

Figure 4.21: Self-biasing effect on the DC supply current. Percentage of current change relative to quiescent condition. Comparison of the measurement to the purely static-, purely dynamic- and dispersion models.

@10 GHz	unit	measurement	simulation
$P_{\text{in,1dB}}$	dBm	8.5	7.3
$P_{\text{out,1dB}}$	dBm	20.0	19.9
PAE_{max}	%	20.9	22.4
$P_{\text{in,PAEmax}}$	dBm	15.1	15.1

Table 4.3: Summary of measured and modelled VGA power characteristics.

and a resulting DC component in the frequency spectrum. Depending on the quiescent conditions of the transistors, the supply current will rise or fall with increasing input power levels. This effect is shown in Fig. 4.21 together with the simulation results of the full dispersion model as well as purely static and purely dynamic models. There is a 3% deviation between model and measurement (135 mA measured, 139 mA simulated) in supply current at low power levels, which can very well be attributed to the relatively strong cross-wafer variation of transistor drain current. Apart from that, the dispersion model is most accurate in predicting the rise of supply current with increasing input power, with both the purely static- and dynamic models over-estimating the self-biasing effect. It is interesting to note that at low power levels the dispersion model is identical to the purely static model, since power compression is not yet affecting the DC situation. At high power levels, however, the gain compression is governed by the dynamic IV characteristics, while its effect on supply current is reflected in static operation. Like PAE, the self-biasing effect therefore is a figure of merit which combines static and dynamic device characteristics.

Finally, PAE is evaluated according to equation (2.6). Fig. 4.22 shows measured and modelled results for 5 GHz and 10 GHz fundamental frequencies. In both cases, maximum PAE is found to be 20% at about 15 dBm of input power. Again, the dispersion model is most accurate in predicting this figure of merit made up of both static and dynamic

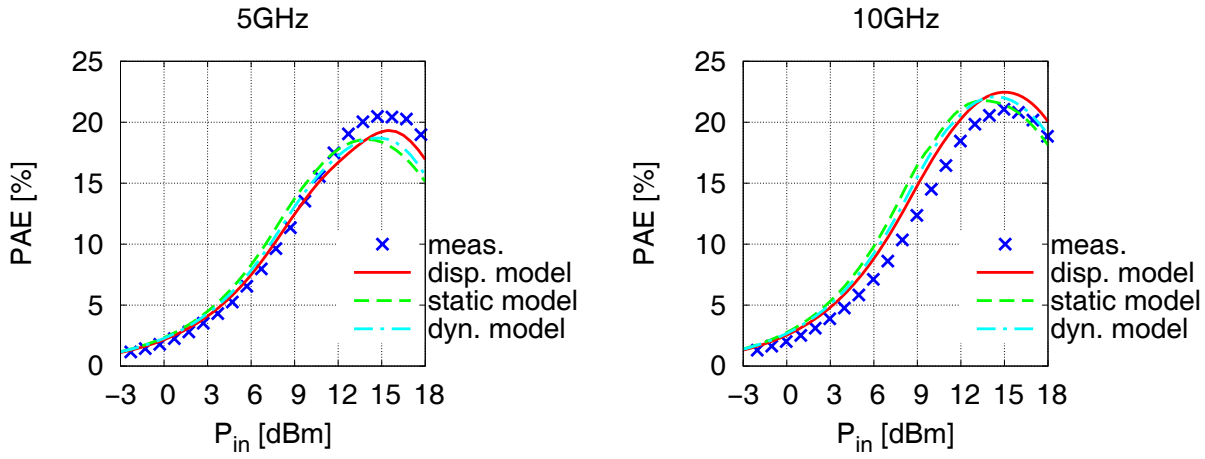

Figure 4.22: PAE at 5 GHz (left) and 10 GHz (right). The full dispersion model is most accurate in predicting both the absolute maximum PAE and its respective input power level.

contributions. In particular, both the purely static and purely dynamic models predict a too low input power for maximum PAE, since they over-estimate both gain compression and the self-biasing effect. Table 4.3 summarises the comparison of measured and modelled one-tone power characteristics under VGA operation.

4.2.4 Mixer Operation

The frequency translating effect is obtained by applying a LO drive signal to the gate line of the feedback transistor. Bias conditions for optimum mixer operation are $V_{G1} = 0.5\,\mathrm{V}$, $V_{G2} = 3\,\mathrm{V}$, $V_{G3} = -0.1\,\mathrm{V}$ and $V_{DD} = 5\,\mathrm{V}$. To satisfy the travelling-wave principle and to guarantee proper power matching, IF frequencies for mixer operation have to be chosen above the lower cut-off. If this condition is violated, measured conversion gain values increase by up to 6 dB. Conversion gain measurements are carried out using both the Rohde&Schwarz ZVK network analyser and a conventional setup employing two RF sources and a spectrum analyser. All power levels are corrected to the MMIC in- and output reference planes.

Conversion gain versus RF frequency

The MMIC may be employed for downconversion of a multi-decade RF spectrum to fixed f_{IF} by using swept f_{LO}. On the other hand, a fixed f_{LO} may downconvert an upper RF spectrum to an equally broad IF spectrum. The two cases are illustrated in Fig. 4.23, together with the measured and simulated conversion gain of the mixer. These results are obtained with 5 dBm LO power and for a small RF power of -10 dBm.

For a fixed f_{IF} of 2 GHz, the mixer achieves a measured conversion loss of $G_c = -2.5 \pm 0.6\,\mathrm{dB}$ with an RF bandwidth exceeding the measurable range of 40 GHz. Model prediction is $G_c = -2.4 \pm 0.9\,\mathrm{dB}$. In the case of a fixed f_{LO} of 25 GHz, an RF spectrum of approx.

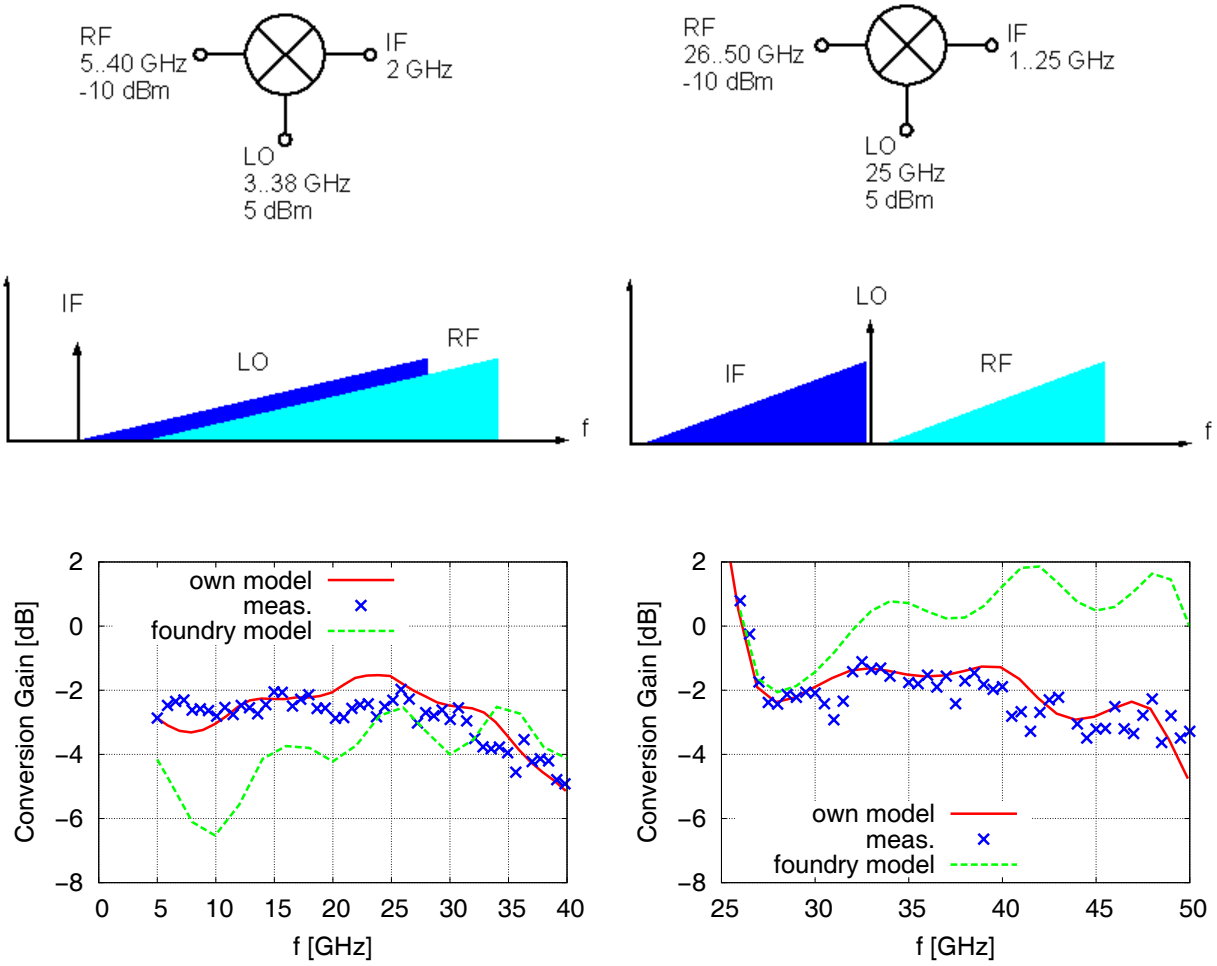

Figure 4.23: Conversion gain of the distributed GaAs pHEMT mixer MMIC. Downconversion to fixed f_{IF} (left). Downconversion using fixed f_{LO} (right). Measurement results are compared to simulations using the present model as well as to the nonlinear model from the foundry design kit.

27 GHz to more than 50 GHz is downconverted with a measured conversion gain of $G_{\mathrm{c}} = -2.3 \pm 1.2\,\mathrm{dB}$. The simulated result was $G_{\mathrm{c}} = -2.4 \pm 1.1\,\mathrm{dB}$. The excellent agreement between measured and simulated conversion gain confirms the large-signal quality of the model, particularly when compared to the nonlinear model contained in the foundry design kit (dashed lines in Fig. 4.23).

Mixer Linearity

Mixer linearity is evaluated using swept RF input power and measuring output power at the IF frequency. As explained in chapter 4.2.1, the current-voltage feedback mixer provides inherently good linearity, since amplifying stages are essentially operated under class A conditions. All other distributed mixer concepts, namely the g_{m}-, cascode- and drain mixers must suffer from poor linearity characteristics, since their active devices are biased either

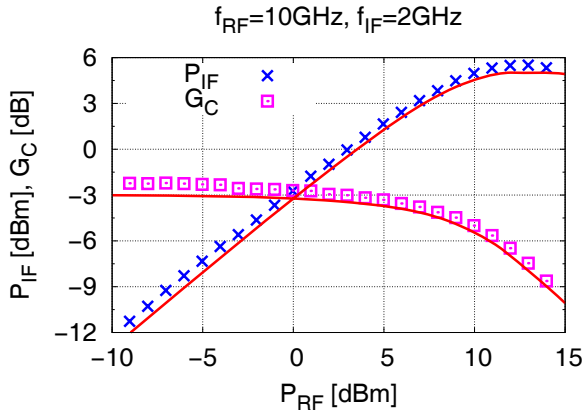

Figure 4.24: Conversion gain compression for $f_{\mathrm{IF}} = 2\,\mathrm{GHz}$ and $f_{\mathrm{RF}} = 10\,\mathrm{GHz}$. Measured (symbols) versus modelled (lines) results.

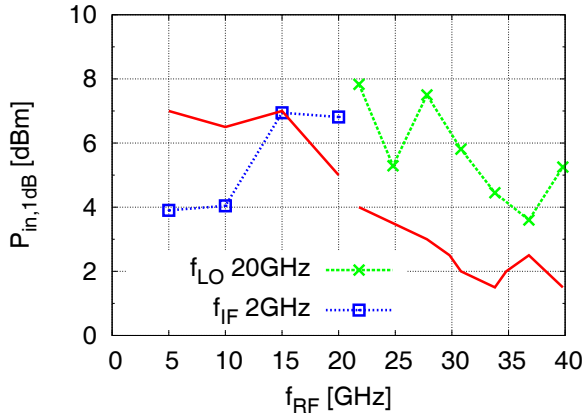

Figure 4.25: Measured (symbols) and modelled (lines) RF input power at 1 dB compression of conversion gain. Sweep of the RF frequency in a fixed $f_{\mathrm{IF}} = 2\,\mathrm{GHz}$ and fixed $f_{\mathrm{LO}} = 20\,\mathrm{GHz}$ setup.

close to threshold or in the knee region.

Fig. 4.24 shows the measured IF output power together with conversion gain as a function of RF input power. Frequency conditions are $f_{\mathrm{IF}} = 2\,\mathrm{GHz}$ and $f_{\mathrm{RF}} = 10\,\mathrm{GHz}$ under low-side injection of 5 dBm LO power. The measurement reveals an input related 1 dB compression point of 4.0 dBm for conversion gain. Although the model predicts a $P_{\mathrm{in,1dB}}$ of 6.5 dBm, it is found to be very accurate in the high power regime.

The same power measurement is performed for sweeps of f_{RF} in a setup with fixed $f_{\mathrm{IF}} = 2\,\mathrm{GHz}$ and fixed $f_{\mathrm{LO}} = 20\,\mathrm{GHz}$. Fig. 4.25 shows the input related 1 dB compression point as a function of RF frequency. It is found to be as high as 5.7 ± 2.1 dBm over the whole spectrum. Particularly for high RF frequencies, the model is found to be too conservative, deviating by between 2..4 dB from measured results.

Ref.	Type/Technology	chip size [mm^2]	BW [GHz]	G_c [dB]	P_{LO} [dBm]	ICP_{1dB} [dBm]
[136]	0.2 μm GaAs HEMT $g_m$mixer/combiner	4	10..50	-3	5	-
[138]	0.15 μm GaAs HEMT cascode mixer	1.8	3..40	3.6	5	-
[139]	0.15 μm GaAs HEMT drain mixer	1.7	3..33	-4	13	<0
here	0.15 μm GaAs HEMT current feedback	3.4	2..>50	-2.3 ± 1.2	5	5.7 ± 2.1

Table 4.4: Figures of merit for measured performance of published distributed mixers in a comparison to the current feedback concept.

Table 4.4 shows a summary of measured performance of the current feedback topology compared to other distributed mixer concepts, realised in comparable technologies. Best conversion gain is obtained in the cascode mixer. The drain mixer requires prohibitively large LO power. The g_m-mixer achieves a performance comparable to the current feedback concept. Since a combiner is required, however, a tradeoff will always have to be made between conversion gain and chip size. Additionally, the current feedback concept is the only one among the distributed mixers capable of acting as VGA, too.

Chapter 5

Conclusion

A custom HFET model was developed and applied in the design of several MMIC applications. The model is expressly dedicated to microwave circuit design. Its analytical nonlinear equations provide a compromise between physical interpretability, numerical efficiency and global validity.

As an essential part of the overall model, the COBRA expression features a highly efficient and accurate description of complex HFET drain current characteristics. A modification was introduced to include the reduction of drain current due to the self-heating effect as well as for improved description of gain compression.

A new approach to frequency dispersion modelling extends the model's validity range from the microwave- down to the low-frequency and DC regimes. The proposed dispersion model relies on conventional device characterisation techniques and standard parameter extraction procedures. The inclusion of multiple dispersion time constants and exponentially decaying step responses accurately reflects the physical nature of individual dispersion effects, providing a correct description of transitions between dispersion regimes both in the time- and frequency domain. As a consequence, the model allows for accurate assessment of dynamic (gain, matching, intermodulation etc.), static (e.g. biasing, power consumption) as well as combined (e.g. PAE, self-biasing) figures of merit during the design phase. Additionally, the simulation error introduced by neglecting frequency dispersion when using purely static or dynamic drain current models, can be evaluated.

A unified capacitance model approach defines the frame for sets of charge-conservative expressions for gate capacitance characteristics. The final equations employed here resemble in composition the Curtice IV model, e.g. in terms of transition from linear- to saturated- and from sub-threshold- to active voltage regimes.

The universal validity of the model was demonstrated by applying it to several different HEMT technologies, encompassing both state-of-the-art GaAs pHEMT low-noise and power processes, high-frequency InP pHEMTs as well as novel concepts such as the strained-Si/SiGe mHEMT. Both the nonlinear capacitance and dispersion models proved to apply very well to all HEMT technologies.

The model was fully implemented into a circuit design environment. The corresponding

design kit along with a dedicated parameter extraction software package were contributed to the European TARGET network of excellence software pools.

Innovative MMIC design was carried out on the basis of the model. The first SiGe mHEMT MMICs were successfully realised. A new travelling-wave circuit concept allows for simultaneous ultra-broadband mixing and variable gain operation. The excellent agreement of measured and modelled circuit performance validates the model's suitability for being employed in millimeter- and microwave circuit design, notably in conjunction with frequency-dispersive technologies.

Bibliography

[1] Kwok K. Ng, *Complete Guide to Semiconductor Devices. Chapter 22: Modulation-Doped Field-Effect Transistor (MODFET)*, ser. 2. McGRaw-Hill, 1995.

[2] R. F. Pierret, *Semiconductor Device Fundamentals: Part III Field-Effect Devices*. Addison-Wesley Publishing Company, 1996.

[3] M. Shur, *Physics of Semiconductor Devices*. Prentice Hall Inc., Englewood Cliffs, N.J., 1990.

[4] S. M. Sze, *High-Speed Semiconductor Devices. Chapter 5: Heterostructure Field-Effect Transistors*. John Wiley, New York, 1990.

[5] "IBM keeps Moore's law on track," *Materials Today*, p. 5, July/Aug. 2001.

[6] A. Sadek, K. Ismail, M.A. Armstrong, D.A. Antoniadis, F. Stern, "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors," *IEEE Trans. Electron Devices*, vol. 43, no. 8, pp. 1224–1232, Aug. 1996.

[7] K. Rim, J.L. Hyot, J.F. Gibbons, "Fabrication and Analysis of Deep Sub-micron Strained-Si n-MOSFETs," *IEEE Trans. Electron Devices*, vol. 47, no. 7, pp. 1406–1415, July 2000.

[8] A.G. O'Neill, D.A. Antoniadis, "Investigation of Si/SiGe based FET geometries for high frequency performance by computer simulation," *IEEE Trans. Electron Devices*, vol. 44, no. 1, pp. 80–88, Jan. 1997.

[9] K. Ismail, J.O. Chu, M. Arafa, "Integrated enhancement and depletion mode FETs in modulation-doped Si/SiGe heterostructures," *IEEE Electron Device Letters*, vol. 18, no. 9, pp. 435–437, Sept. 1997.

[10] W. Lu, X.W. Wang, R. Hammond, A. Kuliev, S. Koester, J.O. Chu, K. Ismail, T.P. Ma, I. Adesida, "p-Type SiGe Transistors with Low Gate Leakage Using SiN Gate Dielectric," *IEEE Electron Device Letters*, vol. 20, no. 10, pp. 514–516, Oct. 1999.

[11] M. Arafa, K. Ismail, J.O. Chu, B.S. Meyerson, I. Adesida, "A 70GHz f_T Low Operating Bias Self-Aligned p-type SiGe MODFET," *IEEE Electron Device Letters*, vol. 17, no. 12, pp. 586–588, Dec. 1996.

[12] M. Arafa, P. Fay, K. Ismail, J.O. Chu, B.S. Meyerson, I. Adesida, "DC and RF Performance of 0.25μm p-Type SiGe MODFET," *IEEE Electron Device Letters*, vol. 17, no. 9, pp. 449–451, Sept. 1996.

[13] U. König, H. Dämbkes, "SiGe HBTs and HFETs," *Solid-State Electronics*, vol. 38, no. 9, pp. 1595–1602, 1995.

[14] U. König, M.Zeuner, G. Höck, T. Hackbarth, M. Glück, T. Ostermann, M. Saxarra, "n-type and p-type SiGe HFETs and circuits," *Solid-State Electronics*, vol. 43, pp. 1383–1388, 1999.

[15] F. Schäffler, "Strained Si/SiGe Heterostructures for Device Applications," *Solid-State Electronics*, vol. 37, no. 4-6, pp. 765–771, 1994.

[16] *SIGMUND IST 1999-1044: SiGe Hetero MOS- and MODFETs for ultimate scaling towards sub-100nm devices, homepage*. [Online]. Available: http://www.imec.be/sigmund/

[17] *Training and Mobility of Researchers Network: Advanced SiGe Hetero Structure Devices for Millimeter-Wave Applications. Contract ERB 4061 PL97-0841, homepage*, 1998-2001. [Online]. Available: http://www-ebs.e-technik.uni-ulm.de/TMR/

[18] *HMOS, SiGe for MOS applications, EPSRC award GR/N65844/01, homepage*. [Online]. Available: http://physweb.spec.warwick.ac.uk/sige/home.htm

[19] F. Schäffler, U. König, *MBE growth and device applications of modulation doped Si/SiGe heterostructures in low-dimensional electronic systems*, ser. in G. Bauer, F. Kuchar, H. Heinrich, Springer Series in Solid State Sciences. Springer Verlag Berlin, 1992, vol. 111.

[20] K. Lyutovich, M. Bauer, E. Kasper, H.J. Herzog, T. Perova, R. Maurice, C. Hofer, C. Teichert, "Thin SiGe buffers with high Ge content for n-MODFETs," *Materials Science and Engineering B*, vol. 89, pp. 1–3, 2002.

[21] C. Rosenblad, M. Kummer, H.D. Deller, T. Graf, A. Dommann, T. Hackbarth, G. Höck, E. Müller, H. von Känel, "Low energy plasma enhanced chemical vapour deposition - plasma enhanced deposition of epitaxial Si and Ge," *Proc. of Material Research Soc. Symp.*, vol. 696, no. N4.7.1-N4.7.12, 2002.

[22] S. Mantl, S.M. Hogg, B. Holländer, S. Lenk, M. Luysberg, M. Grimm, H. Trinkaus, H.J. Herzog, T. Hackbarth, R. Loo, M. Bauer, "Strain relaxed ultrathin SiGe buffer layers on blanket and patterned Si and SOI wafers for strained Si produced by He ion implantation and annealing," *Proc. Int. Electron Device Meeting IEDM*, 2002.

[23] G. Höck, M. Glück, T. Hackbarth, H.J. Herzog, E. Kohn, "Carrier mobilities in modulation doped $Si_{1-x}Ge_x$ heterostructures with respect to FET applications," *Thin Solid Films*, vol. 336, pp. 141–144, 1998.

[24] S. Takagi, A. Toriumi, M. Iwase, H. Tango, "On the Universality of Inversion Layer Mobility in Si-MOSFETs: Part I - Effects of Substrate Impurity Concentration," *IEEE Trans. Electron Devices*, vol. 41, no. 12, pp. 2357–2362, Dec. 1994.

[25] ——, "On the Universality of Inversion Layer Mobility in Si-MOSFETs: Part II - Effects of Surface Orientation," *IEEE Trans. Electron Devices*, vol. 41, no. 12, pp. 2363–2368, Dec. 1994.

[26] H. von Känel, M. Kummer, G. Isella, E. Müller, T. Hackbarth, "Very high hole mobilities in modulation-doped Ge quantum wells grown by low-energy plasma enhanced chemical vapour deposition," *Applied Physics Letters*, vol. 80, no. 16, pp. 2922–2924, 2002.

[27] M. Enciso-Aguilar, F. Aniel, P. Crozat, R. Adde, H.-J. Herzog, T. Hackbarth, U. König, and H. von Känel, "DC and high frequency performance of a 0.1 μm n-type $Si/Si_{0.6}Ge_{0.4}$ MODFET with f_{max}=188 GHz at 300 K and f_{max}=230 GHz at 50 K," *Electronics Letters*, vol. 39, pp. 149–150, 2003.

[28] J.S. Koester, K.L. Saenger, J.O. Chu, Q.C. Ouyang, J.A. Ott, K.A. Jenkins, D. F. Canaperi, J.A. Tornello, C.V. Jahnes, S.E. Steen, "Laterally Scaled Si-$Si_{0.7}Ge_{0.3}$ n-MODFETs with f_{max}>200GHz and Low Operating Bias," *IEEE Electron Device Letters*, vol. 26, no. 3, pp. 178–180, March 2005.

[29] T. Hackbarth, M. Zeuner, U. König, "The Future of SiGe Beyond HBT Applications," *Advanced Silicon*, pp. 32–35.

[30] T. Hackbarth, H.-J. Herzog, K.-H. Hieber, U. König, M. Bollani, D. Chrastina, H. von Känel, "Reduced self-heating in Si/SiGe field-effect transistors on thin virtual substrates prepared by low-energy plasma-enhanced chemical vapor deposition," *Applied Physics Letters*, vol. 83, no. 26, pp. 5464–5466, Dec. 2003.

[31] U. König, M. Glück, G. Höck, "Si/SiGe field-effect transistors," *Journal Vac. Science Tech. B*, vol. 16, no. 5, pp. 2609–2614, 1998.

[32] H. Schumacher, *Modern Semiconductor Devices, Lecture Script.* University of Ulm, 2004.

[33] S. C. Jain, M. Willander, *Silicon-Germanium Strained Layers and Heterostructures*, 2nd ed., ser. Semiconductors and Semimetals. Academic Press, Elsevier, 2003, vol. 74.

[34] A. Vilches, K. Fobelets, K. Michelakis, S. Despotopoulos, C. Papavassiliou, T. Hackbarth, U. König, "Monolithic microwave amplifiers using SiGe n-MODFET device," *Electronics Letters*, vol. 39, no. 12, pp. 884–886, June 2003.

[35] C. Papavassiliou, K. Fobelets, C. Toumazou, "SiGe Hetero-FETs potential for Microwave Applications," *Proc. TWHM, Kyoto, in IEICE Trans. Electron.*, vol. E00-A, 2000.

[36] F. Aniel, N. Zerounian, R. Adde, M. Zeuner, T. Hackbarth, U. König, "Low Temperature Analysis of 0.25 μm T-Gate Strained Si/SiGe n-MODFETs," *IEEE Trans. Electron Devices*, vol. 47, no. 7, pp. 1477–1483, July 2000.

[37] M. Enciso, F. Aniel, L. Giguerre, P. Crozat, R. Adde, M. Zeuner, T. Hackbarth, "High Frequency Properties of Si/SiGe n-MODFETs: Dependence on Gate Length and Temperature," *in Proc. 9th European Microwave Week GAAS, London*, Sept. 2001.

[38] I. Kallfass, M. Zeuner, U. König, H. Schumacher, and T. J. Brazil, "A Model for SiGe MODFETs with Improved Large-Signal Quality and Frequency Range," *in Proc. 10th GaAs Symposium, European Microwave Week, Milano, Italy*, Sept. 2002.

[39] I. Kallfass, T. J. Brazil, B. OhAnnaidh, P. Abele, T. Hackbarth, M. Zeuner, U. König, H. Schumacher, "Large Signal Modelling including Low-Frequency Dispersion of N-channel SiGe MODFETs and MMIC Applications," *Solid-State Electronics*, vol. 48, no. 8, pp. 1433–1441, Aug. 2004.

[40] J. Grünenpütt, UMS, "personal conversation."

[41] D. Keiper, P. Velling, A. Brennemann, M. Agethen, C. van den Berg, R. M. Bertenburg, "MOVPE growth of InAlAs using TBAs and DitBuSi for HEMT applications," *Journal of Crystal Growth*, vol. 248, pp. 153–157, Feb. 2003.

[42] P. K. Bhattacharya (Ed.), *Properties of lattice-matched and strained Indium Gallium Arsenide. Chapters 3 and 4. Pages 67, 92, 118.* INSPEC, the Institution of Electrical Engineers, London, UK, 1993.

[43] W. Liu, X. Jin, J. Chen et. al., *BSIM3v3 MOSFET Model, User Manual.* University of California, Berkeley, 1999. [Online]. Available: http://www-device.eecs.berkeley.edu/~bsim3/intro.html

[44] M. Bucher, C. Lallement, C. Enz, F. Théodoloz, F. Krummenacher, *The EPFL-EKV MOSFET Model Equations for Simulation, homepage*, June 1997. [Online]. Available: http://legwww.epfl.ch/ekv/index.html

[45] T. A. Fjeldly, A. Ytterdal, M. Shur, *Introduction to Device Modelling and Circuit Simulation. Chapter 6: Advanced FET Modeling.* John Wiley, New York, 1998.

[46] C.J. Wei, Y. A. Tkachenko, D. Bartle, "Table-based Dynamic FET Model Assembled From Small-Signal Models," *IEEE Trans. Microwave Theory and Techn.*, vol. 47, no. 6, pp. 700–705, June 1999.

[47] K. Koh, H. M. Park, S. Hong, "A Spline Large-Signal FET Model Based on Bias-Dependent Pulsed I-V Measurement," *IEEE Trans. Microwave Theory and Techn.*, vol. 50, no. 11, pp. 2598–2603, Nov. 2002.

[48] T. Wang, T.J. Brazil, "The Estimation of Volterra Transfer Functions with Applications to RF Power Amplifier Behaviour Evaluation for CDMA Digital Communication," *in Proc. IEEE MTT-S Int. Microwave Symp., Boston, Massachusetts*, June 2000.

[49] D. Schreurs, N. Tufillaro, J. Wood, D. Usikov, L. Barford, D.E. Root, "Development of Time-Domain Behavioural Nonlinear Models for Microwave Devices and ICs from Vectorial Large-Signal Measurements and Simulations," *in Proc. 8th Gallium Arsenide and Other Semiconductors Application Symposium, Paris*, Oct. 2000.

[50] A Ahmed, S.S. Islam, A.F.M. Anwar, "A Temperature-Dependent Nonlinear Analysis of GaN/AlGaN HEMTs Using Volterra Series," *IEEE Trans. on Microwave Theory and Techn.*, vol. 49, no. 9, pp. 1518–1524, Sept. 2001.

[51] D.V. Lang, "Deep-level transient spectroscopy: A new method to characterize traps in semiconductors," *Journal of Applied Physics*, vol. 45, no. 7, pp. 3023–3032, July 1974.

[52] P. C. Canfield, S. C. F. Lam, D. J. Allstot, "Modelling of Frequency and Temperature Effects in GaAs MESFETs," *IEEE Journal Solid-State Circuits*, vol. 25, no. 1, pp. 299–306, Feb. 1990.

[53] E. Kasper, *Properties of strained and relaxed Silicon Germanium.* INSPEC, the Institution of Electrical Engineers. Chapter 3.2: Thermal properties of SiGe, 1995, vol. 12.

[54] P.H. Ladbrooke, S.R. Blight, "Low-Field Low-Frequency Dispersion of Transconductance in GaAs MESFETs with Implications for Other Rate-Dependent Anomalies," *IEEE Trans. on Electron Devices*, vol. 33, no. 3, pp. 257–267, Mar. 1988.

[55] R Reuter, M. Agethen, U. Auer, S van Waasen, D. Peters, W. Brockerhoff, F. J. Tegude, "Investigation and Modeling of Impact Ionization with Regard to the RF and Noise Behaviour of HFET," *IEEE Trans. Microwave Theory and Techn.*, vol. 45, no. 6, pp. 977–983, June 1997.

[56] R. Vetury, N. Q. Zhang, S. Keller, U. K. Mishra, "The Impact of Surface States on the DC and RF Characteristics of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 560–566, March 2001.

[57] S. C. Binari, K. Ikossi, J. A. Roussos, W. Kruppa, D. Park, H. B. Dietrich, D.D. Koleske, A. E. Wickenden, R. L. Henry, "Trapping Effects and Microwave Power Performance in AlGaN/GaN HEMTs," *IEEE Trans. on Electron Devices*, vol. 48, no. 3, pp. 465–471, Sept. 2001.

[58] A. Siligaris, G. Dambrine, F. Danneville, "Non-Linear Modelling of the Kink Effect in Deep Sub-micron SOI MOSFET," *in Proc. 12th GaAs Symposium, European Microwave Week, Amsterdam*, pp. 47–50, 2004.

[59] Y. Yang, Y.Y. Woo, J. Yi, B. Kim, "A New Empirical Large-Signal Model of Si LDMOSFETs for High-Power Amplifier Design," *IEEE Trans. Microwave Theory and Techn.*, vol. 9, no. 49, pp. 1626–1633, Sept. 2001.

[60] T.J. Brazil, "vfetdc11: Electrothermal DC FET solver software," Aug. 2003.

[61] M. Berroth, E. Chigaeva, I. Dettmann, N. Wieser, W. Walthes, M. Grözing, H. Roll, O. Breitschädel, J. Off, B. Kuhn, F. Scholz, H. Schweizer, "Non-linear GaN-HEMT Modelling Including Thermal Effects," *in Proc. Second Joint Symposium on Opto- and Microelectronic Devices and Circuits, Stuttgart*, pp. 236–239, March 10-16 2002.

[62] M. Rudolph, R. Doerner, K. Beilenhoff, P. Heymann, "Scalable GaInP/GaAs HBT Large-Signal Model," *in Proc. IEEE MTT-S Int. Microwave Symp., Boston, Massachusetts*, June 2000.

[63] BSIM group, *BSIMSOI4.0 MOSFET model, User's manual. Chapter 5: Temperature Dependence and Self-Heating*, university of California, Berkeley, November 2005.

[64] M. Schroter, "HICUM: A scalable physics-based compact bipolar transistor model. Description of model version 2.1," Dec. 2000. [Online]. Available: www.iee.et.tu-dresden.de

[65] J. Conger, A. Peczalski, M. S. Shur, "Modeling Frequency Dependence of GaAs MESFET Characteristics," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 1, pp. 71–76, Jan. 1994.

[66] C. Camacho-Penalosa, C.S. Aitchison, "Modelling Frequency Dependence of Output Impdance of a Microwave MESFET at Low Frequencies," *Electronics Letters*, vol. 21, no. 12, pp. 528–529, June 1985.

[67] M. Hirose, Y. Kitaura, N. Uchitomi, "A Large-Signal Model of Self-Aligned Gate GaAs FETs for High-Efficiency Power-Amplifier Design," *IEEE Trans. on Microwave Theory and Techn.*, vol. 47, no. 12, pp. 2375–2381, Dec. 1999.

[68] S. Choi, M. B. Das, "Origin and Modeling of the Frequency Dependent Output Conductance in Microwave GaAs MESFET's With Buried p Layer," *IEEE Trans. Electron Devices*, vol. 41, no. 10, pp. 1725–1733, Oct. 1994.

[69] I. Angelov, L. Bengtsson, M. Garcia, "Extensions of the Chalmers Nonlinear HEMT and MESFET Model," *IEEE Trans. Microwave Theory and Techn.*, vol. 44, no. 10, pp. 1664–1674, October 1996.

[70] Agilent Technologies, *Advanced Design System Manual: Nonlinear Devices*, Dec. 2003.

[71] J.W. Lee, K.J. Webb, "A Temperature-Dependent Nonlinear Analytic Model for AlGaN-GaN HEMTs on SiC," *IEEE Trans. Microwave Theory and Techn.*, vol. 52, no. 1, pp. 2–9, Jan. 2004.

[72] S.S. Islam, A. F. M. Anwar, "Self-Heating and Trapping Effects on the RF Performance of GaN MESFETs," *IEEE Trans. Microwave Theory and Techn.*, vol. 52, no. 4, pp. 1229–1236, Apr. 2004.

[73] S.S. Islam, A.F.M. Anwar, R.T. Webster, "A Physics-based Frequency Dispersion Model of GaN MESFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 6, pp. 846–853, June 2004.

[74] A. Santarelli, G. Zucchelli, R. Paganelli, G. Vannini, F. Filicori, "Equivalent-Voltage Description of Low-Frequency Dispersive Effects in Large-signal FET Models," *in Proc. European GaAs and Related III-V Compounds Application Symposium, London*, pp. 45–48, Sept. 2001.

[75] F. Filicori, G. Vannini, A. Santarelli, A.M. Sanchez, A. Tazon, Y. Newport, "Empirical Modeling of Low-Frequency Dispersive Effects Due to Traps and Thermal Phenomena in III-V FETs," *IEEE Trans. Microwave Theory and Techn.*, vol. 43, no. 12, pp. 2972–2981, Dec. 1995.

[76] K. Jeon, Y. Kwon, S. Hong, "A Frequency Dispersion Model of GaAs MESFET for Large-Signal Applications," *IEEE Microwave and Guided Wave Letters*, vol. 7, no. 3, pp. 78–80, Mar. 1997.

[77] S. van Waasen, A. Umbach, U. Auer et. al., "27 GHz Bandwidth High-Speed Monolithic Integrated Optoelectronic Photoreceiver Consiting of a Waveguide Fed Photodiode and an InAlAs/InGaAs HFET Travelling Wave Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 9, pp. 1394–1401, Sept. 1997.

[78] J.H.K. Vuolevi, T. Rahkonen, J.P.A. Manninen, "Measurement for Characterizing Memory Effects in RF Power Amplifiers," *IEEE Trans. Microwave Theory and Techn.*, vol. 49, no. 8, pp. 1383–1389, Aug. 2001.

[79] H. Ku, M.D. McKinley, J.S. Kenney, "Quantifying Memory Effects in RF Power Amplifiers," *IEEE Trans. Microwave Theory and Techn.*, vol. 50, no. 12, pp. 2843–2849, Dec. 2002.

[80] W. Bösch, G. Gatti, "Measurement and Simulation of Memory Effects in Predistortion Linearizers," *IEEE Trans. on Microwave Theory and Techn.*, vol. 37, no. 12, pp. 1885–1890, Dec. 1989.

[81] H. Ku, J.S. Kenney, "Behavioral Modeling of Nonlinear RF Power Amplifiers Considering Memory Effects," *IEEE Trans. Microwave Theory and Techn.*, vol. 51, no. 12, pp. 2495–2504, Dec. 2003.

[82] T. Liu, S. Boumaiza, F.M. Ghannouchi, "Dynamic Behavioral Modeling of 3G Power Amplifiers using Real-Valued Time-Delay Neural Networks," *IEEE Trans. Microwave Theory and Techn.*, vol. 52, no. 3, pp. 1025–1033, Mar. 2004.

[83] P. Fellon, *PPH15 Foundry Design Manual, Small-Signal and Nonlinear Model in 3-Port Configuration*, United Monolithic Semiconductors, Nov. 1999.

[84] M. Fernandez-Barciela, P.J. Tasker, Y. Campos-Roca, M. Demmler, H. Massler, E. Sanchez, M.C. Curras-Francos, M. Schlechtweg, "A Simplified Broad-Band Large-Signal Nonquasi-Static Table-Based FET Model," *IEEE Trans. Microwave Theory and Techn.*, vol. 48, no. 3, pp. 395–405, Mar. 2000.

[85] M. Berroth, R. Bosch, "High-Frequency Equivalent Circuit of GaAs FET's for Large-Signal Applications," *IEEE Trans. Microwave Theory and Techn.*, vol. 39, no. 2, pp. 224–229, Feb. 1991.

[86] A. D. Snider, P. Winson, "A Generalized Dirichlet Principle for Smoothing Small-Signal Measurements," *IEEE Trans. on Microwave Theory and Techn.*, vol. 47, no. 5, pp. 636–639, May 1999.

[87] D. Schreurs, E. Vandamme, C. van Dinther, "Development and Verification of a Nonlinear Look-up Table Model for MOSFETs," *in Proc. 8th GaAs and Other Semiconductors Application Symposium, Paris*, Oct. 2000.

[88] D.E. Root, S. Fan, "Experimental Evaluation of Large-Signal Modeling Assumptions Based On Vector Analysis of Bias-Dependent S-Parameter Data from MESFETs and HEMTs," *in Proc. IEEE MTT-S Int. Microwave Symp., Albuquerque*, pp. 255–258, June 1992.

[89] G. Dambrine, A. Cappy, F. Heliodore, E. Playez, "A New Method for Determining the FET Small-Signal Equivalent Circuit," *IEEE Trans. Microwave Theory and Techn.*, vol. 36, no. 7, pp. 1151–1159, July 1988.

[90] P. L. Hower, N. G. Bechtel, "Current Saturation and Small-Signal Characteristics of GaAs Field-Effect Transistors," *IEEE Trans. on Electron Devices*, vol. 20, no. 3, pp. 213–220, March 1973.

[91] G. D. Vendelin, A. M. Pavio, U. L. Rohde, *Microwave Circuit Design Using Linear and Nonlinear Techniques. Chapter 1.1.3 Two-Port Network S Parameters.* John Wiley, New York, 1990.

[92] S. M. Sze, *Physics of Semiconductor Devices. Chapter 6.4.1* , 2nd ed., ser. 2. John Wiley, New York, 1981.

[93] W. R. Curtice, M. Ettenberg, "A nonlinear GaAsFET model for use in the design of output circuits for power amplifiers," *IEEE Trans. Microwave Theory and Techn.*, vol. 33, no. 12, pp. 1383–1394, Dec. 1985.

[94] I. Angelov, H. Zirath, N. Rorsman, "A New Empirical Nonlinear Model for HEMT and MESFET Devices," *IEEE Trans. Microwave Theory and Techn.*, vol. 40, no. 12, pp. 2258–2266, Dec. 1992.

[95] Y. Tajima, P. D. Miller, "Design of Broad-band Power GaAs FET Amplifiers," *IEEE Trans. Microwave Theory and Techn.*, vol. 32, no. 3, pp. 261–267, 1984.

[96] W.R. Curtice, "A MESFET Model for Use in the Design of GaAs Integrated Circuits," *IEEE Trans. Microwave Theory and Techn.*, vol. 28, no. 5, pp. 448–456, May 1980.

[97] V. I. Cojocaru, T. J. Brazil, "A Scalable General-Purpose Model for Microwave FET's Including DC/AC Dispersion Effects," *IEEE Trans. Microwave Theory and Techn.*, vol. 45, no. 12, pp. 2248–2255, Dec. 1997.

[98] B. OhAnnaidh, T.J. Brazil, "Intermodulation Distortion Characteristics of RF MOSFETs," *High Frequency Postgraduate Student Colloquium*, pp. 40–43, Sept. 2003.

[99] K. Levenberg, "A Method for the Solution of Certain Non-linear Problems in Least Squares," *Quaterly Journal of Applied Mathematics*, vol. 2, pp. 164–168, 1944.

[100] D. W. Marquardt, "An Algorithm for Least-Squares Estimation of Nonlinear Parameters," *Journal of the Society for Industrial and Applied Mathematics*, vol. 11, pp. 431–441, 1963.

[101] A. V. S. Narayanan, "Nonlinear Modelling of Non-quasi Static Effects in GaAs pHEMTs," Master's thesis, Department of Electron Devices and Circuits, University of Ulm, Apr. 2005.

[102] D.E. Root, "Measurement-Based Large-Signal Device Modeling: a Conceptual Overview," *presented at IEEE International Microwave Workshop on Nonlinear Modeling*, Apr. 1999.

[103] A. Siligaris, M. Vanmackelberg, G. Dambrine, N. Vellas, F. Danneville, "A new empirical non-linear model for SOI MOSFETs," *in Proc. 10th GaAs Symposium, European Microwave Week, Milano, Italy*, pp. 101–104, Oct. 2002.

[104] D.E. Root, "Nonlinear Charge Modeling for FET Large-Signal Simulation and Its Importance for IP3 and ACPR in Communication Circuits," *in Proc. 44th IEEE Midwest Symp. on Circuits and Systems MWSCAS*, vol. 2, pp. 768–772, August 2001.

[105] A.D. Snider, "Charge Conservation and the Transcapacitance Element: An Exposition," *IEEE Trans. on Education*, vol. 38, no. 4, pp. 376–379, Nov. 1995.

[106] H. Statz, P. Newman, I. Smith, R. Pucel, H. Haus, "GaAs FET device and circuit simulation in SPICE," *IEEE Trans. on Electron Devices*, vol. 34, pp. 160–169, Feb. 1987.

[107] S. D'Agostino, A. Betti-Berutto, "Physics-Based Expressions for the Nonlinear Capacitances of the MESFET Equivalent Circuit," *IEEE Trans. Microwave Theory and Techn.*, vol. 42, no. 3, pp. 403–406, March 1994.

[108] B. OhAnnaidh, T. J. Brazil, "A Globally-Continuous, Charge-Conservative, Non-linear Equivalent Circuit Model for RF MOSFETs," *in Proc. 11th GaAs Symposium, European Microwave Week, Munich*, pp. 65–68, Sept. 2003.

[109] M. Wren, T.J. Brazil, "Enhanced Prediction of pHEMT Nonlinear Distortion Using a Novel Charge Conservative Model," *in IEEE MTT-S Int. Microwave Symp., Fort Worth, Texas*, pp. 31–34, June 2004.

[110] E. Kohn, H. Schumacher, "University of Ulm, private conversation," 2004.

[111] P. Roblin, H. Rohdin, *High-speed heterostructure devices.* Cambridge University Press, 2002.

[112] T. J. Brazil, "FET simulator and parameter optimizer software fetfit2d," *University College Dublin, Ireland*, 2002.

[113] "TARGET Network of Excellence: Top Amplifier Research Groups in a European Group, official website: http://www.target-net.org."

[114] M. Kubovic, M. Kasu, I. Kallfass, M. Neuburger, A. Aleksov, G. Koley, M.G. Spencer, E. Kohn, "Microwave performance evaluation of diamond surface channel FETs," *Diamond and Related Materials*, vol. 13, pp. 802–807, 2004.

[115] A. Kubovic, A. Denisenko, W. Ebert, M. Kasu, I. Kallfass, E. Kohn, "Electronic surface barrier characteristics of H-terminated and surface conductive diamond," *Diamond and Related Materials*, vol. 13, pp. 755–760, 2004.

[116] M. Kasu, M. Kubovic, A. Aleksov, I. Kallfass, H. Schumacher, E. Kohn, N. Kobayashi, "Microwave performance of diamond MESFET," *Japan Society of Applied Physics*, vol. 73, no. 3, pp. 363–367, March 2004.

[117] Wolfgang Berger, "Characterisation and modelling of a 90nm RF-CMOS technology," Master's thesis, University of Ulm, Dept. of Electron Devices and Circuits, Oct. 2005.

[118] Agilent Technologies, *Advanced Design System Manual: Analog/RF User-defined Models*, May 2003.

[119] "Implementation of the COBRA FET model as a user-defined element in the HP EEsof Series IV circuit simulator LIBRA," *Internal Report, University College Dublin*, Mar. 1998.

[120] Agilent Technologies, *Advanced Design System Manual: Design Kit Development*, Dec. 2003.

[121] C. Zhang, "Impact of Frequency Dispersion Effects on MMIC Design," Master's thesis, Dept. of Eletron Devices and Circuits, University of Ulm, Apr. 2005.

[122] I. Kallfass, C. Schick, H. Schumacher, T. J. Brazil, "A Universal Large-Signal Model for Hetero Field-Effect Transistors," *in Proc. 12th GaAs Symposium, European Microwave Week, Amsterdam*, pp. 55–58, Oct. 2004.

[123] T. J. Brazil, I. Kallfass, B. OhAnnaidh, M. Wren, "Nonlinear Device Modelling of Si CMOS, SiGe HFET and GaAs pHEMT," *presented at IEEE MTT-S Int. Microwave Symp. Workshop, Fort Worth*, June 2004.

[124] I. Kallfass, F. Gruson, P. Abele, K. Michelakis, T. Hackbarth, K.-H. Hieber, J. Müller, H. Schumacher, "A SiGe HEMT Mixer IC with Low Conversion Loss," *in Proc. 11th GaAs Symposium, European Microwave Week, Munich, Germany*, pp. 513–516, Oct. 2003.

[125] V. D. Juncu, I. Kallfass, R. Sloan, J. V. Hatfield, "Behaviour of Logic Gates fabricated on Si/SiGe MODFET Technology," *Electronics Letters*, vol. 40, no. 12, pp. 772–774, June 2004.

[126] I. Kallfass, C. Zhang, J. Grünenpütt, C. Teyssandier, H. Schumacher, "Verification of a Frequency Dispersion Model in the Performance of a GaAs pHEMT Travelling-Wave MMIC," *in Proc. European Gallium Arsenide and other Compound Semiconductors Application Symposium, Paris*, pp. 381–384, Oct. 2005.

[127] P. Abele, M. Zeuner, I. Kallfass, J. Müller, H. Laban Hiwilepo, T. Hackbarth, D. Chrastina, H. von Känel, U. König and H. Schumacher, "32 GHz MMIC distributed amplifier based on N-channel SiGe MODFETs," *Electronics Letters*, vol. 39, no. 20, Oct. 2003.

[128] P. Abele, I. Kallfass, M. Zeuner, J. Müller, T. Hackbarth, D. Chrastina, H. von Känel, U. König ,and H. Schumacher, "32 GHz and 40 GHz bandwidth distributed amplifier

MMICs based on N-channel SiGe MODFETs," *in Proc. International Semiconductor Device Research Symposium, Washington D.C.*, pp. 55–56, Dec. 2003.

[129] L. Hiwilepo, "Design of a Wideband Amplifier using Si/SiGe Heterostructure Field-Effect Transistors," Master's thesis, Dept. of Eletron Devices and Circuits, University of Ulm, 2002.

[130] T. Hackbarth, "private conversation," Mar. 2003.

[131] H. Schumacher, *Monolithic Microwave ICs in High Speed Communication Systems, Lecture Script.* University of Ulm, 2005.

[132] H. Shigematsu, M. Sato, T. Hirose, Y. Watanabe, "A 54 GHz Distributed Amplifier With 6 V_{pp} Output for a 40 Gb/s LiNbO3 Modulator Driver," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 9, pp. 1100–1105, Sept. 2002.

[133] I. Kallfass, H. Schumacher, T. Purtova, A. Brokmeier, W. Ludwig, "One single travelling-wave MMIC for highly linear broadband mixers and variable gain amplifiers," *in IEEE MTT-S Int. Microwave Symp., Long Beach*, June 2005.

[134] Stephen A. Maas, *Microwave Mixers. Chapter 9: FET Mixers.* Artech House Inc., Norwood, MA, 1993.

[135] On San A. Tang, Colin S. Aitchison, "A Very Wide-Band Microwave MESFET Mixer using the Distributed Mixing Principle," *IEEE Trans. Microwave Theory and Techn.*, vol. 33, no. 12, pp. 1470–1478, Dec. 1985.

[136] D. Hollmann, R. Heilig, G. Baumann, "A Monolithic Broadband 10-50 GHz Distributed HEMT Mixer Including ActiVe LO-RF Combiner," *in Proc. Gallium Arsenide Integrated Circuits Symposium*, pp. 100–103, Oct. 1994.

[137] K.S. Ang, I.D. Robertson, "Multiple-FET Mixer Analysis with Applications to the Cascode Distributed Mixer," *in Proc. High-Frequency Postgraduate Colloquium, University of Leeds*, pp. 22–27, Sept. 1999.

[138] W. Ko, Y. Kwon, "A GaAs-based 3-40 GHz Distributed Mixer with Cascode FET Cells," *in Proc. IEEE Radio Frequency Integrated Circuits Symposium*, pp. 413–416, June 2004.

[139] K.-L. Deng, H. Wang, "A 3-33 PHEMT MMIC Distributed Drain Mixer," *in Proc. IEEE Radio Frequency Integrated Circuits Symposium*, pp. 151–154, June 2002.

[140] T. Purtova, "Design of a Wide-band Distributed Mixer in pHEMT Technology," Master's thesis, Dept. of Electron Devices and Circuits, University of Ulm, Nov. 2004.

List of Acronyms and Symbols

List of Acronyms

2DEG	Two Dimensional Electron Gas
2DHG	Two Dimensional Hole Gas
ACPR	Adjacent Channel Power Ratio
ADS	Agilent Advanced Design System
BW	Bandwidth
CAD	Computer Aided Design
CDMA	Code Division Multiple Access
CMOS	Complementary MOSFET
CPW	Coplanar Waveguide
DA	Distributed Amplifier
DLTS	Deep Level Transient Spectroscopy
DUT	Device under Test
ESM	Electronic Surveillance Measures
FOM	Figure of Merit
Gbps	Gigabits per second
GSG	Ground-Signal-Ground coplanar probe
GUI	Graphical User Interface
HB	Harmonic Balance
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HFET	Heterostructure Field Effect Transistor
IC	Integrated Circuit
IF	Intermediate Frequency
ISM	Industrial, Scientific, Medical frequency bands
IV	Current-Voltage Characteristics
LEPECVD	Low energy plasma enhanced chemical vapour deposition
LNA	Low-Noise Amplifier
LO	Local Oscillator

LTE	Low Temperature Epitaxy
MAG	Maximum Available Gain
MBE	Molecular Beam Epitaxy
mHEMT	Metamorphic High Electron Mobility Transistor
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave and mm-Wave Integrated Circuit
MODFET	Modulation Doped Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MS	Metal-Semiconductor
MPW	Multi Project Wafer
NoE	Network of Excellence
OEIC	Opto-Electronic Integrated Circuit
PA	Power Amplifier
PAE	Power Added Efficiency
PGSGP	Power-Ground-Signal-Ground-Power coplanar probe
pHEMT	Pseudomorphic High Electron Mobility Transistor
PIN	p-doped - intrinsic - n-doped diode structure
Q	Quiescent point/condition
R-C	Resistance - Capacitance Network
R-L	Resistance - Inductance Network
RF	Radio Frequency
SDD	Symbolically Defined Device (ADS specific)
SDH	Synchronous Digital Hierarchy
(Si)Ge	SiGe alloy with very high Ge content up to pure Ge
SiP	System in Package
SoC	System on Chip
SOI	Silicon-on-Insulator
SP	Scattering Parameters (and Simulation)
SPICE	Simulation Program with Integrated Circuit Emphasis
STM	Synchronous Transport Module
TIA	Transimpedance Amplifier
TR	Transient Simulation
TWA	Travelling-Wave Amplifier
U	Mason's Maximum Unilateral Gain
VGA	Variable Gain Amplifier
VS	Virtual Substrate

List of Symbols

α, β, γ δ, ζ, λ μ, ξ, η	COBRA model parameters
θ, κ, ι ψ, ν	Capacitance model parameters
β	wave propagation constant
μ_n, μ_p	Electron / hole mobility
τ	Drain current time delay
τ_gr	Group delay
$\tau_{\mathrm{x}i}$	Time constant of i-th dispersion source
$\Im\,()$	Imaginary part
$\Re\,()$	Real part
ΔE_C	Conduction band offset
ΔE_V	Valence band offset
C_{ij}	Capacitance between branch ij
C_{abc}	Capacitance model parameter named “abc”, unit [F]
C'	Capacitance per unit width
E	Error function in parameter optimisation
E_g	Bandgap energy
F	Frequency range
F_min	Minimum noise figure
f_max	Maximum frequency of oscillation
f_T	Transit(ion) frequency
$f_{\mathrm{x}i}$	Corner frequency of i-th dispersion source
G_ass	Associated gain
G_c	Mixer conversion gain
G_i	Intrinsic transistor voltage gain
G_V	Voltage gain
I_ds0	Static drain current
IIP_3	input-related third-order intercept point (two-tone measurement)
$\mathrm{IIP}_{3,1tone}$	input-related third-order intercept point (one-tone measurement)
k	Boltzmann constant
k	Thermal conductivity
L'	Inductance per unit length
NF_{50}	$50\,\Omega$ noise figure
OIP_3	output-related third-order intercept point (two-tone measurement)
$\mathrm{OIP}_{3,1tone}$	output-related third-order intercept point (one-tone measurement)

P_{ij}	Any twoport parameter (Z, Y, H, S...)
$P_{\mathrm{in,1dB}}$	Input-related 1 dB compression point
$P_{\mathrm{out,1dB}}$	Output-related 1 dB compression point
q	Elementary charge
Q_i	Charge at node i
Q	Quiescent point
T	Absolute temperature [K]
V_{bds}	Drain-source breakdown voltage
V_{gs0}, V_{ds0}	Static gate-source- and drain-source voltage
V_{ij}	Large-signal voltage between branch ij
v_{ij}	Small-signal voltage between branch ij
V_{k}	Knee voltage, linear-to-saturation transition
v_{sat}	(Electron) saturation velocity
V_{t}	Threshold voltage
V_{th}	Thermal voltage
V_{ti}	Model parameter named “ti”, unit [V]
w	Weights in error functions
Z	Characteristic transmission line impedance
Z_{L}	Load impedance

Appendix A

Dynamic Small-Signal FET Model Equations

In [85], the authors solve the internal transistor Y-matrix for eight small-signal model parameters. The gate leakage conductors G_{lgs} and G_{lgd} have to be extracted separately from DC gate current measurements. For reference, the resulting model extraction equations are listed here:

$$C_{\mathrm{gd}} = -\frac{\Im\{Y_{12}\}}{\omega}\left(1+\left(\frac{\Re\{Y_{12}\}+G_{\mathrm{lgd}}}{\Im\{Y_{12}\}}\right)^2\right) \tag{A.1}$$

$$R_{\mathrm{gdi}} = \frac{\Re\{Y_{12}\}+G_{\mathrm{lgd}}}{\omega C_{\mathrm{gd}}\Im\{Y_{12}\}} \tag{A.2}$$

$$C_{\mathrm{gs}} = \frac{\Im\{Y_{11}\}+\Im[Y_{12}\}}{\omega}\left(1+\frac{\left(\Re\{Y_{11}\}+\Re\{Y_{12}\}-G_{\mathrm{lgs}}\right)^2}{\left(\Im\{Y_{11}\}+\Im\{Y_{12}\}\right)^2}\right) \tag{A.3}$$

$$R_{\mathrm{gsi}} = \frac{\Re\{Y_{11}\}+\Re\{Y_{12}\}-G_{\mathrm{lgs}}}{\omega C_{\mathrm{gs}}\left(\Im\{Y_{11}\}+\Im\{Y_{12}\}\right)} \tag{A.4}$$

$$g_{\mathrm{m}} = \sqrt{\left(\left(\Re\{Y_{21}\}-\Re\{Y_{12}\}\right)^2+\left(\Im\{Y_{21}\}-\Im\{Y_{12}\}\right)^2\right)\left(1+\left(\omega C_{\mathrm{gs}}R_{\mathrm{gsi}}\right)^2\right)} \tag{A.5}$$

$$\tau = \frac{1}{\omega}\arcsin\left(\frac{\Im\{Y_{12}\}-\Im\{Y_{21}\}-\omega C_{\mathrm{gs}}R_{\mathrm{gsi}}\left(\Re\{Y_{21}\}-\Re\{Y_{12}\}\right)}{g_{\mathrm{m}}}\right) \tag{A.6}$$

$$C_{\mathrm{ds}} = \frac{\Im\{Y_{22}\}+\Im\{Y_{12}\}}{\omega} \tag{A.7}$$

$$g_{\mathrm{ds}} = \Re\{Y_{22}\}+\Re\{Y_{12}\} \tag{A.8}$$

Appendix B

Model Parameters, Equations and Derivatives

Schematic level parameters

Parameter	Unit	Default	Description
WU	μm	50	width of gate finger
N	1	2	number of gate fingers
VIA	1	0	use with source via?
TAMB	K	300	ambient temperature
FET	-	-	model parameter file
DISPMODEL	-	-1	dispersion model
CAPMODEL	-	1	nonlinear capacitance model
TR_TIME_DELAY	-	0	time delay in transient simulation

Model parameters

Parameter	Unit	Default	Description
WREF	μm	50	reference width of gate fingers
NREF	1	2	reference number of gate fingers
RG	Ω	1	Gate series resistance
RD	Ω	1	Drain series resistance
RS	Ω	1	Source series resistance
LG	nH	1e-3	Gate series inductance
LD	nH	1e-3	Drain series inductance
LS	nH	1e-3	Source series inductance
LVIA	nH	1e-3	Via inductance
ISGS	A	1e-12	Gate-source diode saturation current

Parameter	Unit	Default	Description
NID	1	1	diode ideality factor
ISGD	A	1e-12	Gate-drain diode saturation current
IBV	A	-1e-10	Diode reverse breakdown current
VBV	V	-8	Diode reverse breakdown voltage
NBV	1	5	Diode reverse breakdown ideality factor
IMAX	A	2e-3	Linearisation current in diode
GLGS	S	1e-9	Gate-source leakage conductance
GLGD	S	1e-9	Gate-drain leakage conductance
ALPHA	V^{-1}	5	I_{ds} current parameter: static
BETA	S	0.02	I_{ds} current parameter: static
GAMMA	1	0	I_{ds} current parameter: static
DELTA	V	0	I_{ds} current parameter: static
ZETA	V^{-1}	0	I_{ds} current parameter: static
LAMBDA	1	2	I_{ds} current parameter: static
MIU	V^{-2}	0	I_{ds} current parameter: static
XI	V^{-1}	0	I_{ds} current parameter: static
ETA	1	1	I_{ds} current parameter: static
VTO	V	-0.5	I_{ds} current parameter: static
PEFF	W^{-1}	0	self-heating parameter
TAU	ps	0.1	drain current delay (non quasi-static)
TAUi	ps	1e6	time constant of i-th dispersion source
ALPHAi	V^{-1}	5	I_{ds} current parameter: static
BETAi	S	0.02	i=1..3 I_{ds} current parameter: dynamic
GAMMAXi	1	0	i=1..3 I_{ds} current parameter: dynamic
DELTAXi	V	0	i=1..3 I_{ds} current parameter: dynamic
ZETAXi	V^{-1}	0	i=1..3 I_{ds} current parameter: dynamic
LAMBDAXi	1	2	i=1..3 I_{ds} current parameter: dynamic
MIUXi	V^{-2}	0	i=1..3 I_{ds} current parameter: dynamic
XIXi	V^{-1}	0	i=1..3 I_{ds} current parameter: dynamic
ETAXi	1	1	i=1..3 I_{ds} current parameter: dynamic
VTOXi	V	-0.5	i=1..3 I_{ds} current parameter: dynamic
CPGS	pF	10e-3	gate-source fringing capacitance
CPGD	pF	10e-3	gate-drain fringing capacitance
VBI	V	1	diode built-in voltage
M	1	0.5	diode capacitance ideality factor
FC	1	0.8	diode capacitance linearisation parameter
CGS1	pF	10e-3	gate-source diode capacitance
KAPPA	V^{-1}	2	gate-source capacitance parameter

Parameter	Unit	Default	Description
CGS2	pF	100e-3	gate-source capacitance parameter
VT2	V	-0.5	gate-source capacitance parameter
CGS3	pF	10e-3	capacitance parameter
NU	V^{-1}	4	capacitance parameter
VT3	V	-0.2	capacitance parameter
VGS4	V	0	capacitance parameter
CGD1	pF	10e-3	gate-drain diode capacitance
CGD2	pF	10e-3	gate-drain capacitance parameter
THETA	V	0.2	capacitance parameter
VT5	V	-0.5	gate-drain capacitance parameter

Scaling Model

Table B.2 shows the scaling parameters used in the definition of the scaling rules. Table B.3 lists the default scaling rules employed by the model, where primed parameters are the final, scaled model parameters. Additional scaling rules, if they can be provided by the manufacturer, could easily be incorporated into the model. For example, in case of the GaAs-based HEMT models, the scaling model of UMS has been implemented for all series inductance [83].

Gate Diodes

$$I_{\mathrm{g}}(V_{\mathrm{gs}}, V_{\mathrm{gd}}) = I_{\mathrm{gs}}(V_{\mathrm{gs}}) + I_{\mathrm{gd}}(V_{\mathrm{gd}}) + I_{\mathrm{bgs}}(V_{\mathrm{gs}}) + I_{\mathrm{bgd}}(V_{\mathrm{gd}}) + G_{\mathrm{lgs}}V_{\mathrm{gs}} + G_{\mathrm{lgd}}V_{\mathrm{gd}} \tag{B.1}$$

$$I_{\mathrm{gs}}(V_{\mathrm{gs}}) = I_{\mathrm{sgs}}\left(e^{\frac{V_{\mathrm{gs}}}{n_{\mathrm{id}}\cdot V_{\mathrm{th}}}} - 1\right) \tag{B.2}$$

$$I_{\mathrm{gd}}(V_{\mathrm{gd}}) = I_{\mathrm{sgd}}\left(e^{\frac{V_{\mathrm{gd}}}{n_{\mathrm{id}}\cdot V_{\mathrm{th}}}} - 1\right) \tag{B.3}$$

Linearisation

Parameter	Description
Wu	Unit gate finger width
N	Number of gate fingers
Wu_{ref}	Reference gate width
N_{ref}	Reference number of gate fingers
$wu = \frac{Wu}{Wu_{\mathrm{ref}}}$	Relative gate finger width
$n = \frac{N}{N_{\mathrm{ref}}}$	Ratio of actual to reference number of gate fingers

Table B.2: Scaling model parameters

Scaling rule	Description
$R_{\mathrm{g}}^{'} = \frac{wu}{n} \cdot R_{\mathrm{g}}$	Gate series resistance scales proportional to gate width, but inversely proportional to number of fingers
$R_{\mathrm{d}}^{'} = \frac{1}{n \cdot wu} \cdot R_{\mathrm{d}}$	Drain series resistance scales inversely proportional to total gate width
$R_{\mathrm{s}}^{'} = \frac{1}{n \cdot wu} \cdot R_{\mathrm{s}}$	Source series resistance scales inversely proportional to total gate width
$L_{\mathrm{g}}^{'} = wu \cdot L_{\mathrm{g}}$	Gate series inductance scales proportional to gate width
$L_{\mathrm{d}}^{'} = wu \cdot L_{\mathrm{d}}$	Drain series inductance scales proportional to gate width
$L_{\mathrm{s}}^{'} = n \cdot L_{\mathrm{s}}$	Source series inductance scales proportional to number of fingers
$I_{\mathrm{ds}}^{'} = wu \cdot n \cdot I_{\mathrm{ds}}$	Drain current scales proportional to total gate width
$I_{\mathrm{dsx}}^{'} = wu \cdot n \cdot I_{\mathrm{dsx}}$	Dispersion source current scales proportional to total gate width
$C_{\mathrm{gs}}^{'} = wu \cdot n \cdot C_{\mathrm{gs}}$	C_{gs} scales proportional to total gate width
$C_{\mathrm{gd}}^{'} = wu \cdot n \cdot C_{\mathrm{gd}}$	C_{gd} scales proportional to total gate width
$C_{\mathrm{ds}}^{'} = wu \cdot n \cdot C_{\mathrm{ds}}$	C_{ds} scales proportional to total gate width

Table B.3: Scaling rules

The parameter $I_{\max}$ is used to calculate the linearisation voltage

$$V_{\max} = n_{\mathrm{id}} V_{\mathrm{th}} \ln\left(\frac{I_{\max}}{I_{\mathrm{s}}} + 1\right) \tag{B.4}$$

where I_{s} is the saturation current of either the gate-drain- or the gate-source diode. The linear extension, as the name implies, uses the differential conductance $g_{\max}$ of the exponential expression as a constant beyond $I_{\max}$:

$$g_{\max} = \frac{I_{\mathrm{s}}}{n_{\mathrm{id}} V_{\mathrm{th}}} e^{\frac{V_{\max}}{n_{\mathrm{id}} V_{\mathrm{th}}}} \tag{B.5}$$

$$I_{\mathrm{gs}}|_{V_{\mathrm{gs}} > V_{\max}} = I_{\max} + (V_{\mathrm{gs}} - V_{\max}) g_{\max} + G_{\mathrm{lgs}} V_{\mathrm{gs}} \tag{B.6}$$

$$I_{\mathrm{gd}}|_{V_{\mathrm{gd}} > V_{\max}} = I_{\max} + (V_{\mathrm{gd}} - V_{\max}) g_{\max} + G_{\mathrm{lgd}} V_{\mathrm{gd}} \tag{B.7}$$

Breakdown current

$$I_{\mathrm{bgs}}(V_{\mathrm{gs}}) = I_{\mathrm{bv}} e^{\frac{-(V_{\mathrm{gs}} - V_{\mathrm{bv}})}{n_{\mathrm{bv}} V_{\mathrm{th}}}} \cdot \frac{V_{\mathrm{gs}}}{V_{\mathrm{bv}}} \tag{B.8}$$

$$I_{\mathrm{bgd}}(V_{\mathrm{gd}}) = I_{\mathrm{bv}} e^{\frac{-(V_{\mathrm{gd}} - V_{\mathrm{bv}})}{n_{\mathrm{bv}} V_{\mathrm{th}}}} \cdot \frac{V_{\mathrm{gd}}}{V_{\mathrm{bv}}} \tag{B.9}$$

For correct polarity, $I_{\mathrm{bv}} < 0$ and $V_{\mathrm{bv}} < 0$. The breakdown current is linearised for

$V_{\rm d} < V_{\rm bmax}$, with[1]

$$V_{\rm bmax} = V_{\rm bv} - n_{\rm bv} V_{\rm th} \ln \frac{-I_{\rm max}}{I_{\rm bv}} \tag{B.10}$$

where $V_{\rm d}$ is the diode voltage. The current is linearised with a constant conductance

$$g_{\rm bmax} = \frac{I_{\rm bv}}{V_{\rm bv}} e^{\frac{-(V_{\rm bmax}-V_{\rm bv})}{n_{\rm bv}V_{\rm th}}} \left(1 - \frac{V_{\rm bmax}}{n_{\rm bv}V_{\rm th}}\right) \tag{B.11}$$

and becomes

$$I_{\rm bgs}|_{V_{\rm gs}<V_{b\rm max}} = I_{\rm bgs}(V_{\rm bmax}) + g_{\rm bmax}(V_{\rm gs} - V_{\rm bmax}) \tag{B.12}$$

$$I_{\rm bgd}|_{V_{\rm gd}<V_{b\rm max}} = I_{\rm bgd}(V_{\rm bmax}) + g_{\rm bmax}(V_{\rm gd} - V_{\rm bmax}) \tag{B.13}$$

Diode conductance

$$g_{\rm dgs} = \frac{\partial I_{\rm gs}}{\partial V_{\rm gs}} = \frac{\partial I_{\rm gs}}{\partial V_{\rm gs}} + G_{\rm lgs} + \frac{\partial I_{\rm bgs}}{\partial V_{\rm gs}} \tag{B.14}$$

$$g_{\rm dgd} = \frac{\partial I_{\rm gd}}{\partial V_{\rm gd}} = \frac{\partial I_{\rm gd}}{\partial V_{\rm gd}} + G_{\rm lgd} + \frac{\partial I_{\rm bgd}}{\partial V_{\rm gd}} \tag{B.15}$$

$$\frac{\partial I_{\rm gs}}{\partial V_{\rm gs}} = \begin{cases} \frac{I_{\rm sgs}}{n_{\rm id}V_{\rm th}} e^{\frac{V_{\rm gs}}{n_{\rm id}V_{\rm th}}} & V_{\rm gs} < V_{\rm max} \\ g_{\rm max} & V_{\rm gs} > V_{\rm max} \end{cases} \tag{B.16}$$

$$\frac{\partial I_{\rm bgs}}{\partial V_{\rm gs}} = \begin{cases} \frac{I_{\rm bv}}{V_{\rm bv}} e^{\frac{-(V_{\rm gs}-V_{\rm bv})}{n_{\rm bv}V_{\rm th}}} \left(1 - \frac{V_{\rm gs}}{n_{\rm bv}V_{\rm th}}\right) & V_{\rm gs} > V_{\rm bmax} \\ g_{\rm bmax} & V_{\rm gs} < V_{\rm bmax} \end{cases} \tag{B.17}$$

$$\frac{\partial I_{\rm gd}}{\partial V_{\rm gd}} = \begin{cases} \frac{I_{\rm sgd}}{n_{\rm id}V_{\rm th}} e^{\frac{V_{\rm gd}}{n_{\rm id}V_{\rm th}}} & V_{\rm gd} < V_{\rm max} \\ g_{\rm max} & V_{\rm gd} > V_{\rm max} \end{cases} \tag{B.18}$$

$$\frac{\partial I_{\rm bgd}}{\partial V_{\rm gd}} = \begin{cases} \frac{I_{\rm bv}}{V_{\rm bv}} e^{\frac{-(V_{\rm gd}-V_{\rm bv})}{n_{\rm bv}V_{\rm th}}} \left(1 - \frac{V_{\rm gd}}{n_{\rm bv}V_{\rm th}}\right) & V_{\rm gd} > V_{\rm bmax} \\ g_{\rm bmax} & V_{\rm gd} < V_{\rm bmax} \end{cases} \tag{B.19}$$

Drain-Source Current

$$I_{\rm ds} = \beta \cdot A_1 \cdot A_2 \tag{B.20}$$

$$A_1 = V_{\rm eff}^{\rm exp} \tag{B.21}$$

$$A_2 = \tanh\left(\alpha V_{\rm ds}\left(1 + \zeta V_{\rm eff}\right)\right) \tag{B.22}$$

$$\exp = \frac{\lambda}{1 + \mu V_{\rm ds}^2 + \xi V_{\rm eff2}^{\eta}} \tag{B.23}$$

$$V_{\rm eff} = \frac{1}{2}\left(V_{\rm gs} - V_{\rm t1} + \sqrt{\left(V_{\rm gs} - V_{\rm t1}\right)^2 + \delta^2}\right) \tag{B.24}$$

[1]Note: the calculated $V_{\rm bmax}$ does not exactly correspond to $I_{\rm max}$, in fact, the current at $V_{\rm bmax}$ will slightly exceed $I_{\rm max}$. For simplicity, however, it is calculated like for a simple exponential current expression. In calculating $g_{\rm bmax}$, one therefore needs to use $I_{\rm bgs}(V_{\rm bmax})$ and $I_{\rm bgd}(V_{\rm bmax})$ instead of $I_{\rm max}$ to correct for this.

$$V_{\mathrm{t1}} = \left(1+\beta^2\right) V_{\mathrm{to}} - \gamma V_{\mathrm{ds}} \tag{B.25}$$

$$V_{\mathrm{eff2}} = \frac{1}{2}\left(V_{\mathrm{gs}} - V_{\mathrm{t2}} + \sqrt{\left(V_{\mathrm{gs}} - V_{\mathrm{t2}}\right)^2 + \delta^2}\right) \tag{B.26}$$

$$V_{\mathrm{t2}} = \left(1+\beta^2\right) V_{\mathrm{to}} \tag{B.27}$$

Transconductance

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{gs}}} = \beta\left(\frac{\partial A_1}{\partial V_{\mathrm{gs}}} A_2 + A_1 \frac{\partial A_2}{\partial V_{\mathrm{gs}}}\right) \tag{B.28}$$

$$\frac{\partial A_1}{\partial V_{\mathrm{gs}}} = \frac{\partial}{\partial V_{\mathrm{gs}}} e^{\ln V_{\mathrm{eff}} \cdot \exp} = e^{\ln V_{\mathrm{eff}} \cdot \exp}\left(\frac{\partial \exp}{\partial V_{\mathrm{gs}}} \ln V_{\mathrm{eff}} + \exp \frac{\partial \ln V_{\mathrm{eff}}}{\partial V_{\mathrm{gs}}}\right) \tag{B.29}$$

$$\frac{\partial \exp}{\partial V_{\mathrm{gs}}} = \frac{-\lambda}{\left(1 + \mu V_{\mathrm{ds}}^2 + \xi V_{\mathrm{eff2}}^{\eta}\right)^2} \cdot \eta \xi V_{\mathrm{eff2}}^{\eta-1} \frac{\partial V_{\mathrm{eff2}}}{\partial V_{\mathrm{gs}}} \tag{B.30}$$

$$\frac{\partial \ln V_{\mathrm{eff}}}{\partial V_{\mathrm{gs}}} = \frac{1}{V_{\mathrm{eff}}} \frac{\partial V_{\mathrm{eff}}}{\partial V_{\mathrm{gs}}} \tag{B.31}$$

$$\frac{\partial V_{\mathrm{eff}}}{\partial V_{\mathrm{gs}}} = \frac{1}{2}\left(1 + \frac{V_{\mathrm{gs}} - V_{\mathrm{t1}}}{\sqrt{(V_{\mathrm{gs}} - V_{\mathrm{t1}})^2 + \delta^2}}\right) \tag{B.32}$$

$$\frac{\partial V_{\mathrm{eff2}}}{\partial V_{\mathrm{gs}}} = \frac{1}{2}\left(1 + \frac{V_{\mathrm{gs}} - V_{\mathrm{t2}}}{\sqrt{(V_{\mathrm{gs}} - V_{\mathrm{t2}})^2 + \delta^2}}\right) \tag{B.33}$$

$$\frac{\partial A_2}{\partial V_{\mathrm{gs}}} = \frac{1}{\cosh^2\left(\alpha V_{\mathrm{ds}}(1 + \zeta V_{\mathrm{eff}})\right)} \alpha V_{\mathrm{ds}} \zeta \frac{\partial V_{\mathrm{eff}}}{\partial V_{\mathrm{gs}}} \tag{B.34}$$

Output Conductance

$$g_{\mathrm{ds}} = \frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{ds}}} = \beta\left(\frac{\partial A_1}{\partial V_{\mathrm{ds}}} A_2 + A_1 \frac{\partial A_2}{\partial V_{\mathrm{ds}}}\right) \tag{B.35}$$

$$\frac{\partial A_1}{\partial V_{\mathrm{ds}}} = \frac{\partial}{\partial V_{\mathrm{ds}}} e^{\ln V_{\mathrm{eff}} \cdot \exp} = e^{\ln V_{\mathrm{eff}} \cdot \exp}\left(\frac{\partial \exp}{\partial V_{\mathrm{ds}}} \ln V_{\mathrm{eff}} + \exp \frac{\partial \ln V_{\mathrm{eff}}}{\partial V_{\mathrm{ds}}}\right) \tag{B.36}$$

$$\frac{\partial \exp}{\partial V_{\mathrm{ds}}} = \frac{-\lambda}{\left(1 + \mu V_{\mathrm{ds}}^2 + \xi V_{\mathrm{eff2}}^{\eta}\right)^2} \cdot 2\mu V_{\mathrm{ds}} \tag{B.37}$$

$$\frac{\partial \ln V_{\mathrm{eff}}}{\partial V_{\mathrm{ds}}} = \frac{1}{V_{\mathrm{eff}}} \frac{\partial V_{\mathrm{eff}}}{\partial V_{\mathrm{ds}}} \tag{B.38}$$

$$\frac{\partial V_{\mathrm{eff}}}{\partial V_{\mathrm{ds}}} = \frac{1}{2}\left(-\frac{\partial V_{\mathrm{t1}}}{\partial V_{\mathrm{ds}}} + \frac{V_{\mathrm{gs}} - V_{\mathrm{t1}}}{\sqrt{(V_{\mathrm{gs}} - V_{\mathrm{t1}})^2 + \delta^2}}(-1)\frac{\partial V_{\mathrm{t1}}}{\partial V_{\mathrm{ds}}}\right) \tag{B.39}$$

$$\frac{\partial V_{\mathrm{t1}}}{\partial V_{\mathrm{ds}}} = -\gamma \tag{B.40}$$

$$\frac{\partial A_2}{\partial V_{\mathrm{ds}}} = \frac{1}{\cosh^2\left(\alpha V_{\mathrm{ds}}(1+\zeta V_{\mathrm{eff}})\right)}\left(\alpha(1+\zeta V_{\mathrm{eff}}) + \alpha V_{\mathrm{ds}}\zeta\frac{\partial V_{\mathrm{eff}}}{\partial V_{\mathrm{ds}}}\right) \tag{B.41}$$

Dispersion Sources

$$I_{\mathrm{dsac}} = \beta_{\mathrm{x}} \cdot A_1 \cdot A_2 \tag{B.42}$$

$$A_1 = V_{\mathrm{eff}}^{\mathrm{exp}} \tag{B.43}$$

$$A_2 = \tanh\left(\alpha_{\mathrm{x}} V_{\mathrm{ds}}\left(1+\zeta_{\mathrm{x}} V_{\mathrm{eff}}\right)\right) \tag{B.44}$$

$$\mathrm{exp} = \frac{\lambda_{\mathrm{x}}}{1+\mu_{\mathrm{x}} V_{\mathrm{ds}}^2 + \xi_{\mathrm{x}} V_{\mathrm{eff2}}^{\eta_{\mathrm{x}}}} \tag{B.45}$$

$$V_{\mathrm{eff}} = \frac{1}{2}\left(V_{\mathrm{gs}} - V_{\mathrm{t1}} + \sqrt{\left(V_{\mathrm{gs}} - V_{\mathrm{t1}}\right)^2 + \delta_{\mathrm{x}}^2}\right) \tag{B.46}$$

$$V_{\mathrm{t1}} = \left(1+\beta_{\mathrm{x}}^2\right) V_{\mathrm{to}} - \gamma_{\mathrm{x}} V_{\mathrm{ds}} \tag{B.47}$$

$$V_{\mathrm{eff2}} = \frac{1}{2}\left(V_{\mathrm{gs}} - V_{\mathrm{t2}} + \sqrt{\left(V_{\mathrm{gs}} - V_{\mathrm{t2}}\right)^2 + \delta_{\mathrm{x}}^2}\right) \tag{B.48}$$

$$V_{\mathrm{t2}} = \left(1+\beta_{\mathrm{x}}^2\right) V_{\mathrm{to}} \tag{B.49}$$

Dynamic transconductance and output conductance result accordingly (compare static current).

Gate Capacitance

$$\begin{aligned} C_{\mathrm{gs}}(V_{\mathrm{gs}}, V_{\mathrm{gd}}) \;=\; & C_{\mathrm{pgs}} + C_{\mathrm{d}}(V_{\mathrm{gs}}) \\ & + C_{\mathrm{gs2}}(1+\tanh(\kappa(V_{\mathrm{gs}} - V_{\mathrm{t2}}))) \\ & + C_{\mathrm{S}}(V_{\mathrm{gs}}) \cdot (1+\tanh\left(\iota\left[V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right]\right)) \\ & - \frac{\partial C_{\mathrm{S}}(V_{\mathrm{gs}})}{\partial V_{\mathrm{gs}}} \cdot \left(V_{\mathrm{gd}} - \frac{1}{\iota}\ln\left(\cosh\left[\iota\left(V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right)\right]\right)\right) \end{aligned} \tag{B.50}$$

$$\begin{aligned} C_{\mathrm{gd}}(V_{\mathrm{gs}}, V_{\mathrm{gd}}) \;=\; & C_{\mathrm{pgd}} + C_{\mathrm{d}}(V_{\mathrm{gd}}) \\ & + C_{\mathrm{gd2}}(1+\tanh(\kappa(V_{\mathrm{gd}} - V_{\mathrm{t5}}))) \\ & - C_{\mathrm{S}}(V_{\mathrm{gs}}) \cdot (1+\tanh\left(\iota\left[V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right]\right)) \end{aligned} \tag{B.51}$$

$$C_{\mathrm{d}}(V_{\mathrm{d}}) = \begin{cases} \frac{C_{\mathrm{gs1}}}{(1-\frac{V_{\mathrm{d}}}{V_{\mathrm{bi}}})^m} & V_{\mathrm{d}} < V_{\mathrm{bi}} \cdot f_{\mathrm{c}} \\ \frac{C_{\mathrm{gs1}}}{(1-f_{\mathrm{c}})^m} + \frac{mC_{\mathrm{gs1}}}{V_{\mathrm{bi}}(1-f_{\mathrm{c}})^{m+1}} \left(V_{\mathrm{d}} - f_{\mathrm{c}} V_{\mathrm{bi}}\right) & V_{\mathrm{d}} \geq V_{\mathrm{bi}} \cdot f_{\mathrm{c}} \end{cases} \tag{B.52}$$

$$C_{\mathrm{S}}(V_{\mathrm{gs}}) = C_3 \cdot V_{\mathrm{eff}}^{\psi} \tag{B.53}$$

$$V_{\mathrm{eff}} = \frac{1}{2}\left(V_{\mathrm{gs}} - V_{\mathrm{t3}} + \sqrt{\left(V_{\mathrm{gs}} - V_{\mathrm{t3}}\right)^2 + \theta^2}\right) \tag{B.54}$$

Derivatives

$$\begin{aligned} \tfrac{\partial}{\partial V_{\mathrm{gs}}} C_{\mathrm{gs}}(V_{\mathrm{gs}}, V_{\mathrm{gd}}) \;=\; & \tfrac{\partial C_{\mathrm{d}}(V_{\mathrm{gs}})}{\partial V_{\mathrm{gs}}} \\ & + C_{\mathrm{gs2}} \cdot \kappa \cdot \mathrm{sech}^2(\kappa(V_{\mathrm{gs}} - V_{\mathrm{t2}}) \\ & + \tfrac{\partial C_{\mathrm{S}}(V_{\mathrm{gs}})}{\partial V_{\mathrm{gs}}} \cdot (1 + \tanh\left(\iota\left[V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right]\right)) \\ & + C_{\mathrm{S}}(V_{\mathrm{gs}}) \cdot \iota \cdot \mathrm{sech}^2\left(\iota\left[V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right]\right) \\ & - \tfrac{\partial^2 C_{\mathrm{S}}(V_{\mathrm{gs}})}{\partial^2 V_{\mathrm{gs}}} \cdot \left(V_{\mathrm{gd}} - \tfrac{1}{\iota} \ln\left(\cosh\left[\iota\left(V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right)\right]\right)\right) \\ & + \tfrac{\partial C_{\mathrm{S}}(V_{\mathrm{gs}})}{\partial V_{\mathrm{gs}}} \tanh\left[\iota\left(V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right)\right] \end{aligned} \tag{B.55}$$

$$\begin{aligned} \frac{\partial}{\partial V_{\mathrm{gd}}} C_{\mathrm{gs}}(V_{\mathrm{gs}}, V_{\mathrm{gd}}) \;=\; & -C_{\mathrm{S}}(V_{\mathrm{gs}}) \cdot \iota \cdot \mathrm{sech}^2\left(\iota\left[V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right]\right) \\ & - \frac{\partial C_{\mathrm{S}}(V_{\mathrm{gs}})}{\partial V_{\mathrm{gs}}} \cdot (1 + \tanh\left[\iota\left(V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right)\right]) \end{aligned} \tag{B.56}$$

$$\begin{aligned} \frac{\partial}{\partial V_{\mathrm{gs}}} C_{\mathrm{gd}}(V_{\mathrm{gs}}, V_{\mathrm{gd}}) \;=\; & -C_{\mathrm{S}}(V_{\mathrm{gs}}) \cdot \iota \cdot \mathrm{sech}^2\left(\iota\left[V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right]\right) \\ & - \frac{\partial C_{\mathrm{S}}(V_{\mathrm{gs}})}{\partial V_{\mathrm{gs}}} \cdot (1 + \tanh\left[\iota\left(V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right)\right]) \end{aligned} \tag{B.57}$$

$$\begin{aligned} \frac{\partial}{\partial V_{\mathrm{gd}}} C_{\mathrm{gd}}(V_{\mathrm{gs}}, V_{\mathrm{gd}}) \;=\; & \frac{\partial C_{\mathrm{d}}(V_{\mathrm{gd}})}{\partial V_{\mathrm{gd}}} \\ & + C_{\mathrm{gd2}} \kappa \cdot \mathrm{sech}^2(\kappa(V_{\mathrm{gd}} - V_{\mathrm{t5}}) \\ & + C_{\mathrm{S}}(V_{\mathrm{gs}}) \cdot \iota \cdot \mathrm{sech}^2\left(\iota\left[V_{\mathrm{gs}} - V_{\mathrm{gd}} - V_{\mathrm{t4}}\right]\right) \end{aligned} \tag{B.58}$$

$$\frac{\partial}{\partial V_{\mathrm{d}}} C_{\mathrm{d}}(V_{\mathrm{d}}) = \begin{cases} \frac{C_{\mathrm{gs1}} m}{V_{\mathrm{bi}}(1-\frac{V_{\mathrm{d}}}{V_{\mathrm{bi}}})^{m+1}} & V_{\mathrm{d}} < V_{\mathrm{bi}} \cdot f_{\mathrm{c}} \\ \frac{C_{\mathrm{gs1}} m}{V_{\mathrm{bi}}(1-f_{\mathrm{c}})^{m+1}} & V_{\mathrm{d}} \geq V_{\mathrm{bi}} \cdot f_{\mathrm{c}} \end{cases} \tag{B.59}$$

$$\frac{\partial C_{\mathrm{S}}(V_{\mathrm{gs}})}{\partial V_{\mathrm{gs}}} = C_3 \cdot \psi V_{\mathrm{eff}}^{\psi-1} \cdot \frac{\partial V_{\mathrm{eff}}}{\partial V_{\mathrm{gs}}} \tag{B.60}$$

$$\frac{\partial^2 C_{\mathrm{S}}(V_{\mathrm{gs}})}{\partial^2 V_{\mathrm{gs}}} = C_3 \psi \left((\psi - 1) V_{\mathrm{eff}}^{\psi-2} \cdot \frac{\partial V_{\mathrm{eff}}}{\partial V_{\mathrm{gs}}} \cdot \frac{\partial V_{\mathrm{eff}}}{\partial V_{\mathrm{gs}}} + V_{\mathrm{eff}}^{\psi-1} \cdot \frac{\partial^2 V_{\mathrm{eff}}}{\partial^2 V_{\mathrm{gs}}} \right)$$

$$\frac{\partial V_{\mathrm{eff}}}{\partial V_{\mathrm{gs}}} = \frac{1}{2} \left(1 + \frac{V_{\mathrm{gs}} - V_{\mathrm{t3}}}{\sqrt{(V_{\mathrm{gs}} - V_{\mathrm{t3}})^2 + \theta^2}} \right) \tag{B.61}$$

$$\frac{\partial^2 V_{\mathrm{eff}}}{\partial^2 V_{\mathrm{gs}}} = \frac{1}{2} \left(\frac{\theta^2}{((V_{\mathrm{gs}} - V_{\mathrm{t3}})^2 + \theta^2)^{\frac{3}{2}}} \right) \tag{B.62}$$

Appendix C

Detailed Model Parameters and Verification

This chapter contains a complete listing of

- model parameter values,
- graphs of measured and modelled IV characteristics and
- linear (S-parameters) and nonlinear (one- & two-tone power) verification data,

for the strained-Si/SiGe mHEMT, InP pHEMT, low-noise- and power GaAs pHEMT.

C.1 Strained-Si/SiGe mHEMT

Parameter	Value
R_{G}	3.0 Ω
R_{D}	4.95 Ω
R_{S}	4.55 Ω
L_{G}	11.5 pH
L_{D}	12 pH
L_{S}	0.15 pH
C_{DS}	20 fF
R_{GSI}	7 Ω
R_{GDI}	8 Ω
τ	0.5 ps

Table C.1: Linear model parameters of a 2x50 μm strained-Si/SiGe mHEMT.

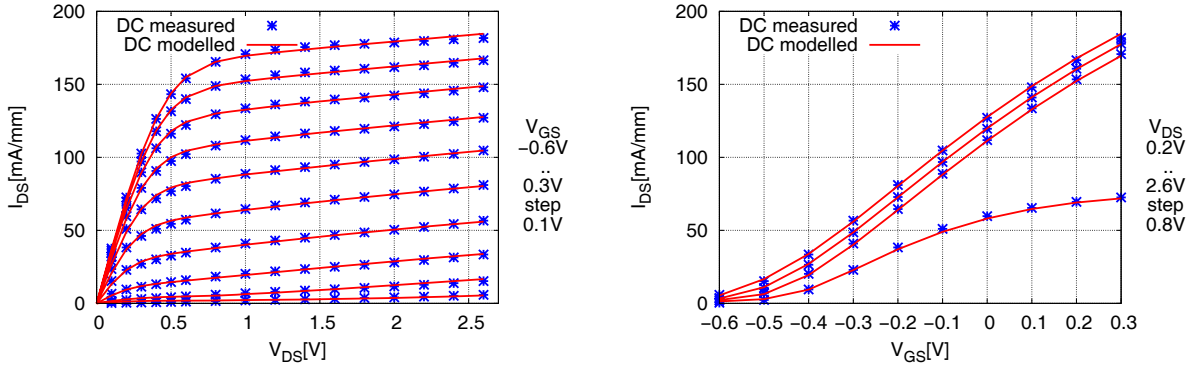

Figure C.1: Static drain current in a 2x50 μm strained-Si/SiGe mHEMT device. Measured values (points) and nonlinear model (line). Output characteristics (left) and transfer characteristics (right).

Parameter	Value
β	2.1347e-002
V_{to}	-4.2456e-001
λ	1.0875e+000
α	5.4861e+000
μ	-1.2231e-002
γ	6.8666e-002
δ	8.6909e-002
ξ	1.0746e+000
ζ	-4.3891e-001
η	1.0454e+000
π_{eff}^{-1}	1e-3

Table C.2: Nonlinear drain current model parameters of a 2x50 μm strained-Si/SiGe mHEMT.

Parameter	Value
n_{id}	1.8856e+000
I_{sgs}	6.2928e-009
I_{sgd}	1.7011e-011
G_{lgs}	1e-8
G_{lgd}	1e-8
f_c	0.8
I_{max}	20e-3
bv	-6e+000
I_{bv}	-9.8066e-002
n_{bv}	1.8551e+001

Table C.3: Nonlinear gate current model parameters of a 2x50 μm strained-Si/SiGe mHEMT.

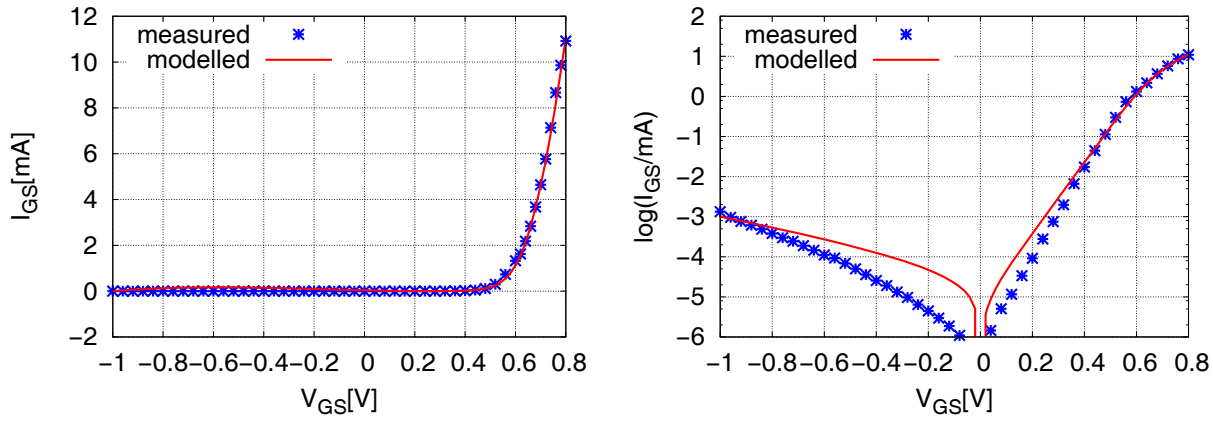

Figure C.2: Static gate current in a 2x50 μm strained-Si/SiGe mHEMT device. Measured values (points) and nonlinear model (line) on a linear scale (left) and in logarithmic form (right).

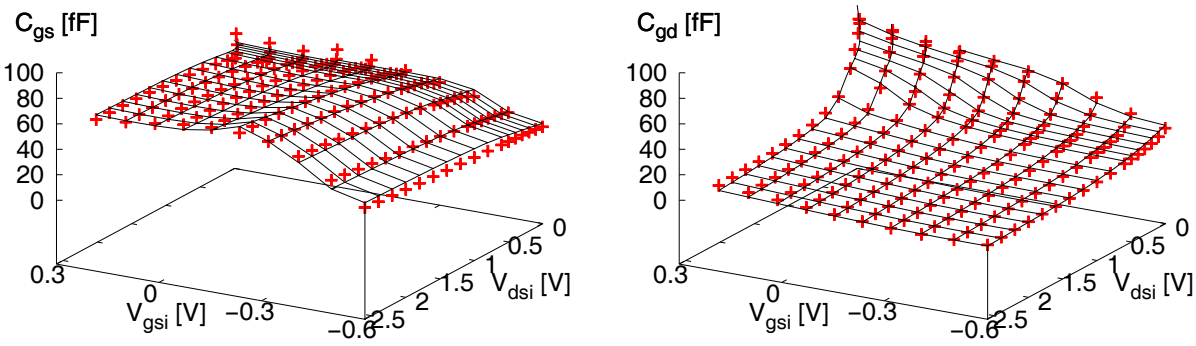

Figure C.3: Nonlinear gate capacitance C_{gs} (left) and C_{gd} (right) in a 2x50 μm strained-Si/SiGe mHEMT device. Measured values (points) and nonlinear model (line).

Parameter	C_{pgs}	C_{pgd}	C_{gs1}	C_{gs2}	C_{gs3}	C_{gd1}	C_{gd2}
Value / fF	21.8	7.0	2.3	20.0	8.5	35.9	20.0

Parameter	V_{bi}	V_{t2}	V_{t3}	V_{t4}	V_{t5}
Value / V	0.5	-0.46	-0.26	0.2	-0.35

Parameter	m	κ	ν	ι	ψ	θ
Value	0.5	14.0	9.93	1.75	0.057	0.081

Table C.4: Nonlinear capacitance model parameters of a 2x50 μm strained-Si/SiGe mHEMT.

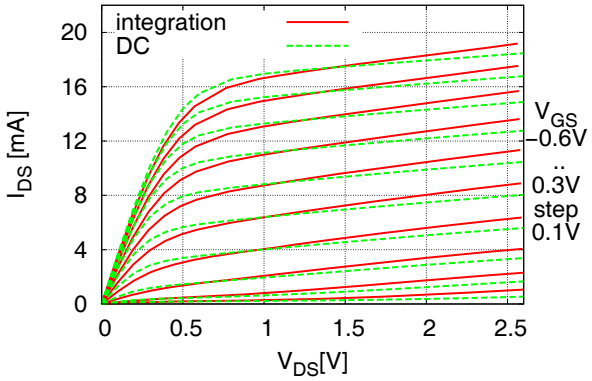

Figure C.4: Dynamic drain current in a 2x50 μm strained-Si/SiGe mHEMT device. I_{dsac1} (dynamic $g_{\mathrm{m}}/g_{\mathrm{ds}}$ integration, quiescent point:$V_{\mathrm{gs}} = -0.5\,\mathrm{V}$, $V_{\mathrm{ds}} = 1.2\,\mathrm{V}$)

Parameter	I_{ds}	I_{dsac1}
β	2.1347e-002	2.0812e-002
V_{to}	-4.2456e-001	-4.0546e-001
λ	1.0875e+000	1.2547e+000
α	5.4861e+000	4.0366e+000
μ	-1.2231e-002	-2.5258e-002
γ	6.8666e-002	1.1499e-001
δ	8.6909e-002	1.1815e-001
ξ	1.0746e+000	1.2160e+000
ζ	-4.3891e-001	-2.4345e-001
η	1.0454e+000	8.2328e-001
π_{eff}^{-1}	1e-3	1e-3

Table C.5: Dispersion drain current model parameters of a 2x50 μm strained-Si/SiGe mHEMT.

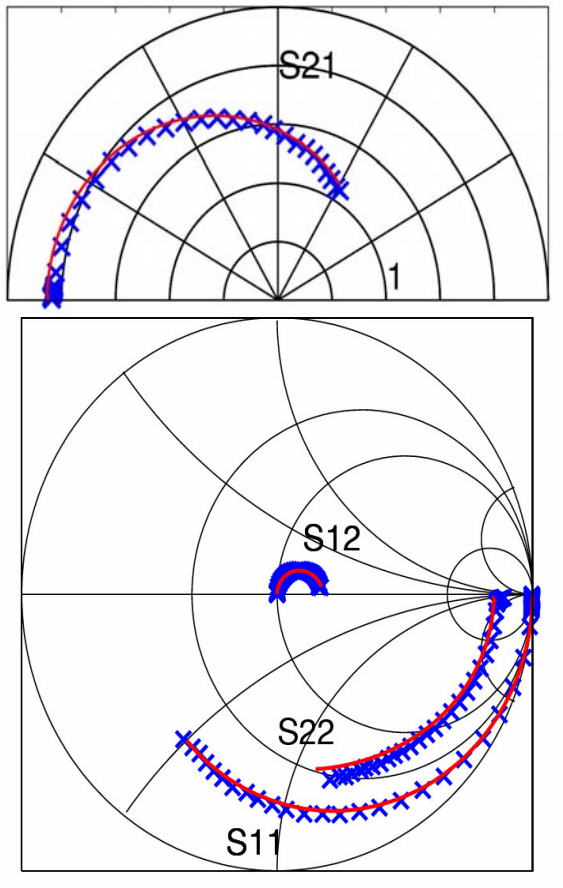

Figure C.5: 50MHz-50GHz S-parameters of a 2x50 μm strained-Si/SiGe device, biased at $V_{\mathrm{gs}} = -0.3\,\mathrm{V}$, $V_{\mathrm{ds}} = 1.2\,\mathrm{V}$ ($\tilde{}g_{\mathrm{m,max}}$). Measurement (dots) and model (lines).

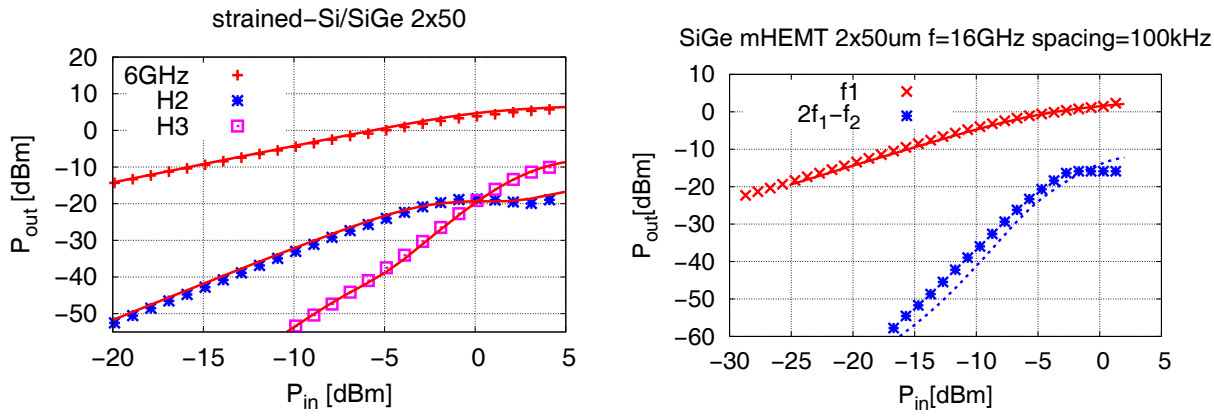

Figure C.6: One-tone power (left, 6GHz fundamental) and two-tone power (right, 16GHz fundamental) measurement of a 2x50 μm strained-Si/SiGe device, biased at $V_{\mathrm{gs}} = -0.3\,\mathrm{V}$, $V_{\mathrm{ds}} = 1.5\,\mathrm{V}$. Measurement (dots) and model (lines).

Parameter	Value
R_G	1.7 Ω
R_D	4.73 Ω
R_S	4.33 Ω
L_G	22.6 pH
L_D	22.0 pH
L_S	1.9 pH
C_{DS}	50 fF
R_{GSI}	2 Ω
R_{GDI}	10 Ω
τ	1 ps

Table C.6: Linear model parameters of the 2x50 μm PH15 GaAs pHEMT.

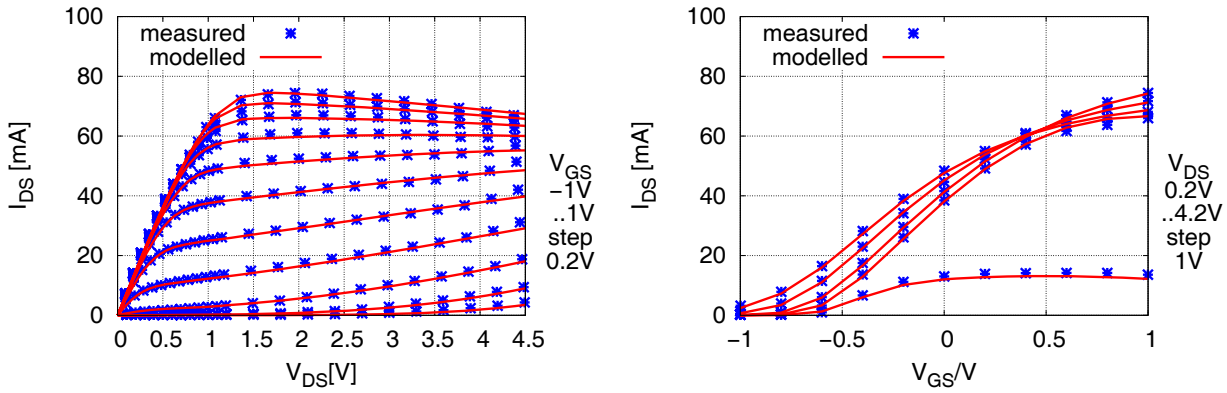

Figure C.7: Static drain current in the 2x50 μm PH15 GaAs pHEMT device. Measured values (points) and nonlinear model (line). Output characteristics (left) and transfer characteristics (right).

C.2 Low-noise AlGaAs/GaAs pHEMT

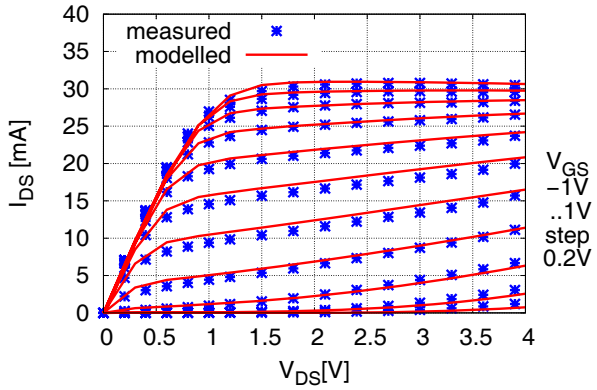

Figure C.8: Application of the modified COBRA model to a 2x20 μm device using linear current scaling of the 2x50 μm parameter set.

Parameter	Value
β	6.7212e-002
V_{to}	-6.3586e-001
λ	4.3651e+000
α	5.1601e+000
μ	5.7432e-002
γ	9.5149e-002
δ	2.7124e-001
ξ	6.1011e+000
ζ	-3.2757e-001
η	8.8337e-001
π_{eff}^{-1}	8.1050e-001

Table C.7: Nonlinear drain current model parameters of the 2x50 μm PH15 GaAs pHEMT.

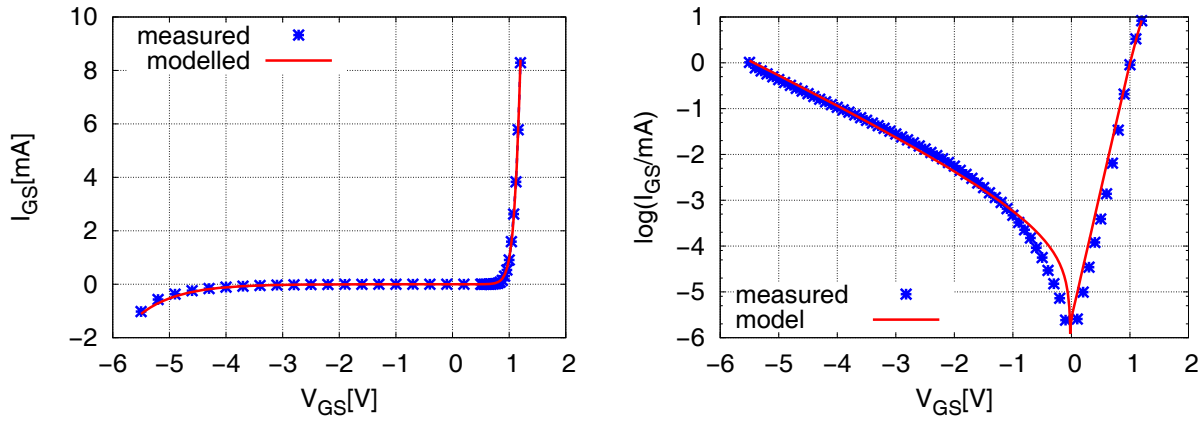

Figure C.9: Static gate current in a 2x50 μm PH15 GaAs pHEMT device. Measured values (points) and nonlinear model (line) on a linear scale (left) and in logarithmic form (right).

Parameter	Value
n_{id}	3.0075e+000
I_{sgs}	3.2016e-009
I_{sgd}	3.9820e-009
G_{lgs}	1e-9
G_{lgd}	1e-9
f_c	0.8
I_{max}	20e-3
bv	-4.2592e+000
I_{bv}	-8.6033e-005
n_{bv}	2.9678e+001

Table C.8: Nonlinear gate current model parameters of a 2x50 μm PH15 GaAs pHEMT.

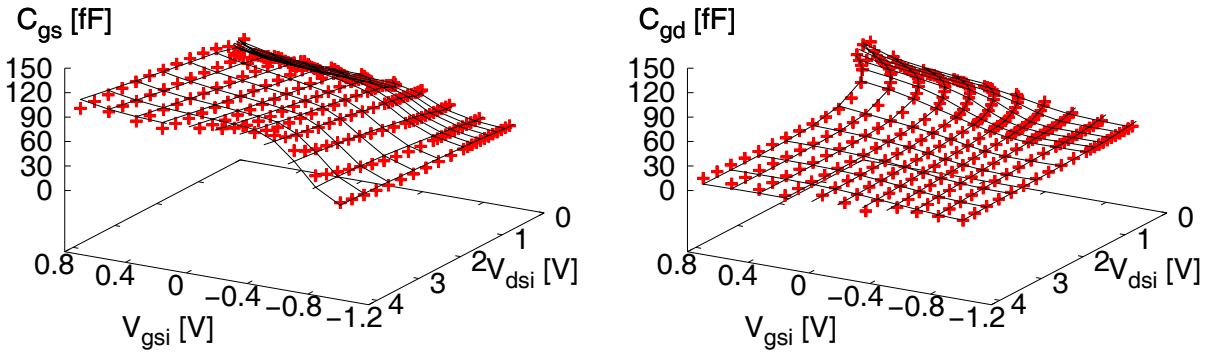

Figure C.10: Nonlinear gate capacitance C_{gs} (left) and C_{gd} (right) in a 2x50 μm GaAs pHEMT (PH15) device. Measured values (points) and nonlinear model (line).

Parameter	C_{pgs}	C_{pgd}	C_{gs1}	C_{gs2}	C_{gs3}	C_{gd1}	C_{gd2}
Value / fF	9.7	11.7	20.1	24.5	7.3	25.0	9.4

Parameter	V_{bi}	V_{t2}	V_{t3}	V_{t4}	V_{t5}
Value / V	1.0	-0.5	-0.68	-0.37	-0.36

Parameter	m	κ	ν	ι	ψ	θ
Value	0.4	6.36	2.40	7.16	0.59	0.22

Table C.9: Nonlinear capacitance model parameters of a 2x50 μm GaAs pHEMT (PH15).

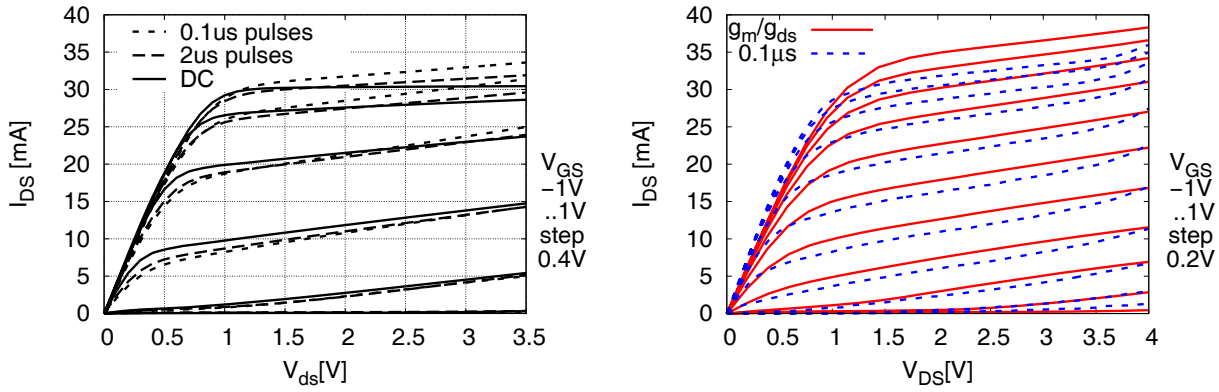

Figure C.11: Dynamic drain current in a 2x20 μm GaAs pHEMT (PH15). Left: $I_{\mathrm{dsac1}}$and I_{dsac2} (Pulsed-IV, 2 μs and 0.1 μs pulse width, quiescent point: $V_{\mathrm{gs}} = 0\,\mathrm{V}$, $V_{ds} = 2\,\mathrm{V}$). Right: I_{dsac3} (dynamic $g_{\mathrm{m}}/g_{\mathrm{ds}}$ integration, quiescent point:$V_{\mathrm{gs}} = -1\,\mathrm{V}$, $V_{\mathrm{ds}} = 0\,\mathrm{V}$).

Parameter	I_{ds}	I_{dsac1}	I_{dsac2}	I_{dsac3}
β	2.7511e-002	2.7189e-002	2.8336e-002	3.0629e-002
V_{to}	-5.3899e-001	-4.6647e-001	-4.3756e-001	-4.5492e-001
λ	1.2160e+000	1.0998e+000	1.1327e+000	9.3494e-001
α	7.3209e+000	5.2256e+000	4.6232e+000	2.8020e+000
μ	-7.4962e-003	-7.5596e-003	-1.8967e-002	-1.4667e-002
γ	1.1580e-001	1.2482e-001	1.4521e-001	1.2502e-001
δ	1.0140e-001	1.0315e-001	1.1387e-001	8.4989e-002
ξ	1.6353e+000	1.6884e+000	1.7273e+000	8.3138e-001
ζ	-3.1757e-001	-1.9369e-001	-1.9119e-001	-1.4818e-001
η	1.4970e+000	1.4991e+000	1.5915e+000	1.2214e+000
π_{eff}^{-1}	8.1050e-001	0	0	0

Table C.10: Dispersion drain current model parameters of the 2x20 μm PH15 GaAs pHEMT.

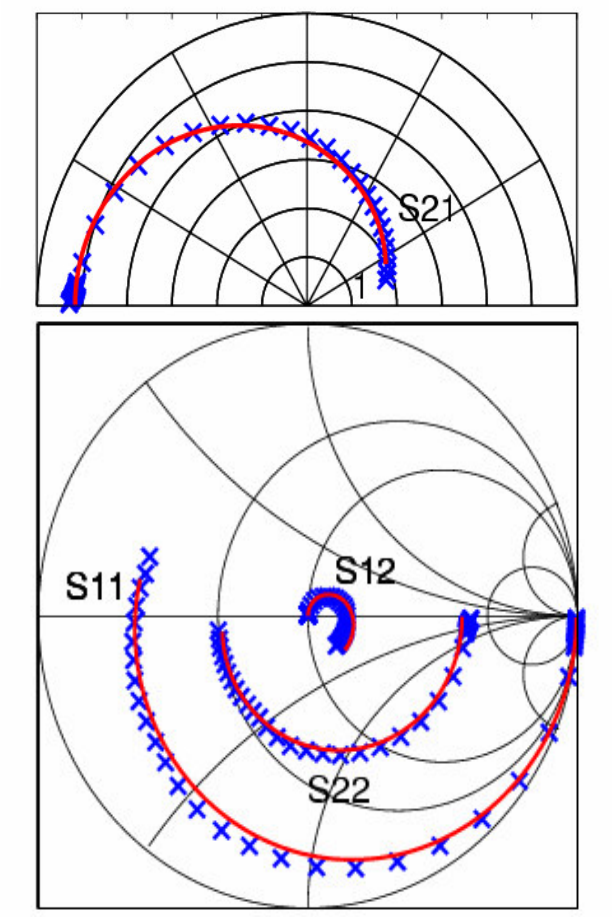

Figure C.12: 50 MHz - 50 GHz S-parameters of a 2x50 μm PH15 device, biased at $V_{gs} = -0.2\,V$, $V_{ds} = 2.4\,V$ ($\tilde{}g_{m,max}$). Measurement (dots) and model (lines).

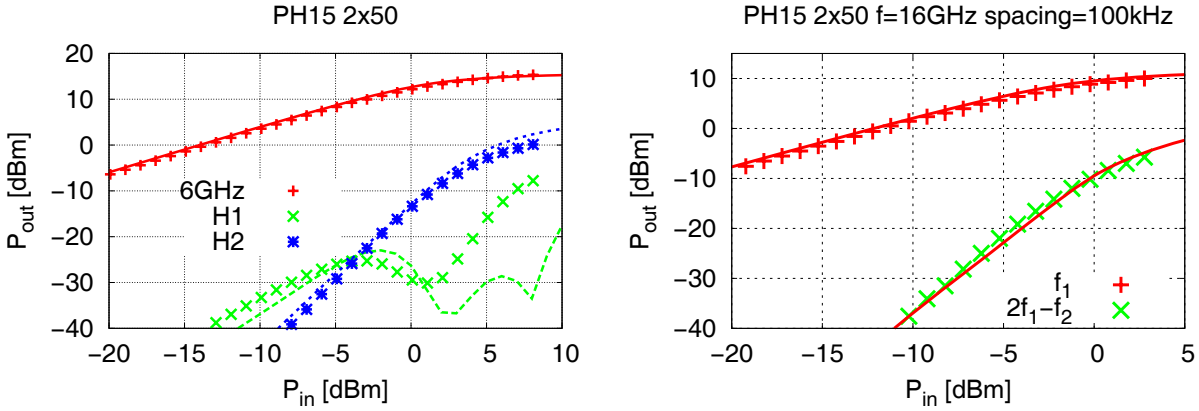

Figure C.13: One-tone power (left, 6 GHz fundamental) and two-tone power (right, 16 GHz fundamental) measurement of a 2x50 μm PH15 device, biased at $V_{gs} = -0.2\,V$, $V_{ds} = 2.5\,V$. Measurement (dots) and model (lines).

Parameter	Value
R_G	1.65 Ω
R_D	3.55 Ω
R_S	3.55 Ω
L_G	22.6 pH
L_D	22.0 pH
L_S	1.9 pH
C_{DS}	43 fF
R_{GSI}	10.6 Ω
R_{GDI}	21 Ω
τ	0.1 ps

Table C.11: Linear model parameters of a 2x50 μm PPH15 GaAs pHEMT.

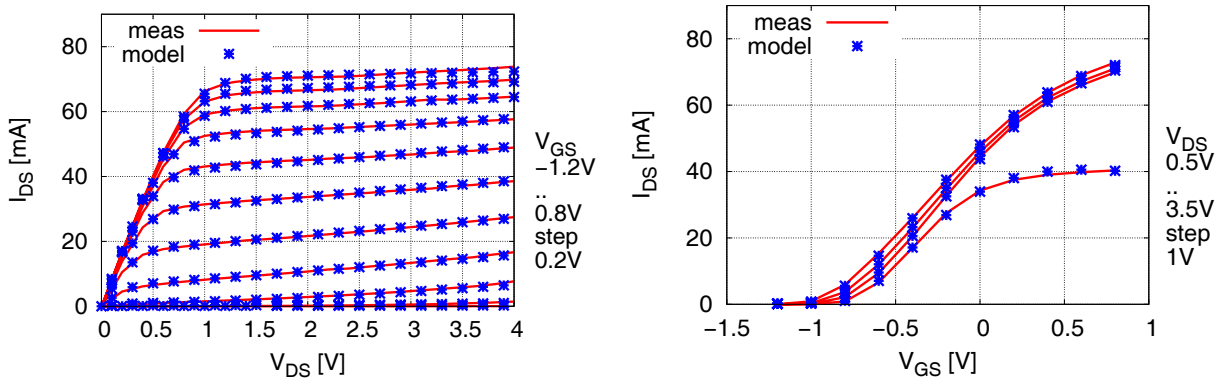

Figure C.14: Static drain current in a 2x50 μm PPH15 GaAs pHEMT device. Measured values (points) and nonlinear model (line). Output characteristics (left) and transfer characteristics (right).

C.3 Power AlGaAs/GaAs pHEMT

Parameter	Value
β	6.2036e-002
V_{to}	-7.3758e-001
λ	1.2183e+000
α	4.9611e+000
μ	9.9992e-004
γ	5.6293e-002
δ	9.9662e-002
ξ	1.0913e+000
ζ	-2.8839e-001
η	1.4918e+000
π_{eff}^{-1}	0.12

Table C.12: Nonlinear drain current model parameters of a 2x50 μm PPH15 GaAs pHEMT.

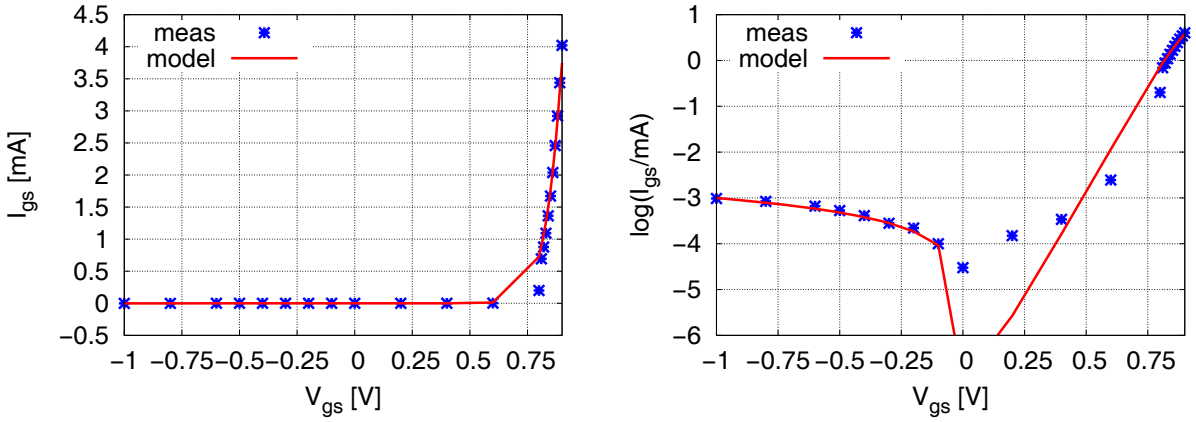

Figure C.15: Static gate current in a 2x50 μm PPH15 GaAs pHEMT device. Measured values (points) and nonlinear model (line) on a linear scale (left) and in logarithmic form (right).

Parameter	Value
n_{id}	1.8156e+000
I_{sgs}	1.7349e-011
I_{sgd}	1.5231e-011
G_{lgs}	1e-9
G_{lgd}	1e-9
f_c	0.8
I_{max}	20e-3
bv	-8.0e+000
I_{bv}	-7.4480e-006
n_{bv}	4.3538e+002

Table C.13: Nonlinear gate current model parameters of a 2x50 μm PPH15 GaAs pHEMT.

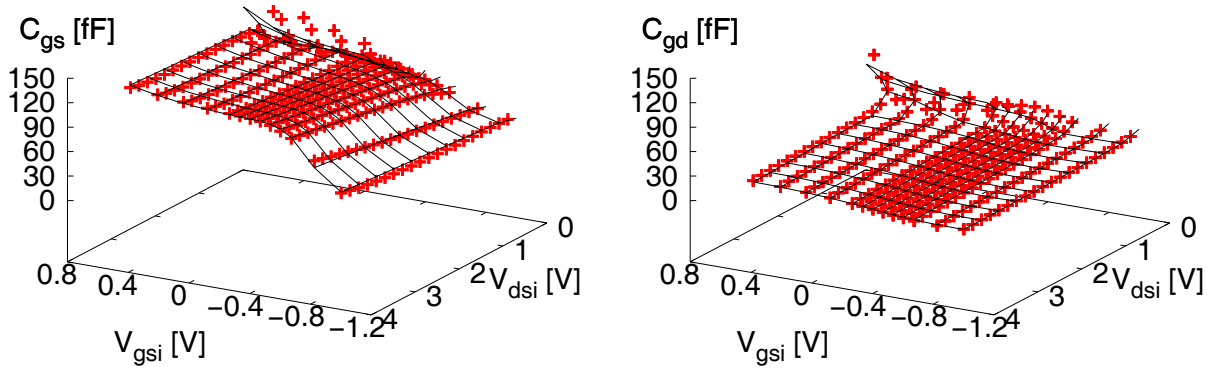

Figure C.16: Nonlinear gate capacitance C_{gs} (left) and C_{gd} (right) in a 2x50 μm GaAs pHEMT (PPH15) device. Measured values (points) and nonlinear model (line).

Parameter	C_{pgs}	C_{pgd}	C_{gs1}	C_{gs2}	C_{gs3}	C_{gd1}	C_{gd2}
Value / fF	13.6	15.4	15.6	28.1	6.9	20.3	21.5

Parameter	V_{bi}	V_{t2}	V_{t3}	V_{t4}	V_{t5}
Value / V	0.9	-0.59	-0.78	0.25	-0.23

Parameter	m	κ	ν	ι	ψ	θ
Value	0.4	6.27	1.92	32.9	0.58	0.18

Table C.14: Nonlinear capacitance model parameters of a 2x50 μm GaAs pHEMT (PPH15).

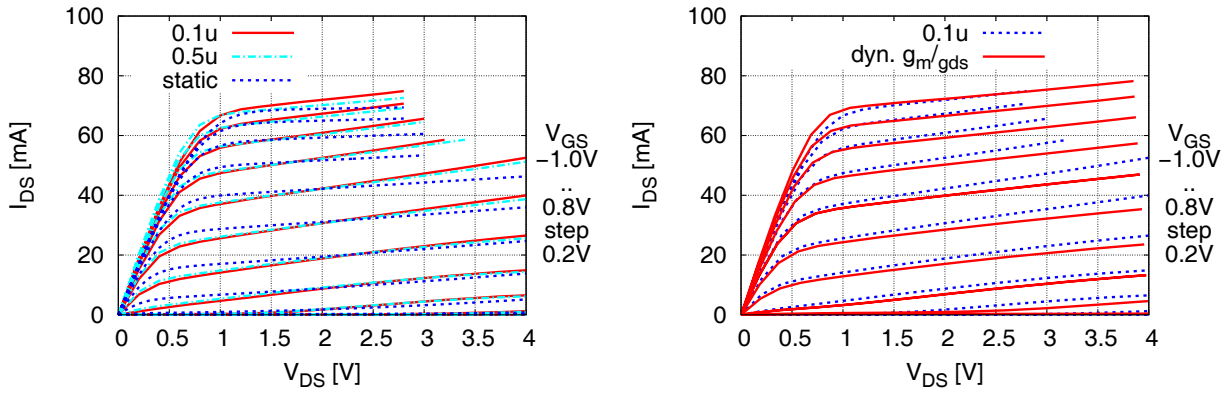

Figure C.17: Dynamic drain current in a 2x50 μm GaAs pHEMT (PPH15). Left: $I_{\mathrm{dsac1}}$and I_{dsac2} (Pulsed-IV, 0.5 μs and 0.1 μs pulse width, quiescent point: $V_{\mathrm{gs}} = -0.3\,\mathrm{V}$, $V_{\mathrm{ds}} = 2\,\mathrm{V}$). Right: I_{dsac3} (dynamic $g_{\mathrm{m}}/g_{\mathrm{ds}}$ integration, quiescent point:$V_{\mathrm{gs}} = -1\,\mathrm{V}$, $V_{\mathrm{ds}} = 0\,\mathrm{V}$).

Parameter	$I_{\mathrm{dc,static}}$	I_{dsac1}	I_{dsac2}	I_{dsac3}
β	6.2036e-002	6.0847e-002	6.1372e-002	6.4768e-002
V_{to}	-7.3758e-001	-6.2079e-001	-6.0653e-001	-5.3136e-001
λ	1.2183e+000	1.1432e+000	1.2088e+000	9.7207e-001
α	4.9611e+000	5.0671e+000	4.8781e+000	3.6849e+000
μ	9.9992e-004	-1.9897e-002	-2.0213e-002	-1.2594e-002
γ	5.6293e-002	1.1279e-001	1.2451e-001	9.6224e-002
δ	9.9662e-002	6.2083e-002	6.5756e-002	7.7152e-002
ξ	1.0913e+000	1.1172e+000	1.0498e+000	7.1533e-001
ζ	-2.8839e-001	2.1411e-002	-1.4224e-001	3.3216e-001
η	1.4918e+000	1.7158e+000	1.4250e+000	1.3768e+000
π_{eff}^{-1}	0.12	0	0	0

Table C.15: Dispersion drain current sources model parameters of a 2x50 μm PPH15 GaAs pHEMT.

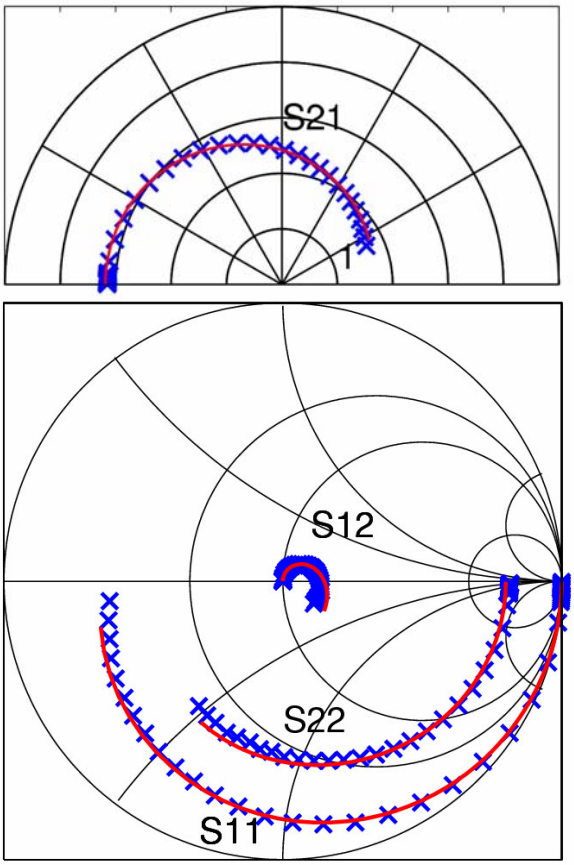

Figure C.18: 50 MHz - 50 GHz S-parameters of a 2x30 μm PPH15 device, biased at $V_{\mathrm{gs}} = -0.4\,\mathrm{V}$, $V_{\mathrm{ds}} = 2\,\mathrm{V}$ ($\tilde{}g_{\mathrm{m,max}}$). Measurement (dots) and model (lines).

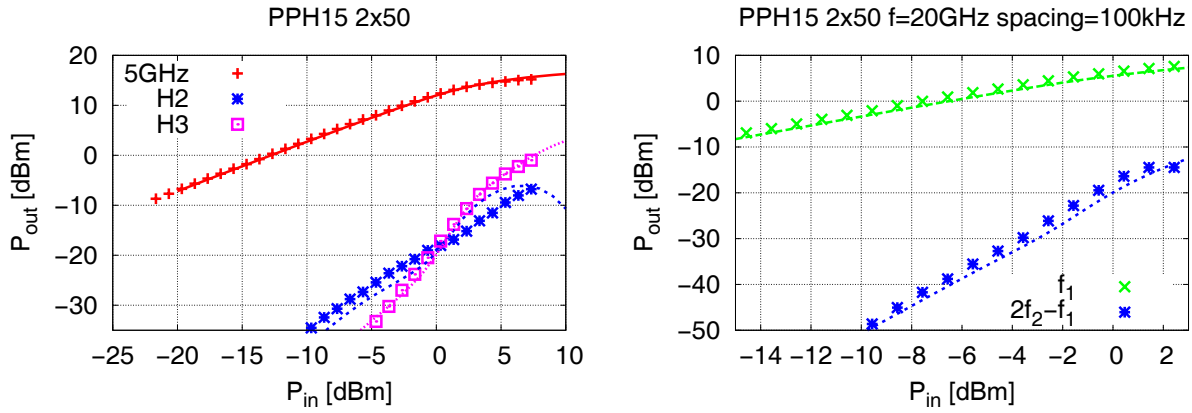

Figure C.19: One-tone power (left, 5 GHz fundamental) and two-tone power (right, 20 GHz fundamental) measurement of a 2x50 μm PPH15 device, biased at $V_{\mathrm{gs}} = -0.3\,\mathrm{V}$, $V_{\mathrm{ds}} = 2.5\,\mathrm{V}$. Measurement (dots) and model (lines).

Parameter	Value
R_G	5.4 Ω
R_D	6.5 Ω
R_S	6.5 Ω
L_G	26.5 pH
L_D	23 pH
L_S	0.5 pH
C_{DS}	8 fF
R_{GSI}	2 Ω
R_{GDI}	0 Ω
τ	0.1 ps

Table C.16: Linear model parameters of the 2x40 μm InP pHEMT.

C.4 InGaAs/InP pHEMT

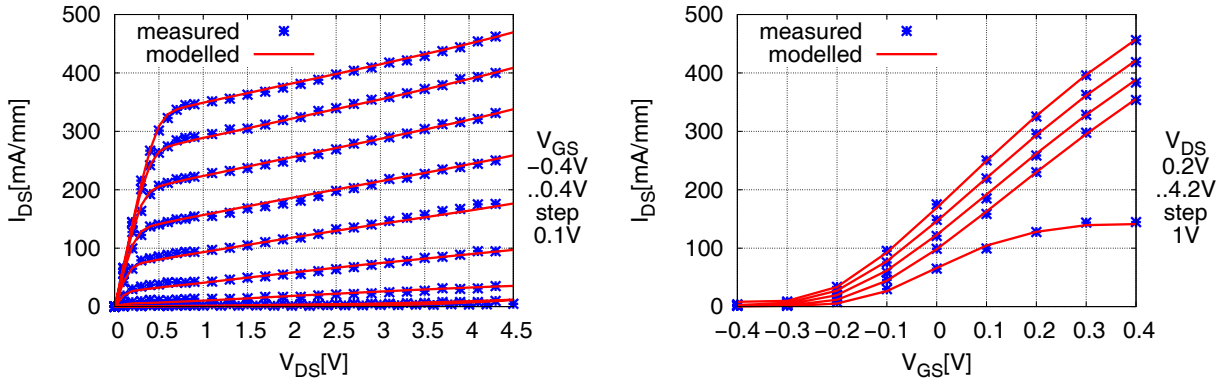

Figure C.20: Static drain current in the 2x40 μm InP pHEMT device. Measured values (points) and nonlinear model (line). Output characteristics (left) and transfer characteristics (right).

Parameter	Value
β	4.5479e-002
V_{to}	-2.3125e-001
λ	4.7965e+000
α	1.1974e+001
μ	-4.3888e-002
γ	1.0450e-001
δ	2.5131e-001
ξ	1.3396e+001
ζ	-6.0794e-001
η	1.3577e+000
π_{eff}^{-1}	1e-6

Table C.17: Nonlinear drain current model parameters of the 2x40 μm InP pHEMT.

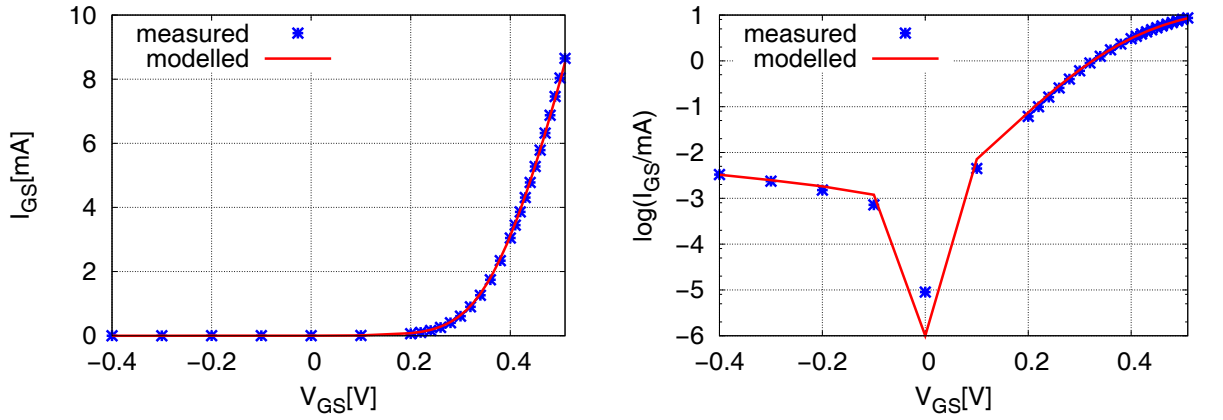

Figure C.21: Static gate current in the 2x40 μm InP pHEMT device. Measured values (points) and nonlinear model (line) on a linear scale (left) and in logarithmic form (right).

Parameter	Value
n_{id}	1.6953e+000
I_{sgs}	2.6218e-007
I_{sgd}	5.5111e-007
G_{lgs}	1e-9
G_{lgd}	1e-9
f_c	0.8
I_{max}	20e-3
bv	-5.0e+000
I_{bv}	-1.0239e-003
n_{bv}	4.2324e+001

Table C.18: Nonlinear gate current model parameters of the InP pHEMT.

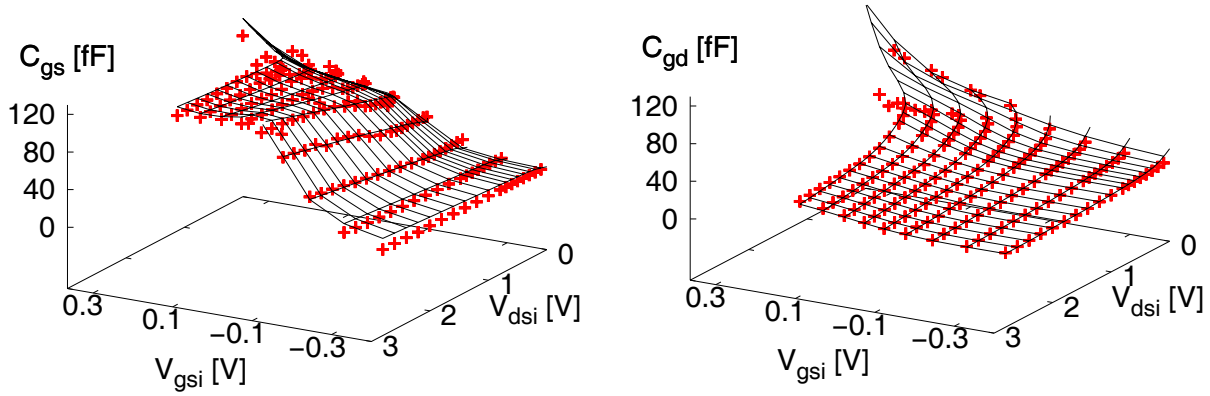

Figure C.22: Nonlinear gate capacitance C_{gs} (left) and C_{gd} (right) in the 2x40 μm InP pHEMT device. Measured values (points) and nonlinear model (line).

Parameter	C_{pgs}	C_{pgd}	C_{gs1}	C_{gs2}	C_{gs3}	C_{gd1}	C_{gd2}
Value / fF	8.0	8.0	20.0	44.3	9.5	30.0	20.0

Parameter	V_{bi}	V_{t2}	V_{t3}	V_{t4}	V_{t5}
Value / V	0.35	-0.11	-0.11	0.1	-0.22

Parameter	m	κ	ν	ι	ψ	θ
Value	0.5	14.2	2.79	10.0	0.32	0.11

Table C.19: Nonlinear capacitance model parameters of the 2x40 μm InP pHEMT.

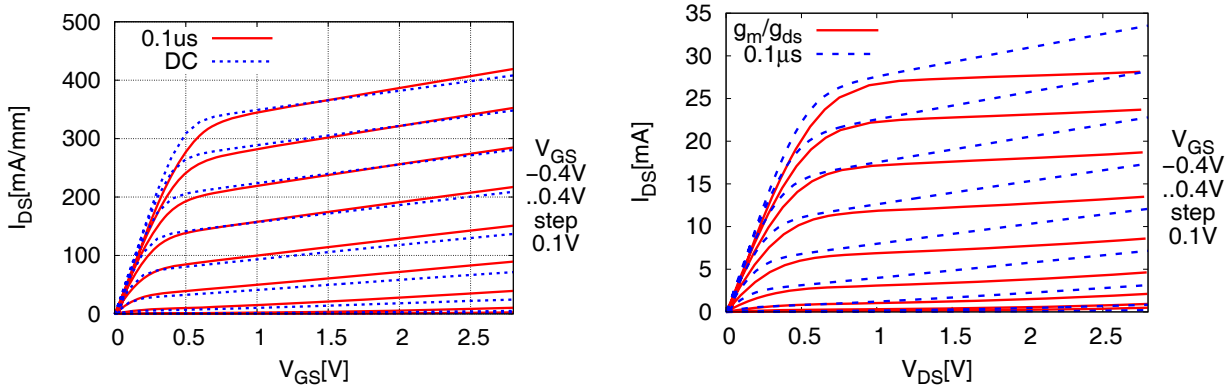

Figure C.23: Dynamic drain current in the 2x40 μm InP pHEMT device. Left: I_{dsac1} (Pulsed-IV, 0.1 μs pulse width, quiescent point: $V_{\mathrm{gs}} = 0\,\mathrm{V}$, $V_{\mathrm{ds}} = 2\,\mathrm{V}$). Right: I_{dsac2} (dynamic $g_{\mathrm{m}}/g_{\mathrm{ds}}$ integration, quiescent point:$V_{\mathrm{gs}} = -0.4\,\mathrm{V}$, $V_{\mathrm{ds}} = 1.6\,\mathrm{V}$).

Parameter	static	0.1 μs pulse	dynamic g_{m} / g_{ds}
β	4.5479e-002	6.2710e-002	3.9896e-002
V_{to}	-2.3125e-001	-2.3427e-001	-1.8736e-001
λ	4.7965e+000	7.4891e+000	2.5222e+000
α	1.1974e+001	7.9602e+000	2.9900e+000
μ	-4.3888e-002	-4.4480e-002	3.3578e-002
γ	1.0450e-001	8.4839e-002	2.0657e-002
δ	2.5131e-001	1.5043e-001	2.7387e-001
ξ	1.3396e+001	6.6689e+000	1.9010e+001
ζ	-6.0794e-001	-6.8821e-001	3.7909e-001
η	1.3577e+000	3.8413e-001	1.9631e+000
π_{eff}^{-1}	0	0	0

Table C.20: Dispersion drain current model parameters of the 2x40 μm InP pHEMT. Static current, pulsed-IV with pulses, dynamic integration.

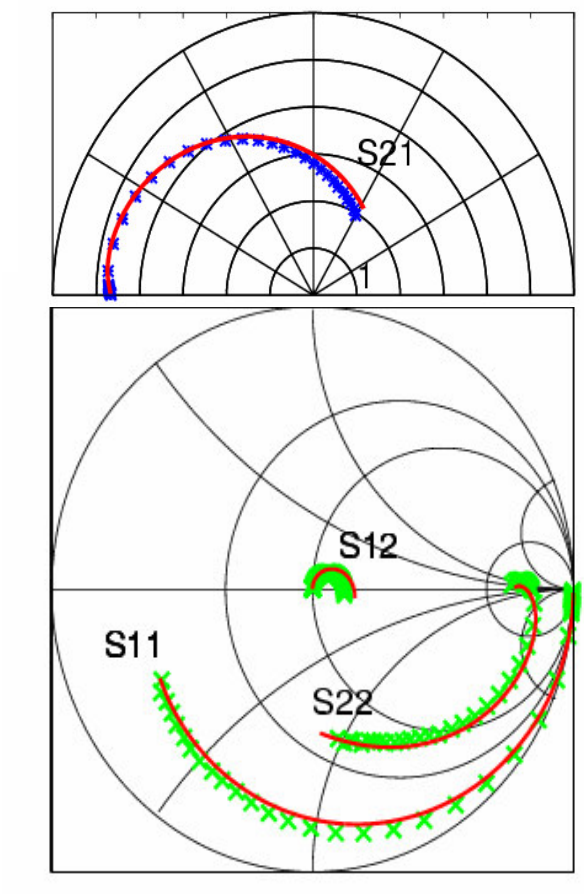

Figure C.24: 50 MHz - 50 GHz S-parameters of a 2x40 μm InP pHEMT device, biased at $V_{gs} = 0.1\,V$, $V_{ds} = 2\,V$ ($\approx g_{m,max}$). Measurement (dots) and model (lines).

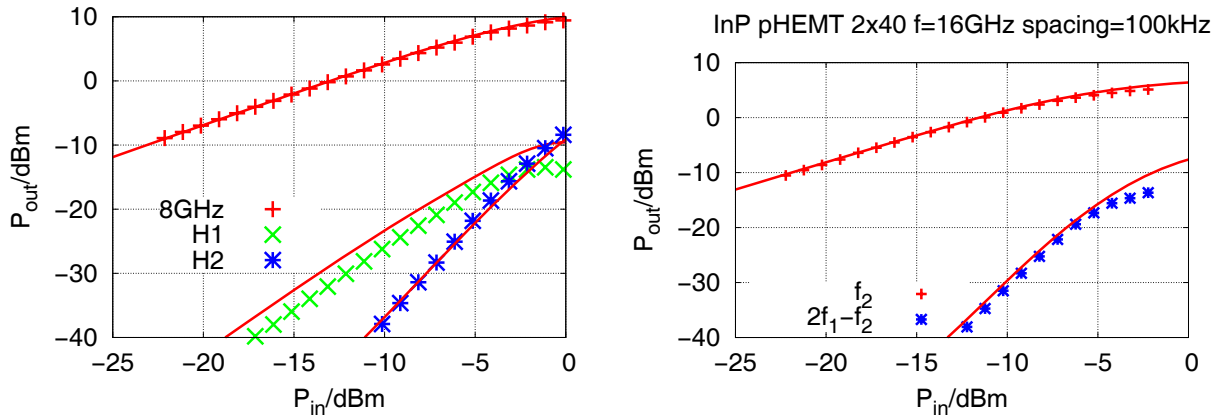

Figure C.25: One-tone power (left, 8 GHz fundamental) and two-tone power (right, 16 GHz fundamental) measurements of a 2x40 μm InP pHEMT device, biased at $V_{gs} = 0.1\,V$, $V_{ds} = 2.5\,V$. Measurement (dots) and model (lines).

Appendix D

SiGe mHEMT Two Metal Layers Process

A second metal layer needed to be included in the SiGe mHEMT technology in order to realise MMIC applications. Among others, it becomes possible to realise

- MIM type integrated capacitors,
- cross-overs in the CPW transmission lines,
- a reduction of ohmic losses in CPW transmission lines.

Fig. D.1 shows the full layer stack used in this work. Following the epitaxial layer stack which forms the mHEMT devices (compare Fig. 1.2), a 150 nm thick SiO_2 field oxide is deposited to separate the first metallisation layer (metal 1) from the substrate. The first metallisation uses a Ti/Pt/Au/Ti material sequence with respective thicknesses of 20/30/250/10 nm. It is structured by a lift-off process to form the contacts of drain- and source implantation regions as well as transmission lines. In a next step, 400 nm of SiO_2 are deposited to form the dielectric between metal 1 and metal 2. The dielectric is patterned in an etching step to generate openings for contacts to metal 1 as well as windows over the active devices. Next, metal 2 is deposited and patterned in another lift-off process. Its Ti/Au combination has a thickness of 50/2000 nm in order to minimise ohmic losses of the transmission lines. Finally, the transistor gates are e-beam written in a sequence consisting of three layers of photoresist to form mushroom gates with an approximately 100 nm footprint. With metal 2 introducing a high vertical topology to the layer stack, a 100 μm exclusion zone needs to be observed in the vicinity of transistor gates to guarantee a reliable control of the photoresist thickness during the e-beam lithography.

The use of metal 2 is illustrated in Fig. D.2, which shows a microphotograph of a realized cascode cell embedded within a travelling-wave structure. The common-gate transistor is grounded via a MIM capacitance structure. CPW transmission lines use underpaths (metal 1 passes below metal 2) to prevent odd-mode propagation.

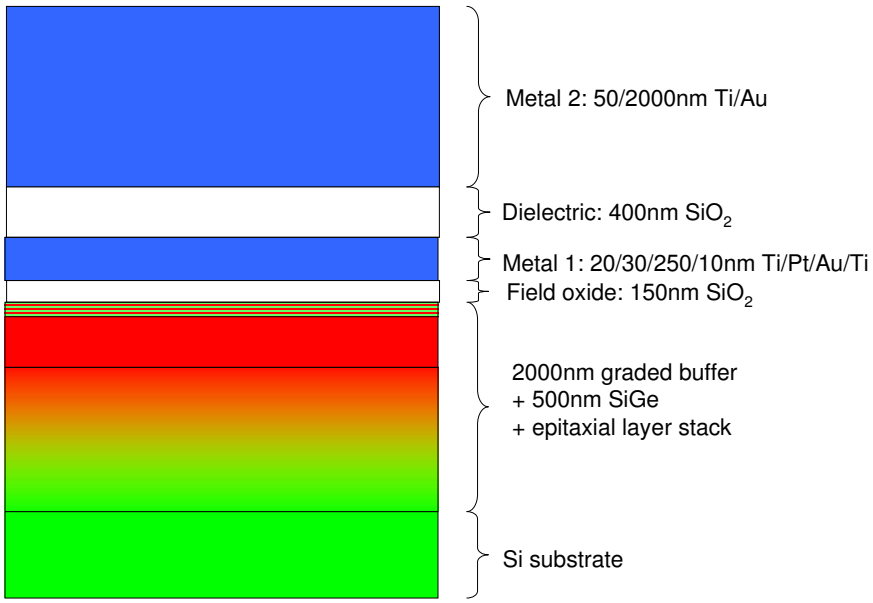

Figure D.1: Layer stack of the SiGe mHEMT MMIC process including two metal layers.

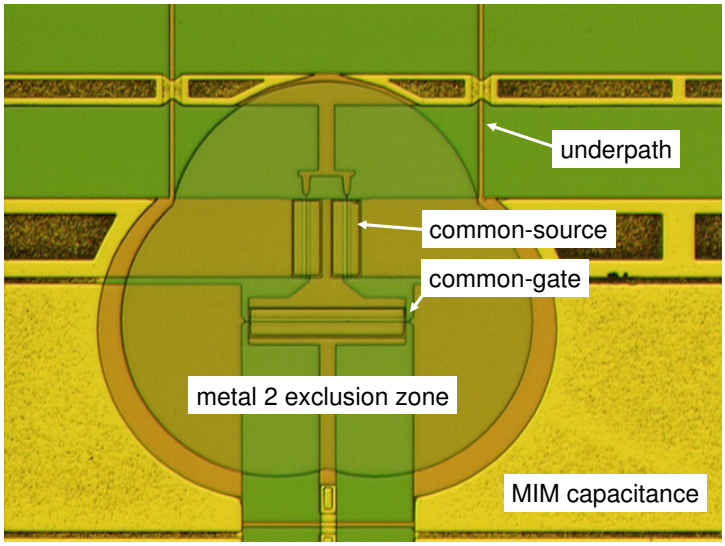

Figure D.2: Microphotograph of a cascode cell of a SiGe mHEMT TWA.

Curriculum Vitae

Born on 9 September 1973 in Stuttgart, Germany.

Education

1985 - 1993	Herzog-Christoph Gymnasium (Grammar school) in Beilstein
July 1993	Allgemeine Hochschulreife (qualification for general university studies)
1993 - 1995	Civil service (German national conscription) in Strasbourg
1995 - 2000	Studies in Electronic Engineering at University of Stuttgart, incl. Studies at Ecole Nationale Supérieure de Télécommunications in Paris Industrial training at Central Research Labs., London, UK Industrial training at Oxford Plasma Techn., Bristol, UK
December 2000	Dipl.-Ing. degree from University of Stuttgart with distinction "Anton u. Clara Röser Preis"

Professional Experience

2001	Visiting Research Associate at University College Dublin, Dept. of Electronic and Electrical Engineering, Ireland
2002 - 2005	Research Associate and Teaching Assistant at University of Ulm, Dept. of Electron Devices and Circuits
since November 2005	Scientist at Fraunhofer Institute for Applied Solid-State Physics, Freiburg