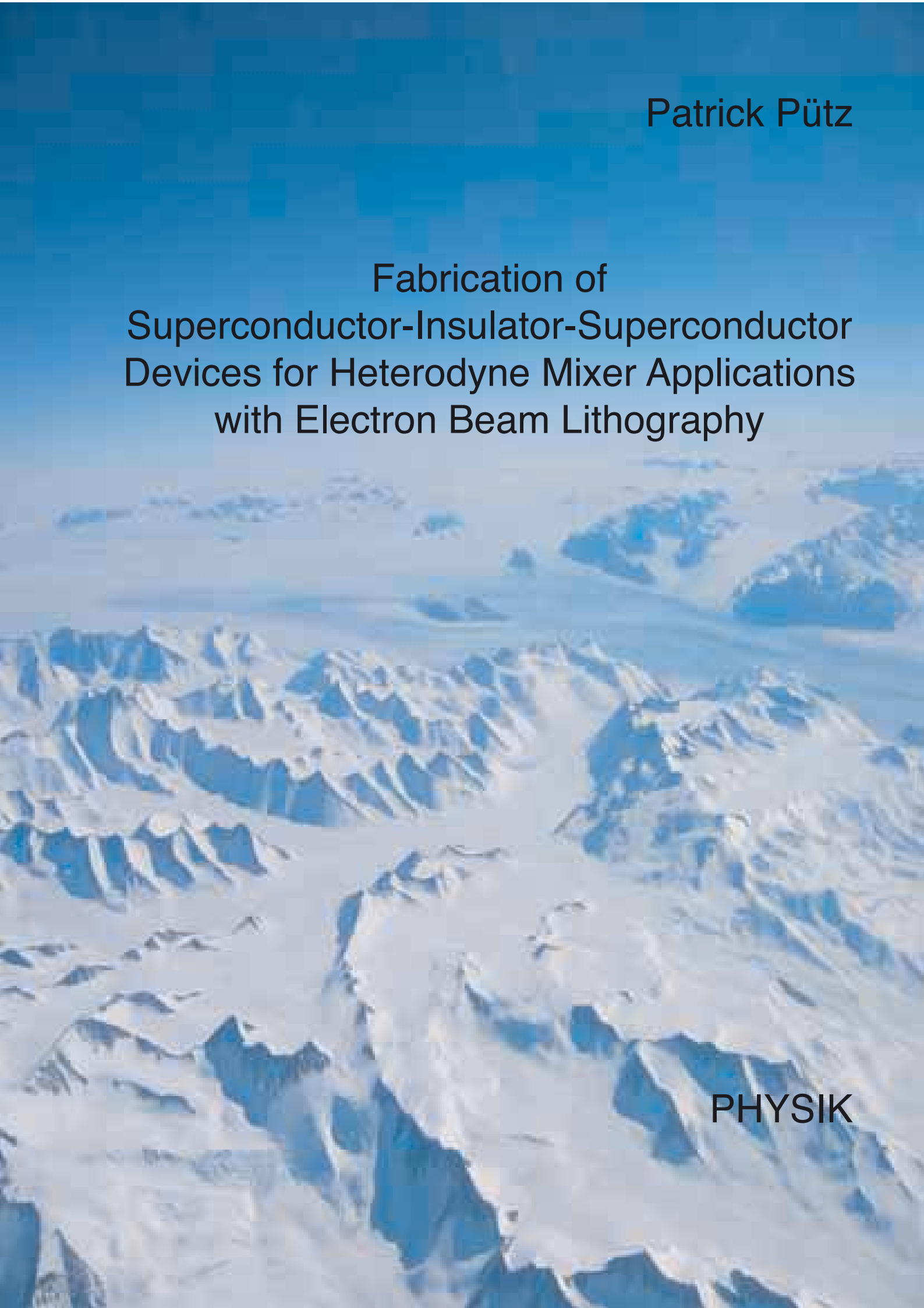
Patrick Pütz

Fabrication of Superconductor-Insulator-Superconductor Devices for Heterodyne Mixer Applications with Electron Beam Lithography



PHYSIK

Fabrication of Superconductor-Insulator-Superconductor Devices for Heterodyne Mixer Applications with Electron Beam Lithography

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The Trans-Antarctic Mountains photographed during the flight back from the Amundsen-Scott South Pole Station to McMurdo on November 27th, 2003. During my stay at the Antarctic Submillimeter Telescope and Remote Observatory (AST/RO) two new 800 GHz SIS mixers from KOSMA were successfully commissioned. © Patrick Pütz

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Abstract

This thesis describes the development of an enhanced fabrication scheme for superconductor-insulator-superconductor (SIS) junction devices and its implementation into regular fabrication at the KOSMA microstructure laboratory. The SIS junctions discussed in this thesis are used as frequency mixers in radio astronomical heterodyne receivers and provide quantum-limited performance and best possible sensitivity in the millimeter and submillimeter wavelength region. SIS mixers consequently are standard instrumentation for spectroscopic measurements between 80 GHz and 900 GHz. New generation SIS mixers demand more accurate fabrication of the devices than is possible with exclusively UV photolithographic based processes. Two examples for such new generation SIS mixer devices are the 640–800 GHz KOSMA Band 2 mixer contribution to the HIFI instrument of the Herschel Space Observatory and mixers for the SMART multi-pixel, dual frequency (475 GHz and 810 GHz band) receiver installed at the Gornergrat observatory in Switzerland. Requirements to device fabrication are further aggravated with future projects, which will extend SIS mixer application above 1 THz.

The influence of fabrication tolerances on simulated device RF performance, in particular submicron junction area reproducibility and the alignment accuracy of the integrated tuning circuit top electrode with respect to the junction position, will be discussed with help of the design of the SMART 475 GHz devices. As a result device design demands a junction area reproducibility of $\pm 5\%$ for $0.6\,\mu\mathrm{m}^2$ areas in order to meet the requirements for sensitivity and input bandwidth. In addition, the integrated tuning circuit top electrode alignment accuracy must be better than $0.3\,\mu\mathrm{m}$ in order to comply with RF band center position requirements.

In comparison, photolithographic definition typically yields relative junction area reproducibilities $\Delta A_J/A_J$ worse than $\pm 20\%$ for $0.6\,\mu\mathrm{m}^2 < A_J < 1\,\mu\mathrm{m}^2$ and alignment accuracies not better than $\pm 0.7\,\mu\mathrm{m}$. Device yield for even smaller junction areas, e. g. as required for THz frequency mixers, is negligible. Consequently, two new processes with more accurate electron beam lithography (e-beam) based definition of the junction area as well as the integrated tuning circuit top electrode features have been developed with this thesis.

During fabrication of a SIS device a process is needed to remove the junction insulation material from the junction's top electrode in order to enable contacting to the top electrode of the integrated tuning circuit. Whereas the UV photolithography scheme uses a self-aligned niobium etch process (SNEP) which employs a photoresist stencil lift-off of the insulation layer, this can not be carried out with the thin e-beam resist layer. Therefore a chemical mechanical polishing (CMP) process for planarization of the SiO_2 junction insulation and integrated tuning circuit dielectric layer was developed. CMP is terminated upon clearance of the junction top electrode and thus replaces the lift-off process. This PARTS (planarized all-refractory technology for low T_c superconductivity) scheme was invented by IBM in the eighties and has the advantage of yielding a planar junction top electrode and dielectric interface.

CMP process development started from scratch and within the scope of this thesis could be developed to a mature process used in regular fabrication, e. g. for the HIFI Band 2 devices that have to undergo a rigorous space-qualification process. SiO_2 layer planarity results of ± 20 nm are readily achieved across the 20 mm diameter device area of the fused quartz wafer, which is sufficient for reproducible device performance and ensures high fabrication yield. Surprisingly, CMP yields a very clean junction top electrode surface which enables a very good contact of the junction to the integrated tuning circuit top electrode. This has very beneficial influence on the device's DC I-V characteristics and device yield. Results presented with fabricated HIFI Band 2 devices clearly show that device gap voltage of these embedded trilayer type devices is systematically 0.2 mV higher and less scattered. Up to 90% device yield is achieved for the HIFI devices, which is a 60% improvement over the photolithographic fabrication scheme.

Development of the e-beam definition processes profited from the existing e-beam lithography system developed for hot-electron bolometer device definition. PMMA resist is used during definition of the junction areas and the pattern is transfered into the SIS trilayer either with a SiO_2 or an aluminum etch mask and subsequent reactive-ion etching (RIE). Junction area reproducibility for the HIFI devices has clearly improved but presently is still limited by the RIE process. These devices require a three-step RIE through all three junction layers and consequently demand a higher etch anisotropy for the process. On the other hand, devices which only require a one-layer RIE show a significantly improved relative junction area reproducibility of $\Delta A_J/A_J \leq 5\%$ for areas down to $0.6\,\mu\mathrm{m}^2$. This lies within specs for the SMART 475 GHz devices. SIS junctions with deeply submicron areas down to $0.1\,\mu\mathrm{m}^2$ were fabricated with excellent subgap leakage currents which confirms further development potential of the e-beam / CMP scheme.

E-beam definition of the top electrode of the integrated tuning circuit uses AZ5206 photoresist. The superior overlay accuracy of the e-beam system is demonstrated to be better than 200 nm. No influence of the e-beam writing on the junction's barrier characteristic is observed in the DC I-V curves. Unfortunately, mixer noise temperatures of these devices are much higher than expected. Analysis of the RF measurements indicate a contamination problem of the integrated tuning circuit top electrode niobium layer in case e-beam definition is employed. Devices fabricated with conventional photolithographic tuning circuit top electrode and e-beam junction area definition, however, show similar performance as SNEP processed devices. It is assumed that the contamination problem is photoresist-related and thus solvable.

Integration of the e-beam / CMP process for junction definition has been successfully demonstrated with the measured RF performance of HIFI Band 2 devices for frequencies between 640 GHz and 800 GHz. Mixer noise temperatures as low as $T_m = 53$ K (DSB) are achieved around 700 GHz (corresponding to less than $2h\nu/k$) and T_m stays below 200 K across the specified RF bandwidth of 160 GHz (corresponding to 22% relative input bandwidth). Mixer performance thus lies within reach of the baseline requirements for the HIFI instrument.

In summary, the e-beam / CMP based fabrication scheme is qualified for new generation device requirements and exhibits enough development potential for future THz frequency SIS mixer designs. In contrast to former photolithographic junction area definition, reproducibility of the junction area is now only limited by the RIE process. In particular, CMP must be judged as a very promising approach for submicron area SIS mixer device fabrication.

Zusammenfassung

Diese Doktorarbeit beschreibt die Entwicklung eines verbesserten Fabrikationsverfahrens zur Herstellung von Supraleiter-Isolator-Supraleiter (SIS) Tunnelelementen und dessen Integration in die vorhandenen Fabrikationsprozesse im KOSMA Mikrostrukturlabor. Die SIS-Tunnelelemente werden als Frequenzmischer in radioastronomischen Heterodynempfängern eingesetzt und bieten als quantenlimitierte Bauteile bestmögliche Empfindlichkeit im Millimeter- und Submillimeter-Wellenlängenbereich. SIS-Mischer gehören daher zur Standardinstrumentierung für spektroskopische Messungen im Frequenzbereich von 80 bis 900 GHz. Bei zukünftigen Array-Empfängern ist die Reproduzierbarkeit der elektrischen Charakteristika der einzelnen Mischerelemente untereinander von großer Bedeutung. Diese neue Generation von SIS-Mischern stellen höhere Ansprüche an die reproduzierbare Herstellung der Mischerelemente als rein UV-photolithographische Fabrikationsverfahren erfüllen können. Beispiele aktueller Instrumentierung, die diese solche Mischer enthalten, sind die 640–800 GHz Band 2 Mischer für das HIFI-Instrument des Herschel Space Observatory (ein Satellitenteleskop) und die Mischer des SMART Multi-Pixel-Zweifrequenz-Empfängers (475 GHz und 810 GHz Bänder), welcher im hauseigenen Observatorium auf dem Gornergrat in der Schweiz installiert ist. Die Ansprüche an die Herstellung der Mischerelemente wird bei zukünftigen Projekten, welche den Einsatz von SIS-Mischern in den Frequenzbereich über ein THz ausweiten sollen, noch weiter steigen.

Der Einfluss, den Fertigungstoleranzen auf die Hochfrequenzeigenschaften eines SIS-Mischerelements haben, soll anhand des Designs der SMART-Mischerelemente für das 475 GHz Band mit Hilfe von Simulationsrechnungen verdeutlicht werden. Hauptaugenmerk gilt dabei der Reproduzierbarkeit der Tunnelelement-Fläche und der Justagegenauigkeit der oberen Elektrode der integrierten Anpassstruktur in Bezug auf die Tunnelelement-Position. Ergebnis dieser Analyse ist die Forderung nach einer relativen Tunnelelement-Flächenreproduzierbarkeit von $\pm 5\%$ für eine Flächengröße von $0.6\,\mu\mathrm{m}^2$, um die Spezifikationen für Mischer-Empfindlichkeit sowie Eingangsbandbreite zu erfüllen. Außerdem muss die Justagegenauigkeit der oberen Elektrode besser als $0.3\,\mu\mathrm{m}$ sein, damit die Position der Mittenfrequenz des Eingangsbandes ausreichend genau ist.

UV-Photolithographie kann diese Rahmenbedingungen nicht erfüllen. So ist z. B. die typische relative Tunnelelement-Flächenreproduzierbarkeit $\Delta A_J/A_J$ schlechter als $\pm 20\%$ für Flächen zwischen 0.6 und $1\,\mu\mathrm{m}^2$ und die Justagegenauigkeit Schwankungen von $\pm 0.7\,\mu\mathrm{m}$ unterworfen. Für noch kleinere Flächen, wie sie z. B. für THz-Frequenzen benötigt werden, ist die Ausbeute photolithographisch basierter Fabrikationsverfahren verschwindend gering. Daher sind im Rahmen dieser Dissertation zwei neue Herstellungsprozesse entwickelt worden, die auf hochauflösender Elektronenstrahllithographie basieren um die beiden kritischsten Strukturen Tunnelelement-Fläche und obere Elektrode der integrierten Anpassstruktur deutlich präziser zu definieren.

Während der Herstellung von SIS-Mischerelementen wird ein Verfahrensschritt benötigt, der die Isolationsschicht des Tunnelelements von der oberen Tunnel-

elektrode entfernt, damit die obere Elektrode der integrierte Anpassstruktur kontaktiert werden kann. Für UV-Photolithographie wird dafür standardmäßig das Self-Aligned Niobium Etch Process (SNEP) Verfahren verwendet, bei dem die Junction definierende Photoresist-Struktur gleichzeitig als Schablone dient, um die Isolationsschicht über der Tunnelelektrode zu entfernen. Ein solches Lift-Off-Verfahren ist mit der wesentlich dünneren Elektronstrahl-Resistschicht nicht möglich. Daher wurde ein Planarisierungsprozess mit chemisch-mechanischem Polieren (CMP) entwickelt, um diese Isolationsschicht von der Tunnelelektrode abzutragen. Dieses PARTS-Fabrikationsverfahren (Planarized All-Refractory Technology for Low T_c Superconductivity) ist um 1985 bei IBM entwickelt worden und bietet gegenüber konkurrierenden Prozessen den Vorteil, dass die Isolationsschicht um das Tunnelelement herum völlig planarisiert wird.

Das CMP-Verfahren stellt für die Mischerelemente-Fertigung im KOSMA Mikrostrukturlabor eine völlige Neuentwicklung dar und konnte im Rahmen dieser Dissertation zu einem leistungsfähigen Prozess optimiert werden. Beispielsweise werden die HIFI Band 2 Mischerelemente mit diesem Verfahren hergestellt und sind damit Teil des strengen Raumfahrt-Qualifizierungsverfahrens. Planaritätsergebnisse von $\pm 20\,\mathrm{nm}$ für den aktiven Bereich (Durchmesser 20 mm) der Wafer werden für die SiO_2-Isolationsschichten, welche gleichzeitig auch als Dielektrikumsschichten für die Mikrostreifenleitungen der integrierten Anpassstrukturen dienen, erzielt. Damit ist eine ausreichende Reproduzierbarkeit der Mischerelemente und eine genügend hohe Ausbeute bei der Fertigung gewährleistet. Es stellt sich heraus, dass das CMP-Verfahren zu einer sehr sauberen Tunnelelement-Oberseite und deshalb zu einem verbesserten Kontakt zwischen dieser und der oberen Anpassstrukturelektrode führt. Dieses wiederum spiegelt sich positiv in der Strom-Spannungs-Kennlinie der Mischerelemente wider. Es werden Ergebnisse der HIFI Band 2 Mischerelemente-Fertigung präsentiert, welche klar darlegen, dass die Tunnelelement-Gapspannungen systematisch um 0.2 mV höher liegen und zudem eine geringere Streuung ihrer Werte aufweist. Für die HIFI Band 2 Mischerelemente werden Fertigungsausbeuten von bis zu 90% erreicht. Dies stellt eine Verbesserung um 60% gegenüber dem vorherigen UV-photolithographisch basierten Fertigungsverfahren dar.

Bei der Entwicklung der Elektronenstrahllithographie-Prozesse konnte auf existierende Hardware zurückgegriffen werden, welche zur Fabrikation der Hot Electron Bolometer Mischerelemente aufgebaut worden ist. Zur Definition der Tunnelelement-Flächen wird PMMA-Resist verwendet und das Muster mittels einer SiO_2- oder einer Aluminium-Ätzmaske und nachfolgendem Reaktiv-Ionen-Ätzverfahren (RIE) in die Tunnelelement-Schichtenfolge übertragen. Die Tunnelelement-Flächenreproduzierbarkeit für die HIFI-Mischerelemente ist dadurch deutlich verbessert worden und wird zur Zeit noch durch das RIE beschränkt. Ursächlich hierfür ist das aufwändige dreistufige RIE, welches für die HIFI-Mischerelemente benötigt wird um durch alle Tunnelelement-Schichten durchzuätzen, und die damit bedingte höhere Anforderung an die Anisotropie des RIE-Verfahrens. Demgegenüber lassen sich mit Mischerelementen, die nur ein einstufiges RIE-Verfahren benötigen, Tunnelelement-Flächenreproduzierbarkeiten für Flächen bis minimal $0.6\,\mu\mathrm{m}^2$ erzielen, die bereits der Spezifikation $\Delta A_J/A_J \leq 5\%$ genügen. Darüber

hinaus konnten Mischerelemente mit Flächen bis minimal $0.1\,\mu\mathrm{m}^2$ hergestellt werden, welche gleichbleibend geringe Leckströme aufweisen. Dies bestätigt damit das ausgezeichnete Potenzial des Elektronenstrahllithographie-CMP-Verfahrens für zukünftige Entwicklungen.

Zur elektronenstrahllithographischen Definition der oberen Elektrode der integrierten Anpassstruktur wird AZ5206 Photoresist verwendet. Es wird gezeigt, dass dabei Justagetoleranzen unter 200 nm erreicht werden. Anhand der Strom-Spannungs-Kennlinien ist kein negativer Einfluss der Elektronenstrahllithographie auf die Tunnelbarrieren-Eigenschaften festzustellen. Trotz des deutlichen Gewinns an Definitiongenauigkeit fallen die gemessenen Mischerrauschtemperaturen signifikant höher aus als erwartet. Die Analyse von HF-Messungen deutet auf eine Verunreinigung des supraleitenden Materials in der oberen Elektrode der integrierten Anpassstruktur hin, wenn diese elektronenstrahllithographisch definiert wird. Demgegenüber zeigen Mischerelemente mit konventioneller UV-Photolithographie und elektronenstrahllithographisch definierten Tunnelelement-Flächen vergleichbare Rauschtemperaturen (Empfindlichkeiten) wie rein photolithographisch definierte Mischerelemente. Es wird daraus gefolgert, dass die Verunreinigung vom AZ5206 verursacht wird und dass Abhilfe höchstwahrscheinlich die Verwendung eines anderen Resists liefern wird.

HF-Messungen von HIFI Band 2 Mischern im Bereich zwischen 640 und 800 GHz verdeutlichen das Leistungsvermögen, welches durch die Integration der Elektronenstrahllithographie-CMP-Fabrikationsschritte zur Definition der Tunnelelemente ermöglicht wird. Bei 700 GHz werden Mischerrauschtemperaturen von nur $T_m = 53\,\mathrm{K}$ (DSB) erreicht (dies entspricht weniger als dem doppelten des Quantenlimits $h\nu/k$), und T_m ist geringer als 200 K über die gesamte Eingangsbandbreite von 160 GHz. Damit liegt die erzielte Mischer-Empfindlichkeit schon nahe an den Spezifikationen für das HIFI-Instrument.

Zusammenfassend lässt sich feststellen, dass sich das Elektronenstrahllithographie-CMP-Verfahren zur Fertigung der neuen Generation von SIS-Mischerelementen qualifiziert und zudem ausreichend Entwicklungspotenzial für zukünftige Mischer-Entwicklungen im THz-Frequenzbereich bietet. Im Gegensatz zur vorherigen photolithographischen Definition wird die Tunnelelement-Flächenreproduzierbarkeit jetzt nur noch durch das RIE-Verfahren beschränkt. Insbesondere die Fertigung mittels CMP muss im Zusammenhang mit Submikrometer großen Tunnelelement-Flächen als sehr viel versprechend angesehen werden.

Contents

1

Introduction

The last twenty years has seen a great increase of our knowledge about the "cold" (2.7–100 K) regions of the interstellar matter (ISM) and the mechanisms of star birth. Due to the low temperatures this matter can gravitationally attract each other to form giant molecular clouds which contain a large amount of molecules and dust. These regions harbor star birth and, consequently, planet formation. In particular, the thermally excited electromagnetic radiation emitted from the atoms and molecules and its subsequent spectral analysis have contributed significantly to our understanding of the physical properties (temperature, density, mass) of these clouds. In case of the molecules the radiation predominately comes from rotational transitions and is emitted in the millimeter and submillimeter wavelength region, i. e. at frequencies of approx. 100 GHz upwards.

The linear molecule carbon monoxide is a good example. The lowest $J = 1 \rightarrow 0$ transition at 2.6 mm (115 GHz), was discovered back in 1970 by Wilson et al. and marks the beginning of modern radio astronomy of the ISM [86]. CO is the most common observable molecular species and exhibits a very simple rotational transition ladder with lines approx. every 115 GHz.[1] Up to the present day more than 130 different molecular species including simple amino acids have been clearly identified using their millimeter and submillimeter wavelength spectroscopic fingerprint [87].

Groundbased astronomical measurements towards higher frequencies are increasingly limited by transmission of our atmosphere to frequency bands where water vapor does not absorb the extraterrestric signals. Non-continuous transmission windows exist up to frequencies of 1.5 THz and can be observed from dry, high altitude sites. Well-known observatories are the IRAM[2] 30-m telescope at the Pico Veleta in Spain for millimeter wavelengths (< 300 GHz), and, for the submillimeter region (< 1 THz), the HHSMT[3] on Mt. Graham in Arizona and the

[1] The most abundant molecule H_2, with relative quantities of over 90% (by mass), is very light-weight and has not dipole moment. It thus does not emit any radiation at submillimeter wavelengths.

[2] Institut de Radioastronomie Millimétrique. http://www.iram.fr/

[3] Heinrich Hertz Submillimeter Telescope. http://aro.as.arizona.edu/

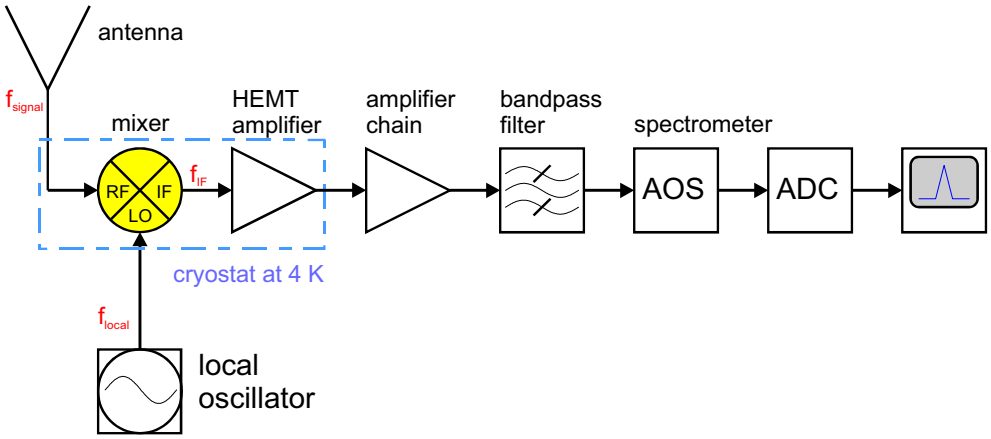


Figure 1.1: Block diagram of a principal heterodyne receiver setup for astronomical measurements at submillimeter wavelengths. The extraterrestric signal is fed from the telescope's antenna to the mixing element where it is combined with the local oscillator signal. The resulting intermediate frequency is amplified and and spectrally analyzed.

CSO[4] on Mauna Kea in Hawaii. KOSMA[5] operates its own observatory on the Gornergrat in Switzerland which is equipped with 230, 345, 490 and 810 GHz receivers. Additionally, 810 GHz mixers from KOSMA are used at AST/RO[6] at the Amundsen-Scott South Pole Station in the Antarctic.

Future groundbased observatories will be situated in the Atacama desert in Chile and, possibly, in the Antarctic. These special sites should enable measurements up to 1.4 THz. For even higher frequencies, air-borne observatories such as SOFIA[7] or space-based such as the HSO[8] are currently being built. Research of our atmosphere itself also profits from submillimeter measurements. Investigation of the ozone layer, for example, relies on measurements of the density of the radical chlorine monoxide (ClO) at 204 GHz.

1.1 Heterodyne receivers for radio astronomy

Progress in detection at submillimeter frequencies is directly correlated to advancement of receiver technology. Extraterrestric lines are very weak, line integrated powers for molecule detection are well below 10^{-15} W, and thus require very sensitive detectors. Additionally, the typical relative velocities between 0.1 km/s and 100 km/s of the cloud matter require a high spectroscopic resolution

[4] Caltech Submillimeter Observatory. http://www.submm.caltech.edu/cso/

[5] Kölner Observatorium für Submillimeter Astronomie. http://www.ph1.uni-koeln.de/gg/

[6] Antarctic Submillimeter Telescope and Remote Observatory. http://cfa-www.harvard.edu/~adair/AST_RO/

[7] Stratospheric Observatory for Infrared Astronomy. http://sofia.arc.nasa.gov/index.html

[8] Herschel Space Observatory. http://astro.estec.esa.nl/SA-general/Projects/First/first.html

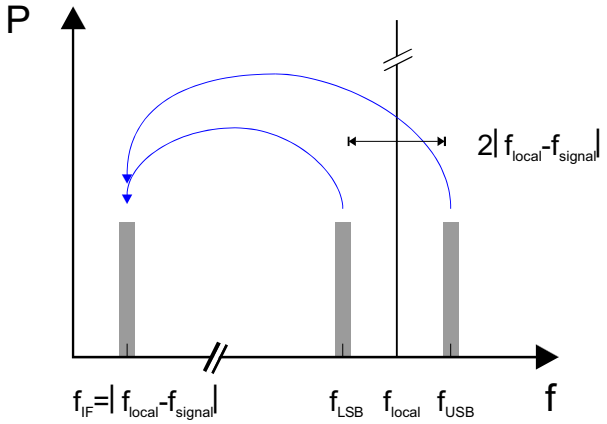


Figure 1.2: Visualization of the frequency conversion and spectral sensitivity of a heterodyne receiver.

of 10^3–10^6 in order to resolve the line profiles [29]. Coherent detection techniques originate from longer wavelength radio astronomy and are the best method for high resolution spectroscopy. In contrast to incoherent detection methods, thousands of frequency channels can be simultaneously measured with a spectrometer without RF input losses due to bandpass filtering [90]. Basis technology is a heterodyne receiver system which uses frequency downconversion of the extraterrestric signal with the help of a nonlinear device as frequency mixer. The mixer is the first active receiver component of such a receiver and with it the incoming signal is heterodyned with a many magnitudes stronger and slightly offset (typically 1–4 GHz) local oscillator signal (Fig. 1.1). Among others the mixer generates a signal at an intermediate frequency (IF) that is the difference between local oscillator (LO) and signal frequency. In this way a signal containing full phase and amplitude information of the extraterrestric signal is yielded at a 2–3 orders of magnitude lower frequency which then can be adequately boosted by state of the art low-noise HEMT amplifiers. As depicted in Fig. 1.2 the heterodyne receiver intrinsically detects power in two frequency bands, i. e. the sidebands, which lie symmetrically to the LO frequency position. For an unambiguous spectral line to frequency relation one sideband has either to be removed by filtering or determined by slightly de-tuning the LO or other means.

Fig. 1.1 shows that a heterodyne receiver consists of series connection of the components mixer, amplifiers, bandpass filter and spectrometer. Sensitivity of the total system is limited by the noise it adds to the signal. Noise contribution of every individual component is usually expressed by its noise temperature T_i which is defined as the equivalent noise power added by this component at the component's input divided by $k_B B$ (with bandwidth B). The total noise temperature of the receiver then is given by the generalized expression

$$T_{rec} = T_1 + \frac{T_2}{G_1} + \frac{T_3}{G_1 G_2} + \frac{T_4}{G_1 G_2 G_3} + \cdots , \tag{1.1}$$

where G_i is the gain (transmission) of each component. T_1 is the noise temperature

and G_1 the gain of the first component. The equation can be simplified to

$$T_{rec} = T_m + \frac{T_{IF}}{G_m} , \tag{1.2}$$

where T_m is the mixer noise temperature, G_m the mixer gain and T_{IF} the summarized noise temperature of the remaining components. Because usually $G_m < 1$ and $G_i > 1$ (for $i \geq 2$) it is clearly evident that the noise and gain contribution of the mixer is crucial for receiver performance.

Calculation of the total system sensitivity of the telescope needs to include the contributions of the optical components and, in case of a groundbased (and to less extend airborne) observatory, the atmospheric transmission. For this the same formalism as in Eq. 1.1 can be applied for calculation of the system noise temperature T_{Sys}. Particularly at submillimeter wavelengths atmospheric transmission becomes the dominant contribution to noise temperature with increasing frequency.

The minimum detectable signal temperature ΔT^A_{min} then is a measure of detection sensitivity:

$$\Delta T^A_{min} = \frac{T_{Sys}}{\sqrt{\Delta\nu\tau}} . \tag{1.3}$$

Here $\Delta\nu$ is the detection bandwidth (usually the bandwidth at the IF) and τ the integration time of the measurement[9] [28]. τ is limited by receiver stability (amplifier gain fluctuations, mixer stability, etc.), which is characterized by the Allan stability time, and typically is a few seconds. [1, 65]. Consequently, this creates a practical lower limit for ΔT^A_{min} for a system.

1.2 Superconducting mixer devices

Superconductor-Insulator-Superconductor (SIS) tunnel junctions at present are the mixing devices of choice for millimeter and submillimeter heterodyne receivers. Their first application for millimeter wave mixing was by Richards et al. at 36 GHz in 1979 [61]. SIS mixers now are used for observations in all atmospheric frequency windows up to 950 GHz as standard instrumentation. They provide more than a factor 5 lower noise temperatures than their predecessors, the Schottky diodes, and have two orders of magnitude lower LO power requirements (which is a very important factor for higher frequencies). The reason for this lies in the extremely non-linear characteristic of the quasiparticle branch visible in the I-V curve (Fig. 2.2) and the lack of series resistance in superconducting wiring material [81, 82]. As a matter of fact, the practically achieved double sideband (DSB) mixer noise temperatures lie close to the quantum limit [41]

$$T^{quantum}_{limit} = \frac{h\nu}{k_B} \quad (\text{i. e. } 4.8\,\text{K}/100\,\text{GHz}) , \tag{1.4}$$

[9] Strictly speaking, this equation only applies to uncorrelated white noise.

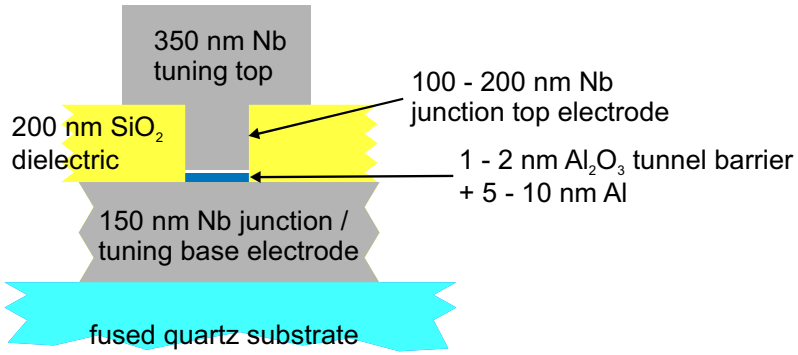


Figure 1.3: Schematic cross-section of a Superconductor-Insulator-Superconductor (SIS) device with standard Nb-Al/Al_2O_3-Nb trilayer including the integrated tuning circuit, e. g. as used for the 475 GHz SMART devices. In case the signal path uses a waveguide in front of the mixer element (as all SIS mixers built at KOSMA do) fused quartz is used as material for the wafer.

with reported DSB mixer noise only 2–3 times higher for frequencies $\nu \leq 700$ GHz (the material dependent gap frequency for niobium junctions) [22]. The remaining discrepancy is mainly due to imperfections in the barrier (leakage currents) and non-perfect matching to the SIS junction.

SIS mixer devices are fabricated with thin film, microfabrication methods as used in the semiconductor industry. In particular, this involves evaporation or sputtering based layer deposition, lithography to define features with submicrometer precision and reactive-ion etch processes. Typical layer thicknesses are 100–150 nm for the junction electrodes and only 1–2 nm for the tunnel barrier. Two developments concerning fabrication of the SIS mixer devices have significantly improved performance in the past and are now used as standard.

First, is the introduction of the Nb-Al/Al_2O_3-Nb junction trilayers [62, 24, 34] as a replacement for the lead based tunnel junctions (Fig. 1.3). The niobium junctions use a 5–10 nm thin aluminum base layer which is thermally in-situ oxidized before the counter electrode is deposited. Because aluminum has the property to completely wet the niobium surface, it leaves a very smooth interface and consequently very high quality tunnel junctions with low subgap currents can be fabricated.

Second, is the integration of a superconducting, thin film microstrip tuning circuit into the device which compensates for the SIS junction shunt capacitance by realization either of a series or parallel inductance and, additionally, yields a broadband match to the antenna (Fig. 1.4). A SIS junction forms a parallel-plate capacitor with large specific capacitances of around 90 fF/μm^2 which effectively short circuits the RF power when not compensated for. The frequency dependent characteristic of the resonant tuning circuit poses limitations on the SIS device RF input bandwidth. While the tuning circuit top electrode is fabricated as a microstrip line on top of the junction insulation layer, the tuning base electrode of an simple all-niobium device is already defined together with the junction base electrode and the RF chokes (Fig. 1.3, Fig. 1.4). The best achieved fractional input

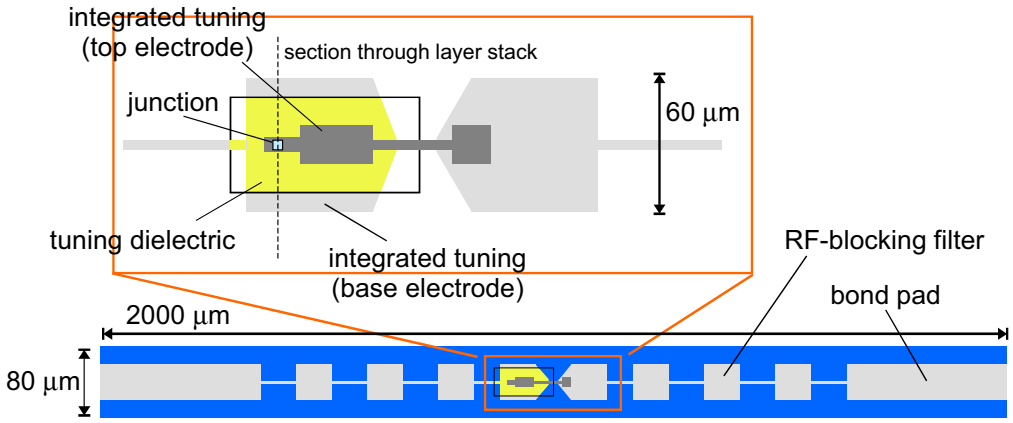


Figure 1.4: Schematic overview of a SIS waveguide device (not to scale). Dimensions are typical for a 800 GHz device. The magnified view of the junction area given in the inset shows a typical integrated tuning circuit with series inductor for compensation of junction capacitance and two $\lambda/4$ transformers for impedance match of the junction to the waveguide.

bandwidths are approx. 30% (this will be discussed more thoroughly in Sec. 2.2 and in Chap. 2.3) [40].

Quasiparticle mixing is limited by the combined double energy gaps $2\Delta_1 + 2\Delta_2$ of the SIS junction electrodes which, for a standard niobium SIS junction, is theoretically 1.4 THz ($4\Delta/h$), but practically limits operation to about 1.2 THz (see Sec. 2.1.2). RF losses in the tuning circuit electrodes deteriorate mixer performance already above the gap frequency $2\Delta/h$ of the used superconducting material (see Sec. 2.2). Therefore latest SIS mixer developments, e. g. SIS device development for HIFI Band 4 (960–1120 GHz) and 5 (1120–1250 GHz), incorporate hybrid superconducting junction electrodes with AlN instead of Al_2O_3 tunnel barriers and one or two normal conducting tuning circuit electrodes (see Sec. 6.5) [39, 47, 11]. For fabrication reasons only one niobium junction electrode is usually replaced by the higher energy gap superconductor NbTiN. Theoretically, the mixing limit of such a Nb-Al/AlN-NbTiN junction SIS device 1.9 THz. To date the highest operation frequency of a SIS mixer reported is 1.13 THz and a best receiver noise temperatures of 400 K was measured [37].

At frequencies above $(2\Delta_1 + 2\Delta_2)/h$ superconducting hot-electron bolometer mixers (HEB) are presently the best choice. These devices are made up of very thin (≤ 10 nm) and small ($< 1 \times 1\,\mu\text{m}^2$) superconducting microbridges and thus also require microfabrication. Unlike SIS tunnel elements, a HEB does not generate the IF signal through frequency multiplication but is sensitive to the amplitude modulation of the incident RF power. Due to the non-linearity of the R-T characteristics of the superconducting microbridge material, the modulation generates an oscillation of device resistance and thus the IF signal [57, 18, 71, 17, 72]. The upper limit for frequency mixing is not determined by the gap frequency of the

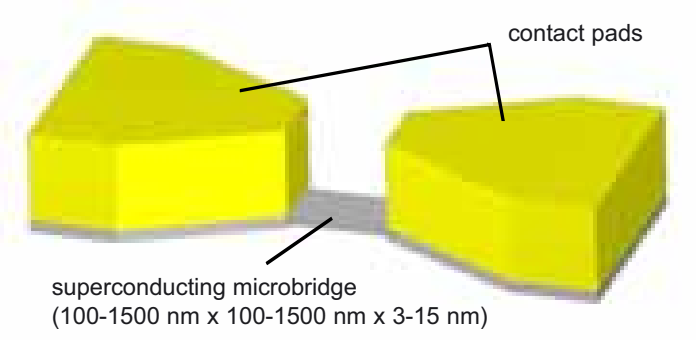


Figure 1.5: Schematic view of a superconducting hot-electron bolometer (HEB, drawn to scale). The normal conducting contact pads (gold) have a thickness of typically less than 100 nm. Phonon-cooled HEB species use thinner microbridges with larger lateral dimensions than their diffusion-cooled counterpart. Illustration adapted from [72].

material.[10]

The speed of a HEB, i. e. the highest possible IF frequency it can generate, is determined by the relaxation time of the hot electrons in the microbridge which are created by absorption of the RF power. Devices with two different types of cooling mechanisms are used. One kind of device relies on phonon-cooling (NbN or NbTiN microbridge) through the substrate while the other employs diffusion-cooling (Nb or Ta microbridge) through normal-conducting contact pads. Although HEB mixers have only been around for about 10 years their performance is significantly better than competing Schottky diodes up to the highest presently evaluated frequencies of 2.5 THz [22].

The phonon-cooled HEB species show better noise temperatures but somewhat limited IF bandwidth performance, e. g. 800 K at 1.6 THz with approx. 4 GHz IF bandwidth, whilst the diffusion-cooled HEB species display higher IF bandwidths with the penalty of worse noise temperatures, e. g. 1800 K at 2.5 THz with $\geq$ 9 GHz IF bandwidth [13, 88]. To date most of the development efforts focus on the phonon-cooled species.

Nevertheless much is still unclear concerning the practical operation of HEB devices (e. g. receiver stability issues) and presently only one observatory is running a HEB receiver for astronomical observations, namely the RLT in the Atacama desert in Chile.[11] [12] Nevertheless HEB devices will play a crucial role for important upcoming projects, like for the HIFI[13] Band 6 mixers (1410–1910 GHz) of

[10] At very high frequencies approaching near infrared wavelengths, the bridge at one point will become transparent for incoming photons.

[11] Receiver Lab Telescope. http://cfa-www.cfa.harvard.edu/srlab/

[12] In February 1999 and January 2000 the CO J $= 7 \rightarrow 6$ and CO J $= 9 \rightarrow 8$ transitions at 807 GHz and 1037 GHz, respectively, have been detected with a phonon-cooled HEB mixer during observing runs at the HHSMT.

[13] Heterodyne Instrument for FIRST. http://www.sron.nl/divisions/lea/hifi/

the Herschel Space Observatory and for GREAT[14] (1.4–4.8 THz) and CASIMIR[15] (1.2–2.1 GHz) currently being developed for SOFIA. It is furthermore planned to operate a groundbased receiver with a HEB mixer in the last atmospheric frequency window at 1.4 THz on APEX[16] .

Presently, the turnover point between HEB and SIS mixer operation is under investigation. For frequencies $> (2\Delta_1 + 2\Delta_2)/h$ HEB mixers have no competitors to date. At lower frequencies HEB mixers have the advantage of imposing no device limitation on RF input bandwidth and require half a magnitude less LO power than SIS mixers. In particular for array receiver applications LO power is a problem and for THz frequencies this might hinder operation of SIS mixer devices.

But SIS mixers deliver better performance than HEB mixers in the presently evaluated frequency range (< 1.13 THz). Best reported SIS mixer noise temperatures are roughly 50% better than HEB noise temperatures at the same frequency. Additionally, SIS mixers are much better understood and demonstrate one order of magnitude larger IF bandwidths.

Therefore it seems very worthwhile to drive SIS mixer development into the THz region. As a basis for this undertaking, SIS mixer device fabrication has to be enhanced in order to yield a significantly higher accuracy of the critical device dimensions.

With that said the goal of this PhD thesis work is set.

1.3 Limitations of UV photolithography based fabrication

The necessity for integrated tuning circuits makes the performance of the SIS mixer device very susceptible to fabrication tolerances. Optimum design of the integrated tuning circuit requires that the most important parameters junction area A_J and the alignment accuracy of the tuning circuit with respect to the junction both need to be scaled approx. $\propto 1/\nu$. Chap. 2.3 will motivate that for SIS mixers operating at low frequencies around 500 GHz it is already beneficial to use submicron junctions areas in the $0.6\,\mu\text{m}^2$ range with a relative area reproducibility of $\pm 5\%$ in order to meet the requirements for sensitivity and input bandwidth as

[14] German Receiver for Astronomy at Terahertz Frequencies. http://www.sofia.arc.nasa.gov/Science/instruments/instruments_great.html

[15] Caltech Submillimeter Interstellar Medium Investigations Receiver. http://www.sofia.arc.nasa.gov/Science/instruments/instruments_casimir.html

[16] Atacama Pathfinder Experiment. http://www.mpifr-bonn.mpg.de/div/mm/apex.html

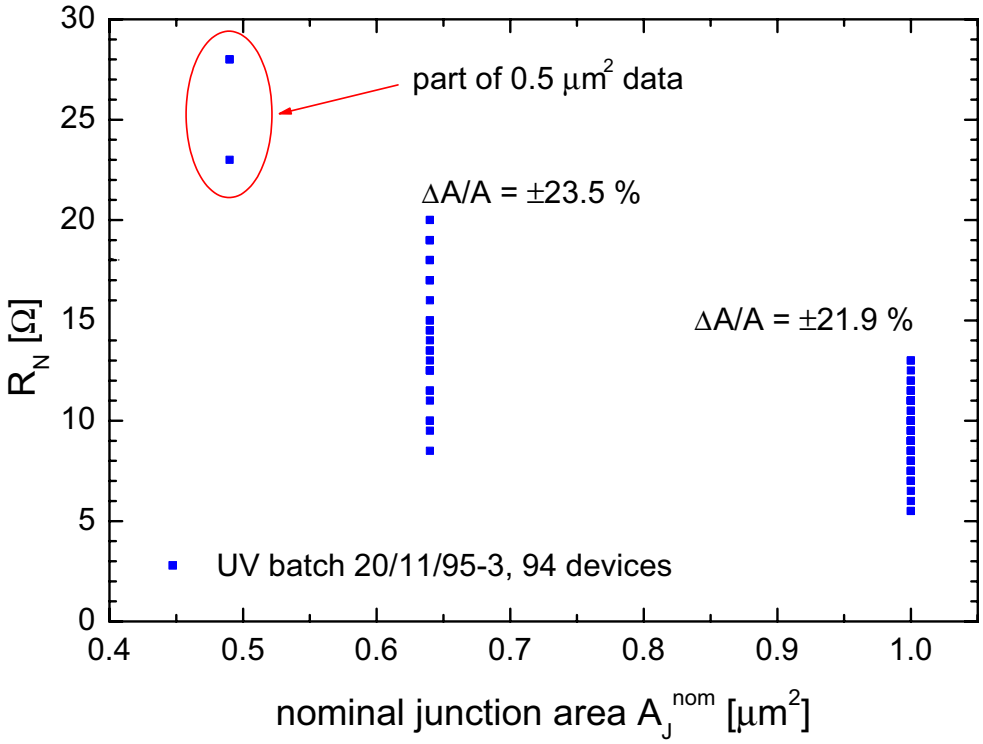


Figure 1.6: Typical junction area reproducibility of SIS devices from one wafer with exclusive UV photolithographic (UV-SNEP) definition. The 0.5 μm^2 data points are included in order to demonstrate the failure of UV photolithography based fabrication of such small areas (the few devices with a SIS I-V characteristic show a R_N spread greater than the y-axis scale).

well as device reproducibility. In addition, the alignment accuracy of the integrated tuning circuit top electrode must be better than 0.3 μm in order to yield a reproducible RF band center position.

Before this thesis work all definition processes used at the KOSMA microstructure laboratory were based on UV photolithography. The manually operated mask aligner contact photolithography processes typically yield relative junction area reproducibilities $\Delta A_J/A_J$ worse than $\pm 20\%$ for $0.6\,\mu\text{m}^2 < A_J < 1\,\mu\text{m}^2$ and alignment (overlay or registration, respectively) accuracies not better than $\pm 0.7\,\mu$m. Fig. 1.6 presents a typical junction area reproducibility result of SIS devices from one wafer fabricated with standard UV photolithography (UV-SNEP, see Sec. 1.4.1). Here the normal resistance R_N value of each junction is plotted against its designed area. The R_N spread is $\propto 1/\Delta A_J$ variation and thus can be used for junction area reproducibility analysis (see Eq. 2.5). Most notably, even the 1 μm^2 areas show a R_N spread more than a factor 4 above the design requirements. The 0.5 μm^2 data points indicate a complete failure of the UV photolithography based fabrication process for junction areas below 0.64 μm^2.

Of course, all good SIS mixer performance reported to date are a direct result of successful fabrication and show that design requirements can be met, but one must bear in mind that these devices have undergone a strict selection process.

In other words, device fabrication yield is of concern and design compromises (e. g. larger junction areas, device layout variations) are the usual workaround in order to achieve an acceptable amount of working SIS devices within fabrication tolerances. For THz devices, where junction areas will have to be $\leq 0.5\,\mu\mathrm{m}^2$, as well as for current lower frequency receiver projects with multi-pixel array receivers, which require several as equal as possible devices, such an approach is not acceptable any more.[17]

Development and fabrication of the 475 GHz devices for the dual-frequency array receiver SMART (Submillimeter Array Receiver for Two Frequencies, 8×475 GHz and 8×800 GHz mixers, Gornergrat) and the device development for the HIFI Band 2 mixers (Herschel Space Observatory) are examples for current development and fabrication efforts at KOSMA [21, 59, 20]. Fabrication of these devices directly benefits from the process development work undertaken in this thesis and the results of the here presented fabrication process will mainly be discussed in the context of these applications.

For mid-term device development multi-junction devices are interesting. Equivalent to multi-pixel receivers these circuits rely on junction area reproducibility. Under discussion are integrated SIS circuits which combine sideband separation and / or balancing with up to four junctions[18] as well as designs with (inhomogeneous) junction arrays for very large RF input bandwidths ([42, 43, 84] and [68, 75, 69, 74], respectively).

In addition to THz mixer development, in a more generalized view beyond in-house fabrication at KOSMA, long-term development will also have to focus on concepts for the ALMA (Atacama Large Millimeter Array) project. This array will consist of 64 12 m-telescopes with receivers for all millimeter and submillimeter atmospheric frequency windows up to 900 GHz. In comparison to current combined mixer output of all microfabrication labs involved in SIS mixer fabrication a comparably huge amount (hundreds!) of SIS mixers will be needed. A high yield, high performance fabrication process seems helpful to solve this "logistic adventure", to say at least, and here presented thesis work may give some fresh stimulus.

1.4 Enhancement of SIS mixer device fabrication

Modern UV projection photolithography equipment, i. e. the stepper and scanner hardware used for definition of semiconductor circuits, would meet the performance requirements for feature size and alignment accuracy, but are eliminated by the tremendous purchasing and maintenance costs involved. Consequently, electron beam lithography (e-beam) is the only way to overcome the limitations

[17] The concept of an array receiver is only justified when all pixels are just as sensitive as a single-pixel receiver and their individual performance as close as possible. Only then observations can profit from faster mapping.

[18] e. g. as in the ALMA Memo Series: http://www.alma.nrao.edu/memos/

of photolithographic mask aligner definition.[19] Luckily, at KOSMA an e-beam system already had been developed for HEB fabrication and in regular use prior to this thesis work [17]. Lateral dimensions down to $100 \times 100\,\mathrm{nm}^2$ are routinely defined and overlay accuracies between the bridge and heat-sinks of less than 200 nm are achieved [72]. This should bear sufficient resolution, even for the long-term (THz) SIS mixer projects.

With all this said it was decided to develop a new SIS junction fabrication process with e-beam definition of the most critical device features junction area and top electrode of the integrated tuning circuit while, for speed reasons, staying with conventional UV photolithography for all other less critical features.

1.4.1 Development of e-beam / CMP fabrication process

E-beam definition of the junction area poses a problem when used in combination with the quasi-standard SNEP (self-aligned niobium etch-back process) scheme and requires major effort in process development. As illustrated in Fig. 1.7 (left column) with SNEP a lift-off of a photoresist stencil is used in order to remove the junction insulation and tuning circuit dielectric material from the top of the junction. Here the same photoresist stencil is used during prior reactive-ion etch definition of the junction top electrode, thus eliminating the need for opening up an precisely aligned via through the dielectric onto the junction. This self-aligned process enables further contacting of the junction to the top electrode of the integrated tuning circuit. The problem is that this scheme does not work in conjunction with an e-beam resist layer for high-resolution e-beam lithography. E-beam resist must be more than a factor five thinner than a typical UV photoresist (e. g. 200 nm vs. 1200 nm) as otherwise the writing resolution is decreased through electron scattering. With such a thin layer a lift-off process is not possible with dielectric layer thicknesses around 200 nm, because not enough side wall area is given for solvent attack. To make matters more complicated the high-resolution resist material of choice PMMA[20] is a positive tone resist which means that the electron beam defines a hole into the layer. Consequently, an additional process for pattern transfer to an etch mask is made necessary prior to RIE definition of the junction.

Two well-known processing schemes are used for submicron area SIS mixer device fabrication in conjunction with PMMA e-beam definition and were taken into consideration for development of the junction definition process. These will be described in the following and the choice of the selected fabrication scheme motivated.

First is an expanded SNEP scheme developed at JPL[21] [49]: Here the PMMA features are transfered via a deposited thin ($< 100\,\mathrm{nm}$) hard etch mask (e.g. chrom-

[19] Although e-beam lithography equipment is not "cheap", it is after all still a magnitude "cheaper" than such projection lithography equipment. The industry does not use e-beam lithography for device manufacturing due to the inherently low throughput of the process.

[20] Polymethylmethacrylate

[21] Jet Propulsion Lab, Pasadena, CA

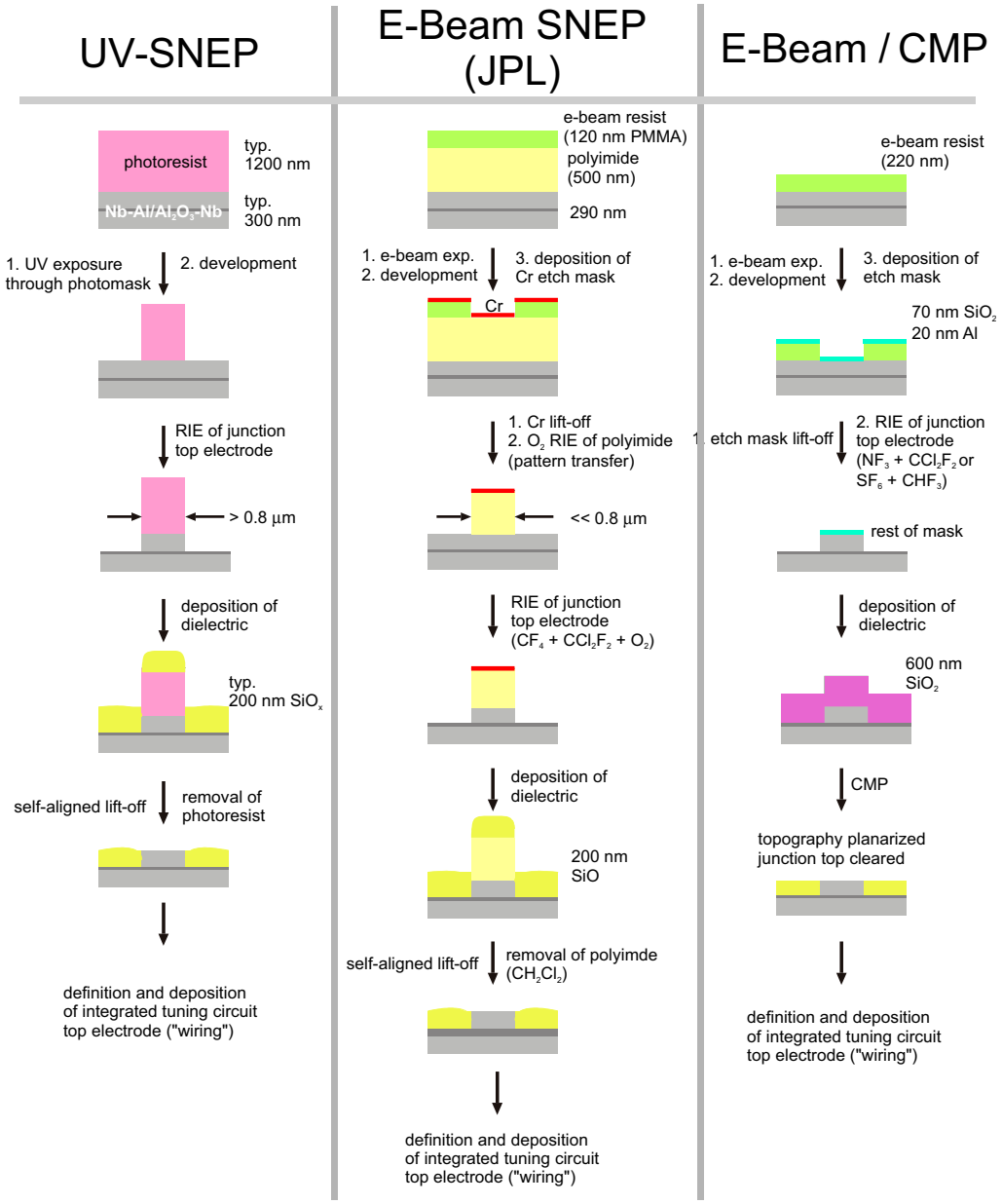


Figure 1.7: Comparison of typical UV photolithography with two possible e-beam based fabrication schemes used for SIS mixer device definition. For each step a cross-section through the SIS junction is illustrated together with typical layer thicknesses. For clarity reasons some process steps have been combined. Left column depicts the niobium self-aligned etch process (UV-SNEP) fabrication flow as used at KOSMA and as basis for junction definition in many other labs. Middle column shows the expanded SNEP process for e-beam junction definition as used at JPL [49]. In comparison, the right column presents a planarization based scheme as developed by IBM and used as basis for this thesis work [54]. Illustration is not to scale.

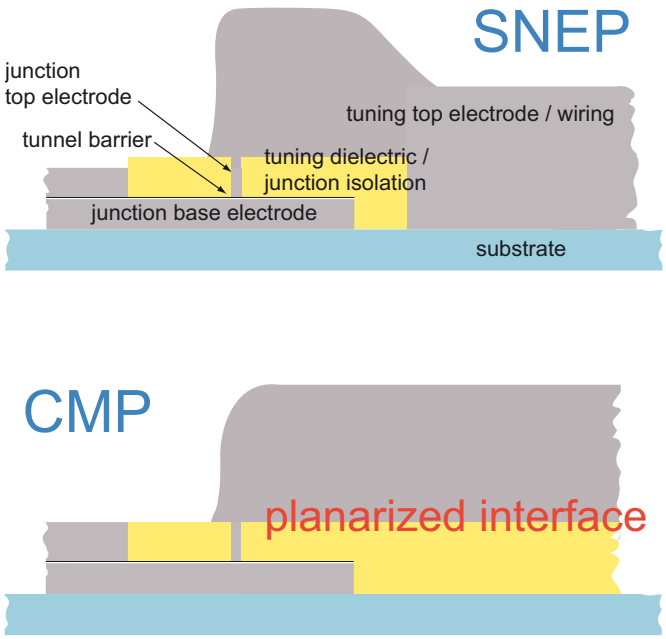


Figure 1.8: Schematic longitudinal section through a standard Nb-Al/Al_2O_3-Nb SIS mixer device. Top section shows a UV-SNEP processed device with confined tuning dielectric area (as processed at KOSMA) and bottom section the result of a CMP based planarization process. The vertical dimension is to scale whereas the horizontal is not.

ium), lift-off and RIE into an underlying thicker, more etch-resistant polyimide layer (Fig. 1.7, middle column). The polyimide then serves as the final junction etch and lift-off mask, and thus substitutes the thick UV photoresist of the standard one-step SNEP. This scheme has been developed to a reliable process for SIS device fabrication down to very small junction areas of 0.1 μm^2. It has the disadvantage that several additional processing steps are required as compared to single-step SNEP [49].

Second is an approach which follows the PARTS (planarized all-refractory technology for low T_c superconductivity [24, 34]) processing scheme (explained in detail in Chap. 4). In contrary to SNEP, PARTS does not require a lift-off step but employs planarization of the dielectric layer with the aid of chemical mechanical polishing (CMP, Fig. 1.7, right column). Here no additional pattern transfer into a thick layer is needed and the junction area is defined with one RIE step from the initially deposited thin etch mask. In contrary to SNEP the dielectric material is deposited onto the whole wafer with the etch mask left in place, covering the free-standing junction pedestals completely. This is followed by the CMP step where the dielectric layer is polished, planarized and thinned until the junction top electrode is cleared for further contacting. During junction clearance the remaining etch mask material is simultaneously removed.

The PARTS scheme has several advantages. Firstly, a planarized interface for subsequent processing is left behind (Fig. 1.8). This is beneficial for deposition of the

wiring layer as it averts step coverage and therewith film discontinuity problems resulting from the topography of already deposited layers. Secondly, the lack of a lift-off step certainly is very helpful at the targeted deeply submicron junction areas as lift-off characteristics generally deteriorate with decreasing feature sizes. In particular, this seemed advantageous for device fabrication of Nb-Al/Al_2O_3-Nb junctions embedded into low-loss tuning circuit material other than niobium. These devices, e. g. the HIFI Band 2 devices are of such a kind, require a more complicated three-step RIE process during junction fabrication. Due to the greater energy input, photoresist etch masks deteriorate during the RIE process and thus make a clean lift-off with complete removal of the remaining residue (e. g. photoresist or polyimide) on top of the junction difficult. Any remaining residue will have a deteriorating effect on mixer RF performance as it hinders both electrical (series RF resistance) and thermal (quasiparticle cooling) contact to the top electrode of the tuning circuit.[22] Last but not least, the pure number of processing steps is lower for the PARTS scheme.

Because CMP needed to be developed as a completely new process for microfabrication at KOSMA, a diploma thesis was initiated prior to this thesis work in order to demonstrate principal feasibility for our small-scale R&D type fabrication [58]. Reassured by these initial results it was then decided to develop a e-beam / PARTS processing scheme at KOSMA in the framework of here presented thesis [60].

In contrary to e-beam junction definition the use of a positive imaging e-beam sensitive photoresist for patterning of the top electrode of the integrated tuning circuit makes a lift-off process very similar to previous photolithographic definition possible. After exposure and development of the top electrode features, the features are defined as holes in the resist layer into which the metalization layer is sputter-deposited into. Subsequently the resist including the metalization layer on top are removed in an organic solvent with only the metalization of the top electrodes remaining on the devices. The definition of the integrated tuning circuit will be explained in detail in Sec. 3.3.

1.5 Organization of thesis

Chap. 2 will give some relevant physics background on SIS junction devices. On the basis of the DC I-V characteristics the underlying tunneling process will be illustrated and important parameters pointed out. Then the functionality of the integrated tuning circuit will be addressed with explanation of the inductive tuning element as well as the impedance matching to the waveguide antenna. In order to complete the picture the antenna and waveguide environment of the SIS mixer device is briefly presented even though this has not been subject of this thesis. Then the requirements to fabrication accuracy will exemplified with the design of the integrated tuning circuits of the SMART 475 GHz devices. Design and fabrication of these devices was the last major task of this thesis work and thus

[22] In hindsight this can be judged as the most important advantage, see HIFI Band 2 related results in Sec. 5.5.2.

fabrication profits from all of the know-how gained during development of the e-beam / CMP process.

Subsequently, the following two chapters present the conducted process development work:

Chap. 3 is dedicated to process development of the e-beam definition of the junction area and the top electrode of the integrated tuning circuit. As junction area definition is the more complicated process and required more development effort, it is predominantly discussed. The established processing parameters for both processes will finally be summarized.

Chap. 4 focuses on the CMP process development. As CMP is a less common process for SIS mixer device fabrication a more thorough introduction to the planarization process is given. In particular, the dependency of the planarization efficiency on several polishing parameters is discussed. Then the polishing setup developed during this thesis is presented. Design and construction of the crucial component wafer carrier as well as the optimization of the process is described. The chapter finishes with a detailed description of operation of the CMP process.

Chap. 5 presents the results, starting with examples from the e-beam definition processes. Standard type Nb-Al/Al_2O_3-Nb as well as embedded trilayer type HIFI Band 2 devices were fabricated and their junction area reproducibility is analyzed. The alignment accuracy of the integrated tuning circuit top electrodes is also discussed. Next are CMP related results. The layout of the latest UV photolithography mask (490EBL) for less critical, large-scale feature definition is visualized in order to exemplify necessary modifications for the e-beam and CMP processes. This mask is used for definition of the 475 GHz SMART devices as well as for definition of backup devices for the HIFI Band 1 (480–640 GHz) SIS mixer devices in collaboration with LERMA[23]. An example for the achieved planarization uniformity is given and then the beneficial impact of the polishing process on the device's DC I-V characteristics is presented. The chapter concludes with a discussion on RF mixer performance. In particular the noise performance of a typical HIFI Band 2 mixer device, which—for reasons given there—relies on standard UV photolithography for the top electrode of the tuning circuit, demonstrates the capabilities of e-beam junction definition.

Chap. 6 discusses the planned improvements to the e-beam and CMP fabrication processes. A roadmap is further presented which points out the processes that additionally need to be developed for fabrication of THz frequency capable SIS devices.

In App. A the complete fabrication process sheet for used for the SMART and LERMA devices is given as reference.

[23]Laboratoire de Radioastronomie, CNRS / Observatoire de Paris. http://www.lra.ens.fr/lra-source/master_fr.html

2

SIS junction devices

In the following a brief introduction to the underlying physics of a SIS tunnel junction shall be given. This will be followed by a discussion of its integrated tuning circuit and the waveguide environment the SIS device is embedded into. Finally, fabrication tolerances will be investigated and exemplified with the tuning circuit design of the 475 GHz SMART devices.

2.1 SIS I-V curve

2.1.1 DC I-V characteristics

A SIS tunnel junction consists of two electrodes of superconducting material which are separated by an insulation layer being thin enough to allow tunneling processes. In the superconducting state, below a material dependent critical temperature T_c, Bose-Einstein condensation takes place[1], during which pairs of electrons are created, the Cooper Pairs [6]. In contrast to the Josephson junctions, which also consist of a tunnel barrier between superconductors, the barrier characteristics of a SIS junction leads to a semiconductor-like, material dependent energy gap structure where the non-paired electrons, the quasiparticles, have no allowable energy states (Fig. 2.1) [83]. The evident singularity in the excited quasiparticle and quasihole superconducting states in the vicinity of the energy gaps at $N_{S1}(\pm\Delta_1)$ and $N_{S2}(\pm\Delta_2)$ is responsible for the steep current rise due to quasiparticle tunneling in the SIS junction's I-V characteristic (Fig. 2.2):

$$N_S(E) = \frac{N_n(\mathscr{E})E}{\sqrt{E^2-\Delta^2}} \approx \frac{N_n(0)E}{\sqrt{E^2-\Delta^2}} \,, \tag{2.1}$$

where $N_n(\mathscr{E})$ is the density of the normal-states which is almost constant $N_n(0)$ (the normal-state density at the Fermi level) for here considered energies [83].

[1] in a classical superconductor

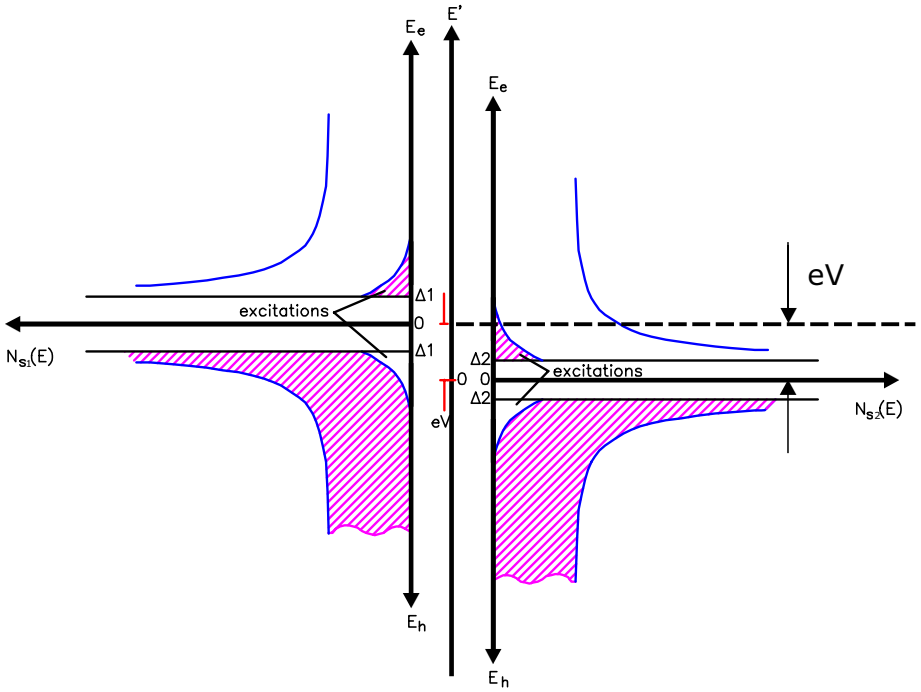


Figure 2.1: Density of states vs. excitation energy in the band model representation of the quasiparticle and quasihole states of the superconductors of a SIS tunnel barrier at a temperature $0\,\mathrm{K} < \mathrm{T} < \mathrm{T_c}[\mathrm{S1}, \mathrm{S2}]$ (generalized case for two different superconductors). The excitation energy is measured positive in both directions. The superconductors with double gap energies $2\Delta_1$ and $2\Delta_2$ are biased at a voltage V with regard to each other.

For energy values E approaching the energy gap Δ, the density of states $N_s(E)$ approaches infinity.

For Nb-Al/Al_2O_3-Nb junctions this onset of quasiparticle tunneling is visible at a bias voltage $2\Delta/e$ which is 2.7–3.0 mV (dependent on fabrication). In contrast, Cooper Pairs can already tunnel through the barrier at $V_{bias} = 0$ (Josephson effects). This tunneling is suppressed during operation of a SIS mixer by a magnetic field, because it generates extra noise [36, 22].

The gap parameter Δ as a function of temperature is numerically computed from the implicit relation, resulting from BCS theory,

$$\frac{1}{N_n(0)\beta} = \int_0^{\hbar\omega_D} \frac{\tanh[(2k_BT)^{-1}\sqrt{E^2+\Delta^2})]}{\sqrt{E^2+\Delta^2)}} d\varepsilon \,, \tag{2.2}$$

where β is the BCS interaction constant and $\hbar\omega_D$ is the Debye frequency ($\gg k_BT_c$) [6]. From Fig. 2.3 it is evident that for $T < T_c/2$ variations from $\Delta(0)$ are small, so that the double energy gap 2Δ can then be approximated to

$$2\Delta \approx 2\Delta(0) = k \cdot 3.52\, k_BT_c \,, \tag{2.3}$$

where, for example, the constant k is ≈ 1 for Nb and ≈ 0.9 for NbTiN, respectively [83]. Niobium thin films have a $T_c = 9.1$ K which suits operation in a LHe

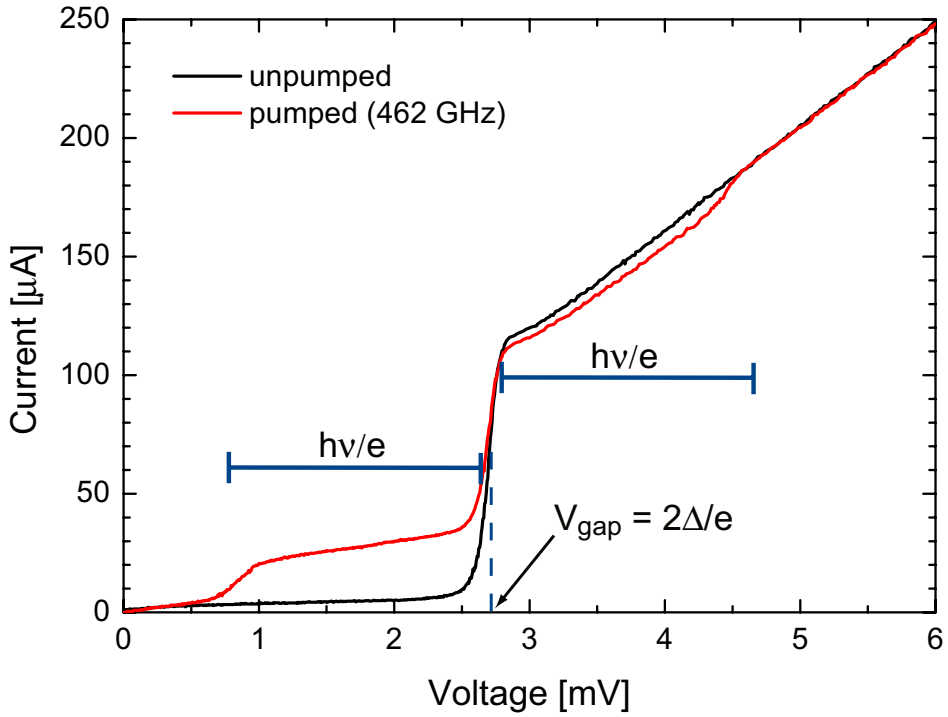


Figure 2.2: Measured unpumped (i. e. no RF power applied) and pumped (i. e. RF power applied) I-V characteristic of a Nb-Al/Al_2O_3-Nb SIS device (UV-SNEP fabrication). The device was measured in a heterodyne receiver setup at 4.5 K with applied magnetic field for Josephson current suppression. The highly nonlinear current rise due to quasiparticle tunneling is clearly visible at $V_{gap} = 2\Delta/e$ as well as the quantum-effect induced modification to the DC I-V characteristic under RF irradiation.

cryostat working near 4.2 K well and ensures a high Δ value which is beneficial for mixer operation: Apart from the gap voltage dependent mixing limit, high V_{gap} values enlarge the possible bias range of the SIS device during heterodyne operation (see next section). V_{gap} can vary due to fabrication influences and besides superconductor material quality it mainly reflects the local temperature of the junction. Investigations concerning mixer performance of Nb junctions embedded into all-NbTiN wiring leads show that quasiparticle heat trapping through Andreev reflection at the superconductor interface can yield significantly elevated barrier temperatures above the bath temperature of the cryostat (≈ 6 K) and thus depression of the gap parameter Δ [16, 50].

In the context of this thesis it is important to stress that contamination of the junction top electrode to wiring interface, e. g. through junction etch mask residue, to a certain extent has the same effect. One important result of this thesis work is a significant improvement of V_{gap} for CMP processed devices, presumably originating from a far cleaner top electrode interface as compared to UV-SNEP devices (see Sec. 5.5.2). This is especially evident for the HIFI Band 2 mixer devices which have a NbTiN base electrode and rely on junction cooling via the top electrode.

The electrodes are separated by a very thin 1-2 nm insulating barrier. Because the critical current density J_c of the SIS junction is a strong function of the barrier thickness h

$$J_c \propto e^{-h} , \tag{2.4}$$

the electrical barrier property is best described through J_c. J_c is set during in-situ[2] thermal oxidation of the aluminum base layer to a predetermined design value by variation of the oxygen partial pressure times exposure duration product [44, 46, 45, 52]. The not well measurable quantity J_c is linked to the area independent $R_N A_J$ product, which can be derived from statistical treatment of all devices on a wafer, via the fundamental equation (see Sec. 5.2.1):

$$J_c = c \ \frac{\pi}{4} \ \frac{V_{gap}}{R_N A_J} . \tag{2.5}$$

Here V_{gap} is the measured device gap voltage, the normal resistance R_N is measured as the slope of the I-V curve for voltages larger than 6 mV [3] and A_J the area of the junction [2, 3]. c is a correction factor taking into account the reduced critical current density for superconductors which show strong electron-phonon-coupling (for niobium $c \approx 0.75$) [30, 83]. For $J_c > 10\,\mathrm{kA/cm^2}$ the Al_2O_3 barriers become increasingly leaky and fabrication yields less reproducible J_c values. Consequently, this sets a practical fabrication limit somewhere between 13 and 17 $\mathrm{kA/cm^2}$ for Nb-Al/Al_2O_3-Nb devices with subgap leakage currents low enough not to adversely affect mixer performance.

The ratio of subgap resistance R_{sg}, calculated from the subgap current at 2 mV, to normal conducting resistance R_N is an important I-V curve property to judge junction quality. A $R_{sg}/R_N > 10$ value is generally judged as good, i. e. leakage current has no big affect on mixer performance, while a value above 15 is excellent. In practice a trade-off between a desirable high J_c value and the resistance ratio must be considered. SIS mixers profit from an as high as possible J_c value with larger J_c resulting into greater power coupling into the junction and thus an increase in sensitivity. For future developments the Al_2O_3 barrier needs to be replaced by AlN for THz device fabrication because it allows significantly higher J_c while retaining constant leakage current, see Sec. 6.5 for further details.

For values $R_{sg}/R_N < 10$, corresponding to a higher subgap (leakage) current I_{sg} of the device, an increasing degradation of mixing performance is observable. I_{sg} can be thought of two parallel conduction channels:

$$I_{sg} = I_{tunnel} + I_{MAR} . \tag{2.6}$$

I_{tunnel} is the tunnel current of the thermally excited quasiparticles and quasiholes. I_{MAR} is a result of the transport of multiply charged quanta through multiple Andreev reflection (MAR) and a result of barrier imperfections, the pinholes. Thus I_{MAR} can be taken as synonymous to junction quality. Detailed analysis of the dependence of I_{MAR} on J_c and its influence on mixer noise has been made for

[2] i. e. without breaking the vacuum during the deposition process of the junction trilayer

[3] The I-V curve closes in asymptotically to a straight line.

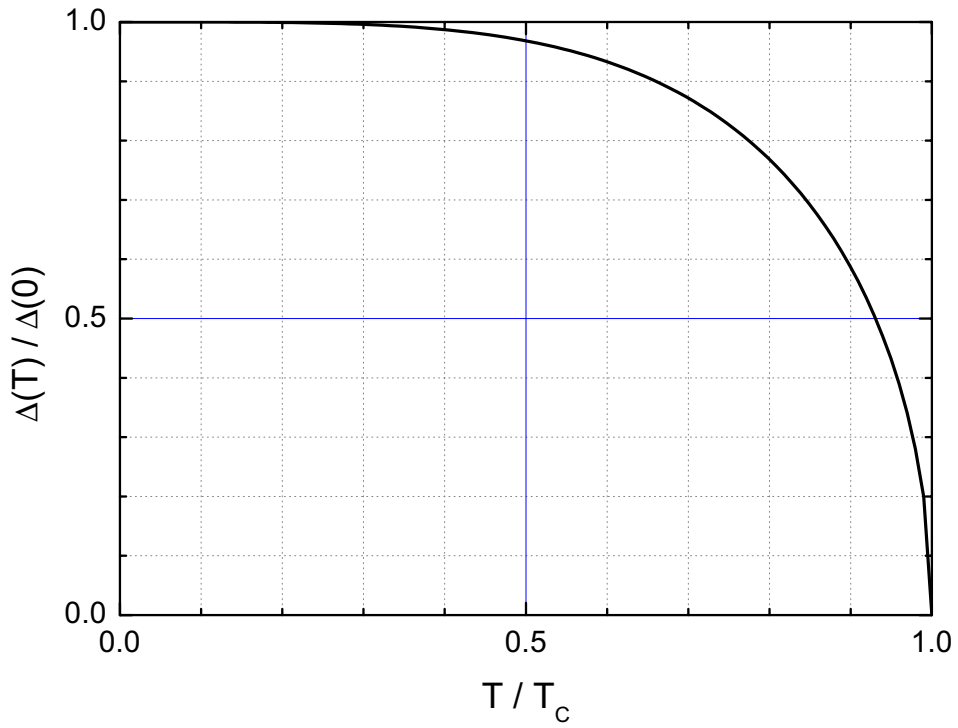


Figure 2.3: Temperature dependence of the superconducting energy gap. Below $T_c/2$ variation of $\Delta(T)$ is negligible.

Nb-Al/Al_2O_3-Nb junctions [15]. It was found that I_{MAR} is several times greater than I_{tunnel} and the main cause for the higher than expected I_{sg} values typically observed for junctions with critical current density around 10 kA/cm^2. Because of the multiple quanta nature of MAR, shot noise generated through a MAR process is higher than for an ordinary tunnel process.

Consequently, the mixer noise temperature T_m is significantly larger than expected from the quantum mixing theory (see next section). If I_{MAR} has a 50% contribution to I_{sg} an increase of the junction shot noise of 63% is calculated, and when the I_{MAR} contribution to I_{sg} increases to 80%, T_m is already doubled [15]. The MAR process is temperature independent and, consequently, further lowering the bath temperature to 3 K during mixer operation only can improve the mixer noise temperature for junctions with high quality barriers. T_m degradation due to higher thermal current through barrier has been judged to be of less importance. For example, it has been measured that a 30% increase in subgap current I_{tunnel} only yields a 2% increase in T_m [16].

The overall "sharpness" of the quasiparticle characteristic, which indicated constant superconductor material characteristics at the barrier, is also critical for the mixing performance [51]. For example, the reactive-ion etch process needed for junction patterning can affect the outer layers of the barrier interface through ion bombardment.

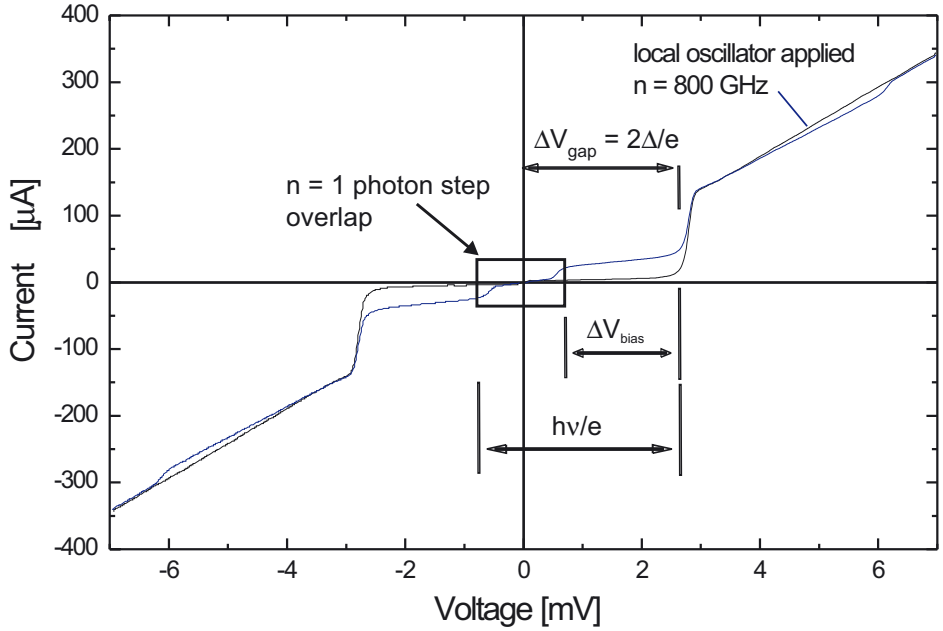


Figure 2.4: Explanation of the the upper mixing limit of a SIS device using the photon step overlap argument. At RF frequencies $> 2\Delta/h$, i. e. the gap frequency, the $n = 1$ photon step from the negative voltage branch of the I-V curve starts to overlap with the positive voltage branch photon step and narrows the possible bias range V_{bias}. A measured pumped I-V characteristic for $\nu = 800$ GHz is displayed.

2.1.2 RF I-V characteristics

Under classical treatment a non-linear element used as frequency mixer should exhibit a switch-like behavior. In order to produce current delta spikes when the operating (bias voltage) point is modulated through incoming RF power this demands an I-V characteristic with a near as possible step-like feature [5]. The quasiparticle current rise of a SIS I-V curve ideally suits these requirements.

Effects which are not classically explainable are visible in the I-V characteristic when a SIS junction pumped, i. e. is irradiated with RF power. The measured I-V curve is modified and photon steps at voltages $V = (2\Delta \pm nh\nu)/e$ for $(n \geq 1)$ are observed [14, 78]. In Fig. 2.2) the two photon steps for $n = 1$ are clearly visible in the pumped I-V characteristic and their width $h\nu/e$ corresponds to the 462 GHz photon energy, i. e. $V_{step} = 1.91$ mV.

Generally speaking, the quantum mixing condition is met when the voltage variation of the non-linearity in a device's I-V curve is much smaller than the photon energy corresponding voltage scale:

$$\Delta V_{gap} \ll h\nu/e \tag{2.7}$$

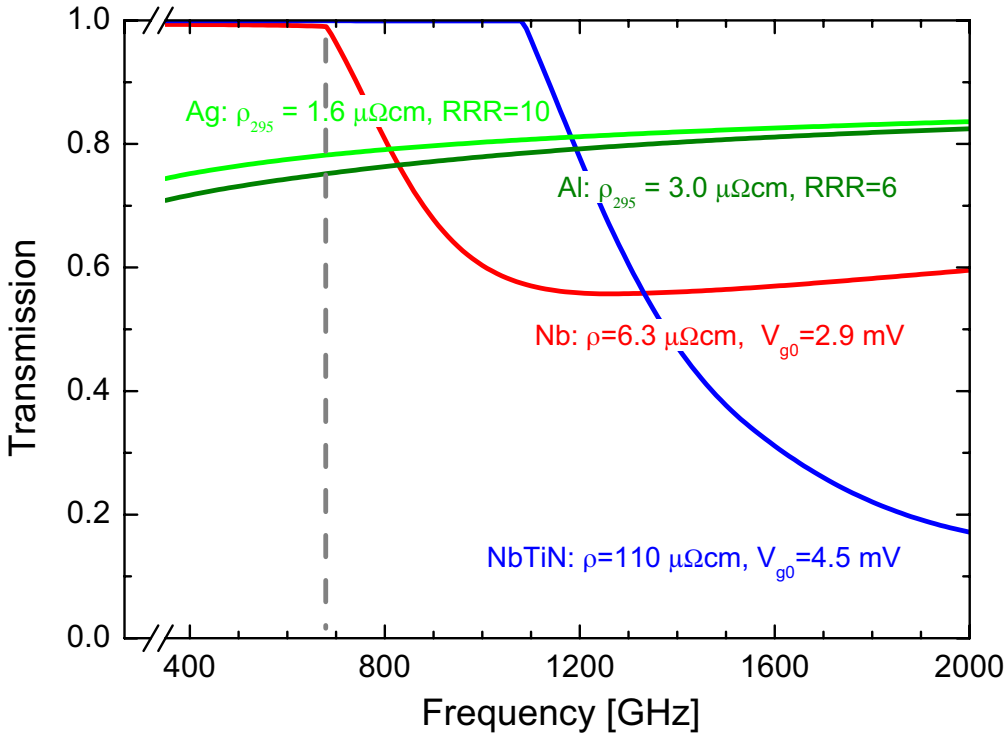


Figure 2.5: Comparison of relative power transmission through a quarter wavelength microstrip lines consisting of Ag, Al, Nb or NbTiN. The Nb gap voltage at approx. 690 GHz is marked and clearly reflected in the trace. Curves have been calculated with Mattis-Bardeen theory for the material parameters given: RRR is the residual resistance ratio, V_{g0} the extrapolated gap voltage at 0 K and ρ the thin film resistivity at 20 K).

An analytical theory for quantum mixing was developed by Tucker in 1979 and is the basis of all SIS mixer analysis [81, 82]. The two most important findings of the theory are:

1. quantum limited sensitivity[4]: $T_m = h\nu/k$ (DSB)
2. positive mixer gain achievable[5]: $G_m > 1$

In principle, quasiparticle mixing is theoretically possible up to the double gap frequency $4\Delta/h$ of the SIS junction which about 1.4 THz for Nb-Al/Al_2O_3-Nb devices. This can be illustrated with the photon step overlap argument and Fig. 2.4: For frequencies $> 2\Delta/h$ the $n = 1$ negative voltage branch photon step starts to overlap with the positive voltage branch photon step and cancels out the quasiparticle current. As a consequence the available bias voltage range for device

[4]The sensitivity, expressed by the noise temperature T_m, is referred to the input of a double sideband (DSB) mixer. Each sideband contributes $h\nu/2k$ noise due to input photon (zero-point) fluctuations, i. e. for an ideal quantum mixer the mixing process itself does not contribute any noise [41]!

[5]In this regime it is difficult to get stable mixer performance due to biasing conditions. Thus a $G_m > 1$ condition is not used for receiver operation.

frequency range [GHz]	tuning circuit material	junction material
$\nu \leq 700$	Nb / Nb	Nb-Al/Al_2O_3-Nb
$700 < \nu < 1200$	NbTiN / Nb or NbTiN / Al	Nb-Al/Al_2O_3-Nb
$1200 < \nu < 1400$	Al / Al or NbTiN / Al	Nb-Al/AlN-NbTiN
$1400 < \nu < 1900$	Al / Al	Nb-Al/AlN-NbTiN or NbTiN-Al/AlN-NbTiN

Table 2.1: Summary of optimum tuning and junction material combinations for different frequencies. Since fabrication influences thin film resistivity and T_c (NbTiN) the best material choice has partly to be empirically evaluated for frequencies near the given limits.

operation is reduced:

$$h\nu/e - V_{gap} < \Delta V_{bias} < V_{gap} \tag{2.8}$$

At a frequency $4\Delta/h$ the photon steps completely overlap, canceling out all quasiparticle current. For niobium junctions feasible bias voltages limit the upper operating frequency to about:

$$V_{bias}^{limit}(\text{Nb junctions}) = 1.2\,\text{THz} . \tag{2.9}$$

Photons with energies greater than 2Δ have enough energy to break up the binding energy of the Cooper pairs and thus the superconductor material becomes lossy. In particular, the RF losses in the integrated tuning circuit electrodes then cause a significant increase of mixer noise temperature. With knowledge of the material quality for fabricated thin film microstrip lines, the resulting RF losses can be calculated in good approximation through the Mattis-Bardeen theory (Fig.2.5) [53]. For the design of SIS mixers this has implication for the material choice of the integrated tuning circuit for which a low loss conductor is essential.

Tab. 2.1 sums up the best material combinations of junction and tuning circuit for readily available thin films. Below the gap frequency of niobium, which is typically around 690 GHz for thin films, pure niobium tuning electrodes deliver optimum performance with very low RF losses. For higher frequencies niobium is gradually replaced. Notably, the normal conductor aluminum is the best material choice for high frequency tuning circuits because its thin films do not corrode as easily as silver does and because of its compatibility to junction fabrication.

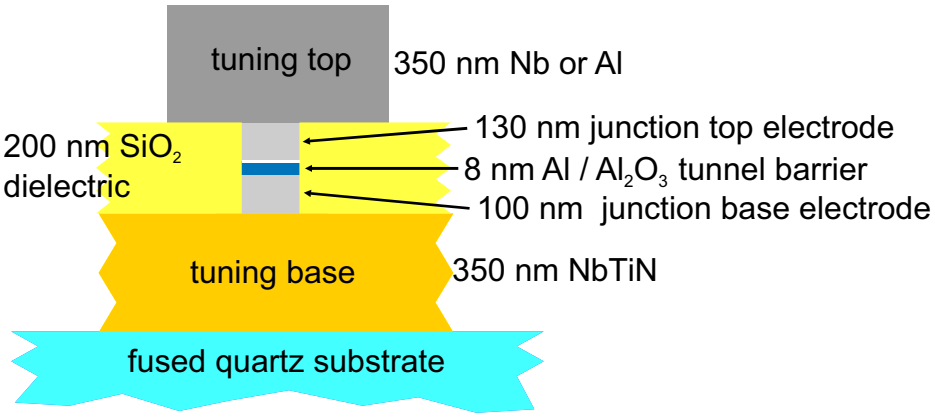


Figure 2.6: Schematic cross-section through a HIFI Band 2 SIS device. The Nb-Al/Al_2O_3-Nb junction is embedded into a NbTiN-Nb or NbTiN-Al tuning circuit [19].

As pointed out in Tab. 2.1 at present 1.9 THz is the absolute theoretical limit for frequency mixing for a SIS device with hybrid Nb and NbTiN junction electrodes.[6] Devices which use different material for the tuning circuit as for the junction electrodes, require more complicated processing which embeds the junction layers. For example, the HIFI Band 2 mixer devices presented later on are of such kind and embed standard Nb-Al/Al_2O_3-Nb junctions either into NbTiN-Nb or NbTiN-Al tuning circuits (Fig. 2.6).

[6] Good NbTiN-Al/AlN-NbTiN junctions have not been fabricated up to date and alternative tunnel barrier compatible, higher T_c materials are not in sight.

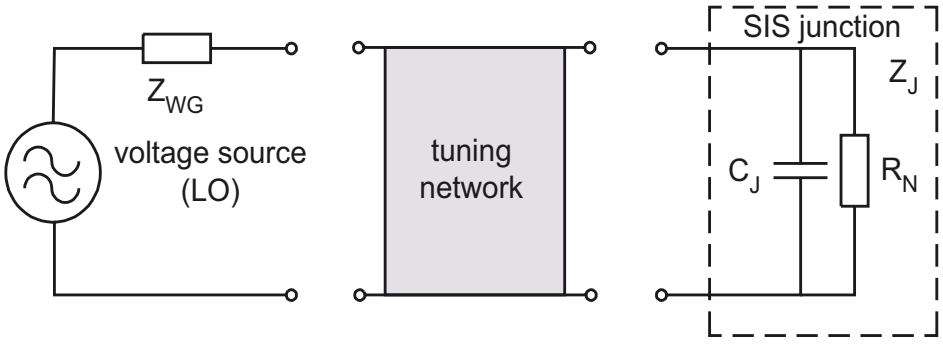


Figure 2.7: Equivalent circuit for the voltage source (LO), SIS junction and tuning network for a series tuning network. The waveguide impedance Z_{WG} is matched to the junction impedance Z_J with the help of a tuning network. Illustration modified from [33].

2.2 Impedance matching of junction to waveguide

All devices fabricated in this thesis work are designed for a waveguide-based environment for feeding the signal and local oscillator power to the junction, thus following discussion focuses on matching the junction to the waveguide impedance. In general, though, all statements given are also valid for quasi-optical setups.

Optimum SIS mixer performance can only be achieved when the power source, i. e. the local oscillator and astronomical signal, is transmitted with low RF losses. Expressed in electrical terms of an equivalent circuit, the complexed numbered junction load impedance Z_J has to be conjugately matched to the complex waveguide source impedance Z_{WG} which is connected in series to the ideal voltage source (Fig. 2.7). The equivalent circuit of a SIS junction is a parallel connection of a RF tunnel resistance R_N (approx. equivalent the measurable normal resistance) and a large parasitic capacitance C_J. SIS junctions of high critical current density $J_c = 10\text{–}17\,\mathrm{kA/cm^2}$ have a specific capacitance of approx. $c_{sp} = 90\,\mathrm{fF}/\mu\mathrm{m}^2$.

The SIS junction load impedance then calculates to:

$$\begin{aligned} \frac{1}{Z_J} &= \frac{1}{R_N} + i\omega C_J \\ \Longleftrightarrow Z_J &= \frac{R_N}{1+(\omega R_N C_J)^2} - i\frac{R_N(\omega R_N C_J)}{1+(\omega R_N C_J)^2} \ . \end{aligned} \tag{2.10}$$

The power transfered by a RF voltage V_0 then is

$$\mathrm{P} = \frac{V_0^2}{(Z_J+Z_{WG})^2} Z_J \ , \tag{2.11}$$

and is maximized when

$$Z_{WG}^* = Z_J \ , \tag{2.12}$$

i. e. when the junction impedance becomes complex conjugated to the waveguide impedance. To achieve this over a certain RF bandwidth, the Z_J must be transformed by an integrated microstrip tuning circuit.

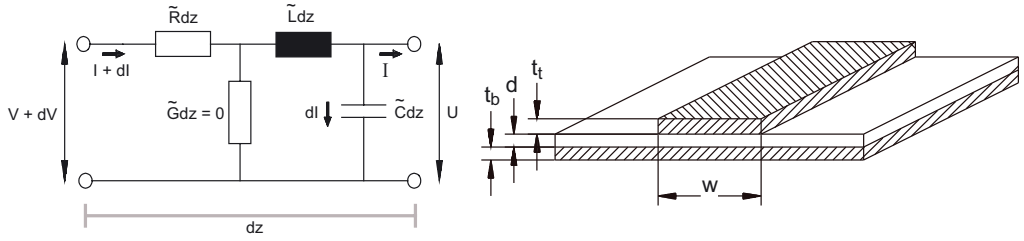


Figure 2.8: Representation of a stripline by its complex valued series impedance and parallel admittance per unit length (left) and geometrical realization (right). Illustration modified from [33].

2.2.1 Integrated tuning circuits

Fig. 2.7 illustrates that both the reactive and the resistive component of the SIS junction's impedance Z_J need to be matched to the source impedance Z_{WG} of the waveguide with the help of an integrated tuning circuit. The main problem is the large geometrical capacitance of the junction. This can be compensated either with a parallel or a series inductance as in Fig. 2.7. Common parallel inductor types are open stub, shorted stub or radial stub [27, 33]. Series inductor types are end-loaded stubs and three-step transformers. The latter additionally includes two $\lambda/4$ segments for broadband real impedance transformation and have been used on many KOSMA devices. Additionally, more complicated antisymmetric tuning circuits have been developed which incorporate a mixture between both parallel and series type [91]. These use twin-junction designs, which additionally can be asymmetrically driven for waveguide application [7]. The tuning circuits are integrated into junction fabrication and are constructed as planar microstrip circuits which will be briefly introduced in the following.

Microstrip transmission line impedance

In principle, a microstrip transmission line is described as a distributed electrical element on which an electromagnetic wave can propagate. Herewith a thin and narrow conductor of thickness t_t and width w is insulated by a thin dielectric layer of thickness d from an extended conducting ground plane of thickness t_b (Fig. 2.8). This geometry confines most of the electromagnetic field of the wave to the cross-section wd between the conducting layers. In order to quantify the frequency, (superconductive-)material and geometry dependent properties of such a microstrip line the complex values characteristic impedance Z_C and the propagation constant γ need to be calculated with help of the surface impedance Z_S. Here Z_C is the voltage to current ratio for the traveling wave and γ its wave vector.

They are defined as [28]:

$$\gamma = \alpha + i \cdot \beta = \sqrt{ZY} \tag{2.13}$$

and

$$Z_C = \sqrt{Z/Y}, \tag{2.14}$$

with the attenuation constant α, the phase constant β, the series impedance per unit length $Z = \tilde{R} + i \cdot \omega\tilde{L}$, the shunt admittance per unit length $Y = \tilde{G} + i \cdot \omega\tilde{C}$. $\tilde{R}$, $\tilde{G}$, $\tilde{L}$ and $\tilde{C}$ are defined in Fig. 2.8.

The series impedance Z contains a contribution from the inductance of the field between the conductors (first term) and a contribution from the surface impedance of the conductors (second term) [38]:

$$Z = i \cdot \omega\mu_0 \frac{d}{w} + \frac{1}{w}[Z_S(t_t) + Z_S(t_b)] \; . \tag{2.15}$$

If the dielectric is assumed to be lossless $\tilde{G} = 0$, e. g. this is approximately valid for SiO_2 at submillimeter wavelengths, the shunt admittance then reduces to the capacitance per unit length:

$$Y = i \cdot \omega\varepsilon_r\varepsilon_0 \frac{w}{d} \; . \tag{2.16}$$

The surface impedance Z_S is:

$$Z_S(\omega) = \sqrt{\frac{i\omega\mu_0}{\sigma_{MB}}} \coth(\sqrt{i\omega\mu_0\sigma_{MB}}t_t) \; , \tag{2.17}$$

with the thickness of the conductor t and superconductor's conductivity σ_{MB} being the frequency dependent numerical solution of the Mattis-Bardeen equations in the "extreme anomalous limit". This approximation has shown to be sufficiently precise for niobium electrodes of thickness $t \geq 150\,\text{nm}$ [10].

Several small correction terms are used for more precise calculation of the series impedance Z and account for the real geometry of a tuning circuit. Principally, above formulas stay valid and some parameters are exchanged for more complicated expressions which are listed below [27, 33]:

1. fringing effects ([12]):
   $1/w \longrightarrow 1/(w \cdot k_f(w,d,t_t,\varepsilon))$ ($k_f > 1$) in first term of Eq. 2.15
2. effects of current distribution ([89]):
   $1/w \longrightarrow 1/(w \cdot k_l(w,d,t_t,\varepsilon))$ in second term of Eq. 2.15
3. correction for dielectric interface ([23]):
   $\varepsilon_r \longrightarrow \varepsilon_{eff}(w,d,t_t,\varepsilon_r)$ effective dielectric constant

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12\frac{d}{w}}} - \frac{\varepsilon_r - 1}{4.6} \frac{t_t/d}{\sqrt{\frac{d}{w}}} \tag{2.18}$$

Additionally, the constriction of current flow at boundaries must be considered [31]. The step inductance including an empirical factor 2 for superconductors is given by:

$$Z_{step} = 2 \cdot \frac{i\omega t_t \mu_0}{\pi} \ln\left[\sin\left(\frac{\mathrm{Re}(Z_{C1})\mathrm{Re}(v_2)}{\mathrm{Re}(Z_{C2})\mathrm{Re}(v_1)} \frac{\pi}{2}\right)^{-1}\right] \; , \tag{2.19}$$

where $i = 1,2$ denote the two microstrips with different widths w_i ($w_1 > w_2$), and Z_{Ci} and $v_i = \omega/\mathrm{Im}(\gamma)$ the characteristic impedances and phase velocities, respectively.

Therewith the impedance transformation properties of a microstrip line of characteristic impedance Z_C and length l can be calculated:

$$Z_{trans}(Z_C, Z_{load}, \gamma, l) = Z_C \frac{Z_{load} + Z_C \coth(\gamma l)}{Z_C + Z_{load} \coth(\gamma l)} \; . \tag{2.20}$$

Z_{trans} is the transformed load impedance Z_{load} at the input of the microstrip line looking toward the load. For example, the three-step tuning circuits which are used for the 475 GHz SMART devices (see Sec. 2.3) are composed of three microstrip line segments and require calculation of the transformation in successive order. Calculation starts with the impedance transformation of $Z_{load} = Z_J$, with Z_C being the characteristic impedance and l being the length of the first transmission line as seen from the junction.

Following summarizes the steps needed for design of a three-step transformer integrated tuning structure on basis of Eq. 2.20:

1. The compensation of junction capacitance is achieved through a stripline with an characteristic impedance $Z_C \gg Z_J$. For a short, lossless microstrip line ($\alpha = 0$) Eq. 2.20 can then be approximated to:

$$Z_{trans}(l) \approx Z_J + i \cdot Z_C \tan(\beta l) \tag{2.21}$$
$$\approx Z_J + i \cdot Z_C \beta l \; . \tag{2.22}$$

   The line segment at the junction ($i = 1$, Fig. 2.12) of a three-step transformer is such an inductive element. As a result of this transformation Z_{trans} is real.

2. The transformation of a real load impedance Z_{load} value to any desired value Z_{trans} can be attained for one frequency with a quarter wavelength, low loss stripline $l = \lambda/4$ of characteristic impedance:[7]

$$Z_C = \sqrt{Z_{trans} \cdot Z_{load}} \; . \tag{2.23}$$

   This property is used for the remaining two microstrip line segments ($i = 2,3$, Fig. 2.12).

RF bandwidth limitation

Tuning of the junction capacitance as well as matching of junction normal resistance can only be obtained across a certain RF frequency band around the design frequency. The integrated tuning circuit is the input RF bandwidth limiting component of a SIS heterodyne receiver. For a simple tuning network with a single

[7] Losses in the microstrip line modify the required length.

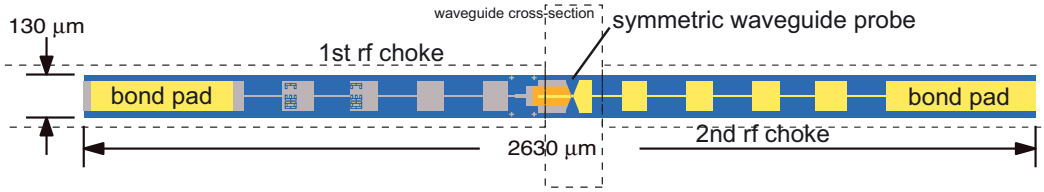


Figure 2.9: Illustration of a 475 GHz SMART waveguide SIS mixer device (symmetric probe version). Vertical view down onto the the device as positioned in a mixer block. The dashed lines point to the waveguide cross-section and substrate channel features of the mixer block. Dimensions of the fused quartz substrate are given. Drawing is to scale.

junction the mixer input bandwidth B is directly related to the junction properties R_N and C_J and the operating angular frequency ω [40]:

$$B \propto \frac{1}{\omega R_N C_J} \,. \tag{2.24}$$

Subsequently, an as low as possible denominator, i. e. the Q parameter, has to be designed through appropriate junction properties in order to achieve broadband tuning circuits. While the $R_N C_J$ product is not junction area dependent, with Eq. 2.5 the product is $\propto 1/J_c$ and thus demands high critical current densities. On the other hand, the waveguide probe impedances have real parts between 20 and 50 Ω. The closer the junction R_N lies to these values, though, the larger the fractional input bandwidth of the tuning circuit becomes [22]. But as $R_N \propto J_c/A_J \simeq const$. this has the consequence that SIS devices must additionally have submicron junction areas. With a set input bandwidth specification, e. g. typically 20–30%, an increase in operating frequency necessitates reduction of A_J as well as increase of J_c [39]. Both variables A_J and J_c are limited by fabrication capabilities. As mentioned in Sec. 2.1.1 J_c is limited to values $< 20\,\mathrm{kA/cm^2}$ for Al_2O_3 barriers. The minimal junction area is determined by the lithography process employed and, of course, is the focus of this thesis work.

2.2.2 Waveguide environment of 475 GHz SMART devices

For operation in a heterodyne receiver the SIS mixer device is placed into the waveguide environment which is called the mixer block. At KOSMA very robust and wideband fixed-backshort waveguides have been developed and these are employed for all frequencies above 400 GHz [25, 27]. The mixer blocks are fabricated in house on a NC lathe to 5 μm precision. Fig. 2.9 illustrates the position of the device in the mixer block. The dashed lines mark the substrate channel features into which the device is glued as well as the waveguide onto which the waveguide probe of the device has to be centered. For precise alignment of the device a micromanipulator is used which provides sub 10 nm motion resolution.[8]

[8] Klocke Nanotechnik. http://www.klocke-nanotechnik.de

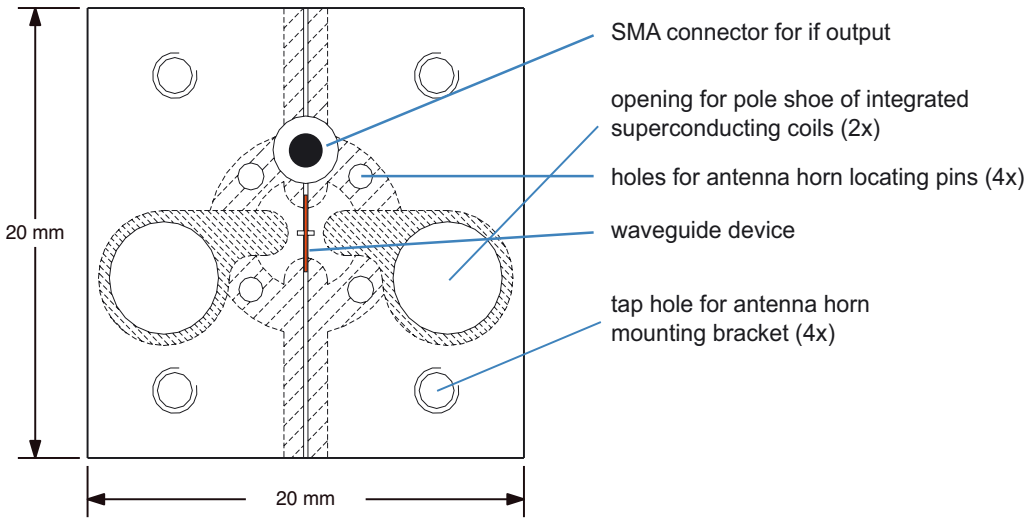


Figure 2.10: Front view of a KOSMA fixed-backshort mixer block for SMART. The SIS device is glued into the substrate channel of the mixer and thereby centrally positioned onto the waveguide. The coaxial SMA connector feeds the IF signal to the first HEMT amplifier as well as supplies the bias voltage. The integrated magnets are for suppression of the Josephson effects. During operation a horn antenna is flanged onto the front of the mixer block, hence holes for locating pins can be seen for centering. The copper mixer block has the outer dimensions $20\times20\times10\,\mathrm{mm}^3$ [27].

The regular features outside of the waveguide area in Fig. 2.9 define the superconducting top electrode of the RF choke features. The electrode is fabricated together with the rest of the device and, together with the fused quartz substrate as dielectric layer and the mixer block as the ground plane, is a microstrip line. In principle, they function as low-pass filters for the IF signal and they reject the RF signal back into the waveguide. The thickness of the substrate is crucial as otherwise the RF signal leaks through. The 475 GHz devices, e. g., are designed for a $50\,\mu$m thick quartz substrate and, as with every waveguide-based mixer, require careful backlapping of the substrate.

The frequency dependencies of the waveguide and waveguide probe as well as the RF choke impedances are simulated with a 3d EM field simulator software package (CST Microwave Studio™).[9] In contrast to prior used scale model measurements, i. e. a 300:1 replica of the mixer block is built and characterized with a network analyzer, the 3d models now are sufficiently close enough to reality and enable much faster design [79, 80]. Optimum design requires a waveguide impedance with as low as possible real ($Z_{WG} < 50\,\Omega$) and only a small imaginary part with low frequency dispersion over the whole RF bandwidth in order to reduce the impedance transformation demands on the integrated tuning circuit.

Fig. 2.10 shows a drawing of the mixer block front. The device is electrically contacted at the bond pad areas through ultrasonic bonding of $25\,\mu$m diam. aluminum wires to the ground side (mixer block) and to the SMA coaxial connector

[9] http://www.cst-world.com

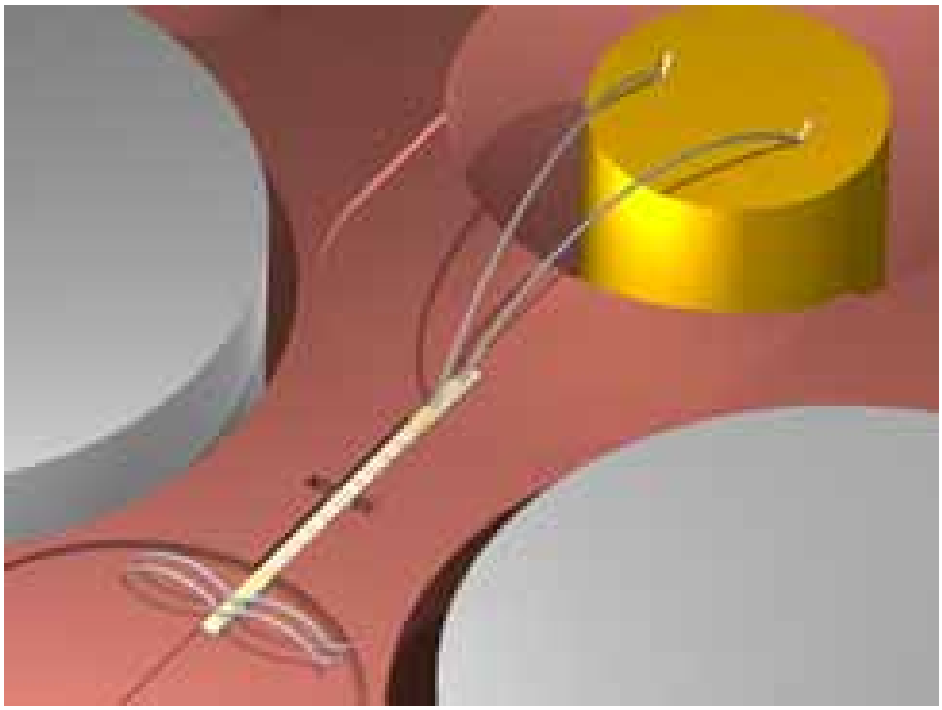


Figure 2.11: View of a 3d model of a KOSMA waveguide mixer block from Fig. 2.10. Rendered image by Michael Schultz [66].

at the top. This connector feeds the IF signal to the IF amplifiers while simultaneously providing the DC bias voltage to the device. The pole shoes of the integrated superconducting coils are needed for suppression of the Josephson effect. In Fig. 2.11 a rendered view of the mixer block front is given. The horn, which is flanged onto the front of the mixer block for matching of the free-space impedance of the incoming EM wave to the waveguide impedance, has been omitted in these figures.

2.3 Design of 475 GHz SMART devices

In this section the design of integrated tuning circuits is exemplified with the 475 GHz SMART devices which are an essential element of the 490EBL mask. These devices will mainly be used for astronomical observation of the rotational transition of CO ($J = 4 \rightarrow 3$) at 461 GHz and the fine-structure transition of neutral carbon C I ($^3P_1 \rightarrow ^3P_0$) at 492 GHz and thus require broadband tuning circuits.

A discussion on how fabrication tolerances influence simulated device performance is conducted and therewith the harsh requirements to SIS device fabrication already given in Sec. 1.3 are motivated. This then, consequently, will lead to presentation of the new e-beam definition based fabrication process in the following chapters.

The 475 GHz SMART devices are standard Nb-Al/Al_2O_3-Nb devices with all-

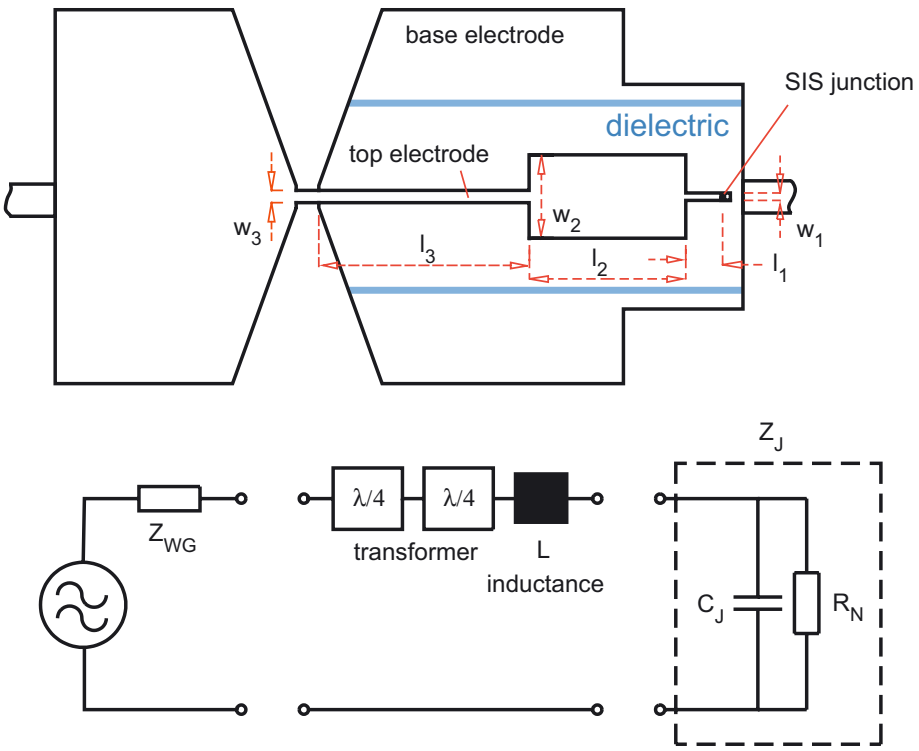


Figure 2.12: Principal mask layout of a three-step transformer (top) and its equivalent circuit (bottom). Top image additionally describes the terminology used for the lengths and widths of the tuning circuit elements. The right feed of the waveguide bow-tie antenna doubles as base electrode of the integrated tuning circuit. Illustration modified from [33].

Nb tuning structures which is this best proven material combination for this frequency band. The design is partly based on the 490 GHz devices already used at the Gornergrat observatory and in receivers at the Heinrich Hertz telescope in Arizona [27]. All devices employ a well-proven, large RF input bandwidth three-step transformer tuning circuit with one inductive and two $\lambda/4$ transformer segments (Fig. 2.12). Some modifications are required to the old waveguide probe and RF choke design, though, because of a change of the dielectric material used for the tuning circuits. As will be explained in Sec. 4.2.1, previously used SiO deposition process does not yield films which are mechanically robust enough for the CMP planarization process. Thus SiO_2 is used as dielectric material but due to its lower ε_r (3.8 vs. 5.7) the microstrip line lengths increase and make longer tuning circuit base electrode necessary. A new symmetric waveguide probe was designed and optimized with the help from the CST software by Thomas Tils [80]. In advantage to previous designs, a newly developed asymmetric waveguide probe design, which results from HIFI Band 2 device development, is additionally used for half of the devices. This probe yields an even lower input impedance for the tuning circuit of around 40 Ω (as compared to roughly 60 Ω for the symmetric probe) at a center frequency of 475 GHz. Tab. 2.2 sums up the mixer block related parameters.

waveguide	type	half height
	cross-section	540 µm ×135 µm
	backshort	200 µm
substrate channel	dimensions	175 µm wide 100µm deep
substrate	material	fused quartz, ε_r = 3.8
	dimensions	130 µm wide 50 µm thick

Table 2.2: Summary of important mixer block design parameters used for 475 GHz SMART devices [80]. The backshort length is the distance between the top of the device (metalization) and the backshort wall.

2.3.1 Initial device parameters

Several design parameters have to be predetermined before the calculation of the microstrip line segments of the integrated tuning circuit can be carried out. First of all, the impedances of the termination loads at both ends, i. e. the junction impedance $Z_J(\nu)$ and the waveguide impedance $Z_{WG}(\nu)$, are required. $Z_{WG}(\nu)$ is calculated with the CST software and shall not be further discussed. $Z_J(\nu)$ is dependent on the variables junction area A_J, critical current density J_c and specific capacitance c_{sp} whose values are constricted by fabrication (as explained in Sec. 1.3 and Sec. 2.1.1). The 475 GHz SMART devices have junction design areas of 0.64 or 0.81 μm^2 because the new e-beam junction area definition process can reproducibly fabricate these values within the limits discussed later on in Sec. 2.3.3.

Due to the e-beam process the junction areas are centered at smaller values than with previous UV photolithography-based fabrication (which also included 1 μm^2 junctions). This is beneficial for device design and therefore somewhat improved mixer performance can be expected. The critical current density J_c is set to 14 kA/cm^2 which, as experienced for fabrication undertaken at KOSMA, can be reproducibly achieved while still yielding high quality DC I-V characteristics. In correspondence to past analysis of mixer performance, the specific capacitance c_{sp} for such a J_c is taken to be 90 fF/cm^2.

Also the thickness and material parameters of the tuning circuit layers are required for calculation of the microstrip surface impedance $Z_S(\nu)$ via the Mattis-Bardeen theory in the extreme anomalous limit approximation [53]. The Mattis-Bardeen calculations will not be explained in detail at this place but can be found in [33, 27]. In compliance with fabrication constrictions, e. g. enabling clean lift-off of the metalization layers, the niobium base and top electrodes are 150 nm and 350 nm thick, respectively. These are standard values for KOSMA SIS mixer devices and there is no need to adjust these for the newly developed fabrication scheme. The niobium material thin film properties needed are the normal con-

ductivity σ_n (niobium film quality), critical temperature T_c and double energy gap at operating temperature of device 2Δ. These values are obtained through van der Pauw (four point) measurements of niobium thin films deposited simultaneously with the device films and need to be checked on a regular basis.[10] The calculation procedure is summarized in the following, together with the values used for device design:

1. determine current normal conductivity of niobium thin films:
   $\sigma_n = 2.0 \cdot 10^7\,\Omega^{-1}\mathrm{m}^{-1}$ (non-device film)

2. measure T_c for same film:
   $T_c = 9.1\,\mathrm{K}$

3. determine double energy gap 2Δ from FTS[11] measurements of latest mixers (point of onset of significant mixer conversion loss) at desired operating temperature of device in receiver:
   $2\Delta(4.3\,\mathrm{K})/h = 691\,\mathrm{GHz}$[12]

4. calculate $Z_S(\nu)$ in 5 GHz intervals for desired frequency band

Due to processing influences, e. g. film growth on top of the dielectric layer, the niobium material of the top electrode has a deteriorated σ_n. Two different reduced values values for σ_n are therefore used during calculation of the tuning circuits: 1.8 and $1.9 \cdot 10^7\,\Omega^{-1}\mathrm{m}^{-1}$. Finally, the dielectric layer properties are set to 200 nm thick SiO_2 with $\varepsilon_r = 3.8$ and no dielectric losses are considered during calculation. In Tab. 2.3 relevant parameters are summarized.

2.3.2 Calculation and optimization of integrated tuning circuit

In the following a short synopsis of the calculation procedure of the integrated tuning circuits is given. At KOSMA the integrated tuning circuits are designed with the ABCD matrix formalism using Mathcad software.[13] Based on the knowledge of the termination impedances $Z_{WG}(\nu)$ and $Z_J(\nu)$ and the other parameters given in Tab. 2.3 the characteristic impedance Z_{Ci} and the transformation properties of each microstrip segment can be simulated. The junction is treated as a lumped element and, consequently, current 2d effects in the junction periphery are not included in the simulation.[14] The frequency dependent power coupling to the junction is calculated and optimized for the targeted frequency band through

[10] The parameters are mainly dependent on sputter target quality and background pressure of the deposition equipment.

[11] Fourier Transform Spectrometer

[12] 4.3 K is the typical operating temperature of a mixer in a Gornergrat receiver with closed-cycle refrigeration.

[13] http://www.mathcad.com

[14] At THz frequency this will not be a good simplification anymore and an additional correctional series inductor must be included into the transformation.

junction	J_c	14 kA·cm^{-2}
	c_{sp}	90 fF·µm^{-1}
	A_J	0.81 and 0.64 µm^2
tuning circuit electrodes	Nb	σ_n = (1.9, 1.8)·10^7 Ω^{-1}·cm^{-1}
		T_c = 9.1 K
		$2\Delta_0$ = 2.93 meV
	base electrode	150 nm
	top electrode	350 nm
tuning circuit dielectric	SiO_2	ε_r = 3.8
	thickness	200 nm

Table 2.3: Initial parameter set used for design of the 475 GHz SMART tuning circuits.

variation of the widths w_i and lengths l_i of the top electrode microstrip segments ($i = 1, 2, 3$).

The segments are treated as a series of one dimensional transmission lines which is a proven approach for these frequencies. However care is taken not to design segments which have dimensions $l_i \leq w_i$ and as a rule $l_i \geq w_i$ is applied in order to minimize 2d effects (the step discontinuities are included, see Eq. 2.19). Starting from scratch, the easiest way for calculating and optimizing a three-step transformer circuit is to begin with the most critical microstrip line which is the inductor segment needed for junction capacitance tuning. In case of UV photolithography and lift-off definition, which is used during definition of the top electrode of the tuning circuit, fabrication tolerances (definition reproducibility and overlay alignment accuracy) yield a practical lower limit for the widths w_i of the microstrip lines of 2.5 μm. The microstrip line dimensions are then iteratively optimized.

In Fig. 2.13(top) the simulated impedance variation for a SMART device with tuning circuit `490ebl_sp_bs200_A064_sn_19_mod` (see Tab. B.1 in App. B) is exemplified in a Smith chart plot. The corresponding power coupling (i. e. RF power into junction) curve is given in Fig. 2.13(bottom). The simulated power coupling stays above the baseline requirement of 95% for a sufficiently wide frequency band centered onto 460 and 490 GHz. In order to compensate for possible fabrication induced shifts of the band center position of the tuning circuit, e. g. due to varying σ_n, an additional 10 GHz roll-off is left on either edge before power coupling is allowed to decrease significantly.[15]

Tab. B.1 in App. B sums up the tuning circuits designed for the 490EBL mask. Besides the dimensions of of the microstrip lines, the columns P(460) and P(490) denote the power coupling to the junction as calculated with the ABCD matrices for-

[15] As with any RF circuit a general trade-off between maximum power coupling and bandwidth is observed.

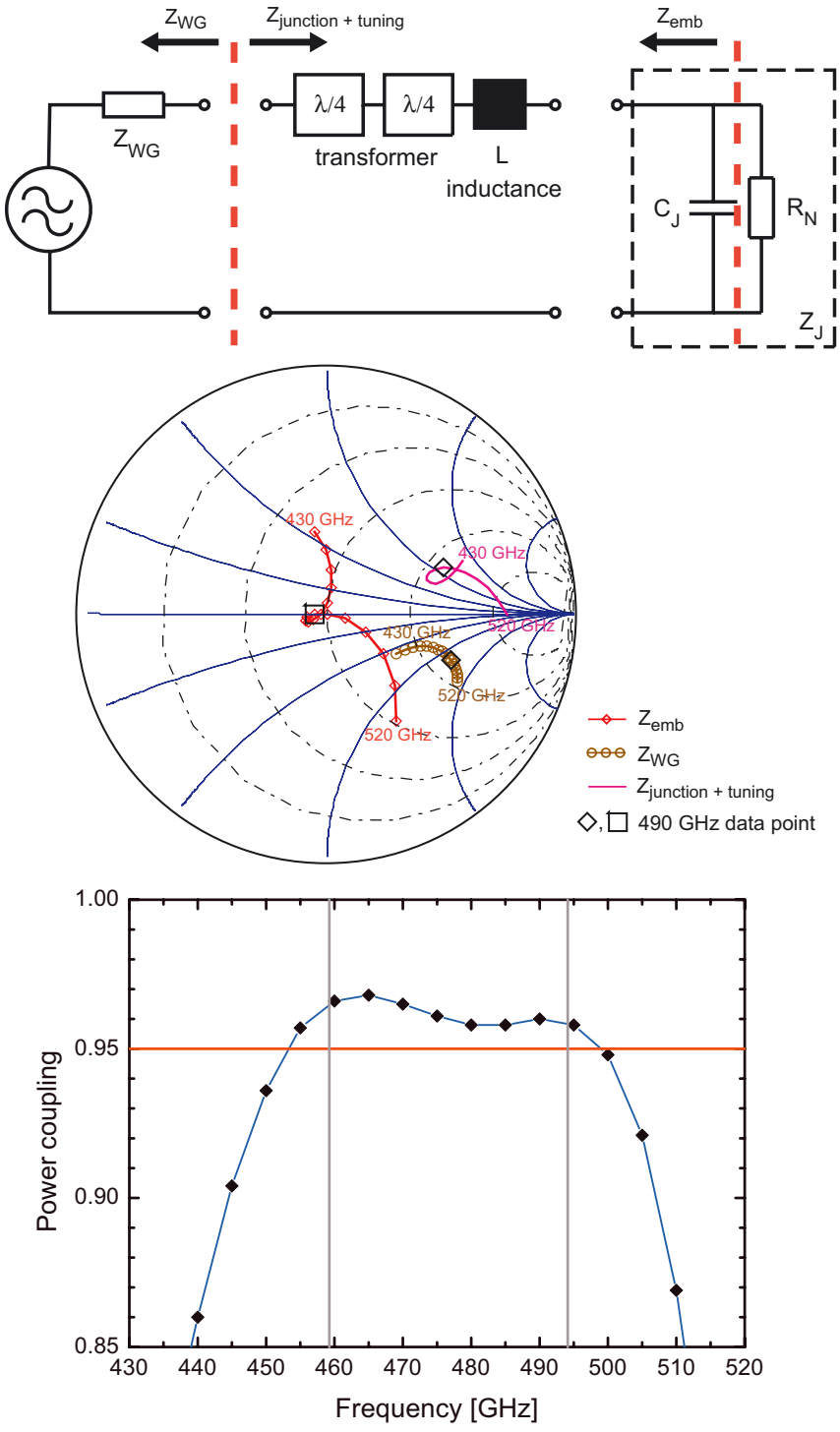


Figure 2.13: Simulated variation of the embedding Z_{emb}, the waveguide Z_{WG} and tuned junction impedance $Z_{junction+tuning}$ for a 475 GHz SMART device tuning circuit (see text), illustrated in a Smith chart (top). The Smith chart impedance scale is normalized onto the $R_N = 25\,\Omega$ of the 0.64 μm^2 junction and the data points for a frequency of 490 GHz are accentuated. The calculated power coupling curve is depicted at the bottom. The frequency positions for the important CO and C I transitions, at 461 and 492 GHz respectively, are indicated.

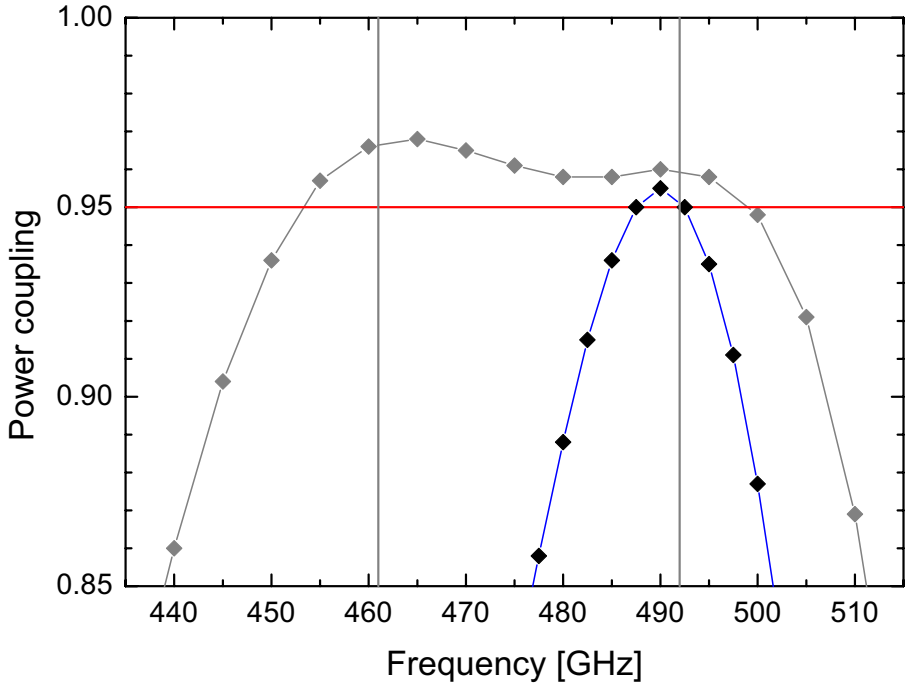


Figure 2.14: Power coupling curve of an end-loaded stub test tuning structure compared with curve from Fig. 2.13(bottom). Although both devices have 0.64 μm^2 junctions, the end-loaded stub tuning is much more narrow-band.

malism for the astrophysical relevant frequencies around 460 GHz and 490 GHz, respectively. Included are devices with detuned tuning circuits which have shifted band center positions of $\pm$20 GHz. This is a standard procedure for UV photolithographic defined tuning circuits and provides compensation options in case of an fabrication flaw.

Additionally test devices with simple end-loaded stub (els) tuning structures are incorporated into the mask design. The tuning structures consist of only one microstrip line and, in comparison to three-step transformer structures, provide a much narrower bandwidth. In Fig. 2.14 the power coupling to the junction for end-loaded stub structure `490ebl_test490_bs200_A064_sn_19` is superimposed onto the result from Fig. 2.13(bottom). The els devices are either tuned onto 450 or 490 GHz. Due to their narrow-band (resonant) behavior and simple geometry these structures are easier to interpret than more complicated tuning circuits. As demonstrated later on the Sec. 5.5.2 the tuning circuit produces resonances in the DC I-V curve of a SIS device from which the band center position can be directly calculated. In case an els device with large junction area is chosen, junction area uncertainty is minimized and real electrode properties, e g. σ_n, can be calculated and compared with initially set values.

The test devices with large junction areas serve one additional cause. In Sec. 5.2.1 the employed measurement routine for junction areas will be explained. This routine calculates the real junction area from the easy measurable normal resistance via the statistically derived critical current density. The current density calculation requires devices with unequal junction areas. The J_c obtained from the largest

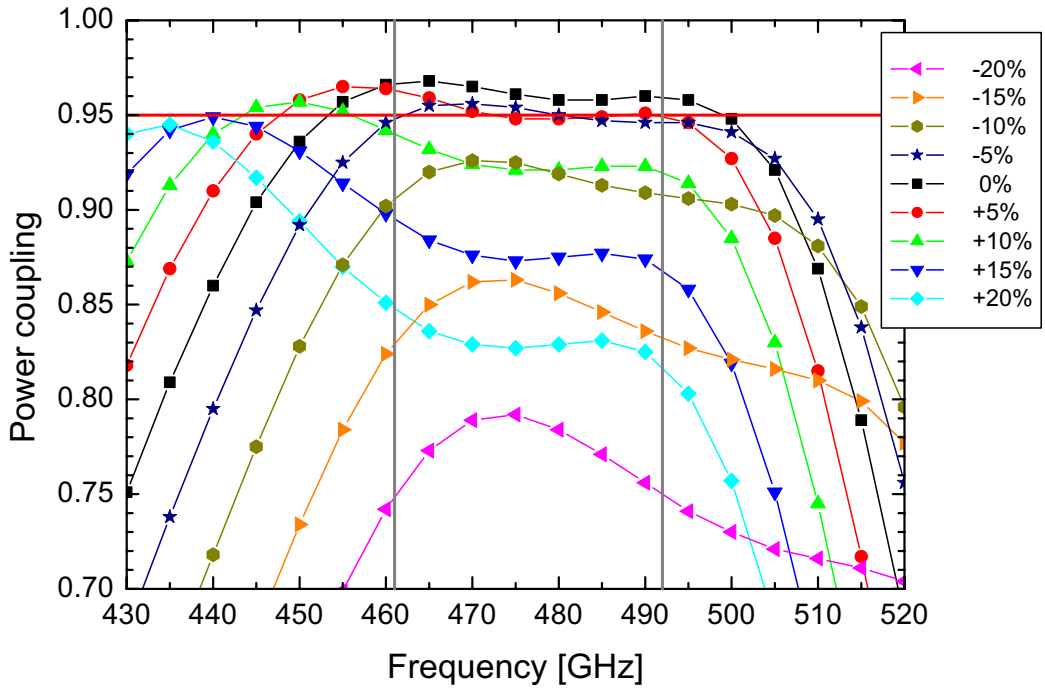


Figure 2.15: Array of power coupling curves of identical three-step transformer tuning structures as presented in Fig. 2.13(bottom) with variation of the junction area. The junction area with design value 0.64 μm^2 has been varied up to $\pm 20\%$ ($\pm 0.13\,\mu$m^2), which corresponds to a junction side-length variation of only $l_J = \pm 80$ nm.

areas have the greatest precision because the relative area reproducibility for the largest junctions is much better than for device areas below 1 μm^2.

2.3.3 Influence of fabrication tolerances on simulated RF performance

This section discusses the impact that fabrication tolerances have on mixer performance, exemplified with two different SMART devices. Emphasis is mainly put on the definition related accuracies of the junction area and the top electrode of the integrated tuning circuit, but the dependence of power coupling on variations in the tuning dielectric thickness will also be quantified. The influence of deviations from the design value will be discussed independently.

In Fig. 2.15 the influence of junction area variation on power coupling is presented for a SMART device with the identical tuning circuit as in the last section. The area is varied in 5% steps up to $\pm 20\%$ which corresponds an maximum variation of junction side-length of only ± 80 nm for the 0.64 μm^2 junction. It is visible that the junction area variation has a dramatic influence on the coupled power as well as on the position of the center frequency position. For example, an increase of area systematically shifts the center frequency of the RF band downward because the inductor microstrip line cannot completely compensate the enlarged junction

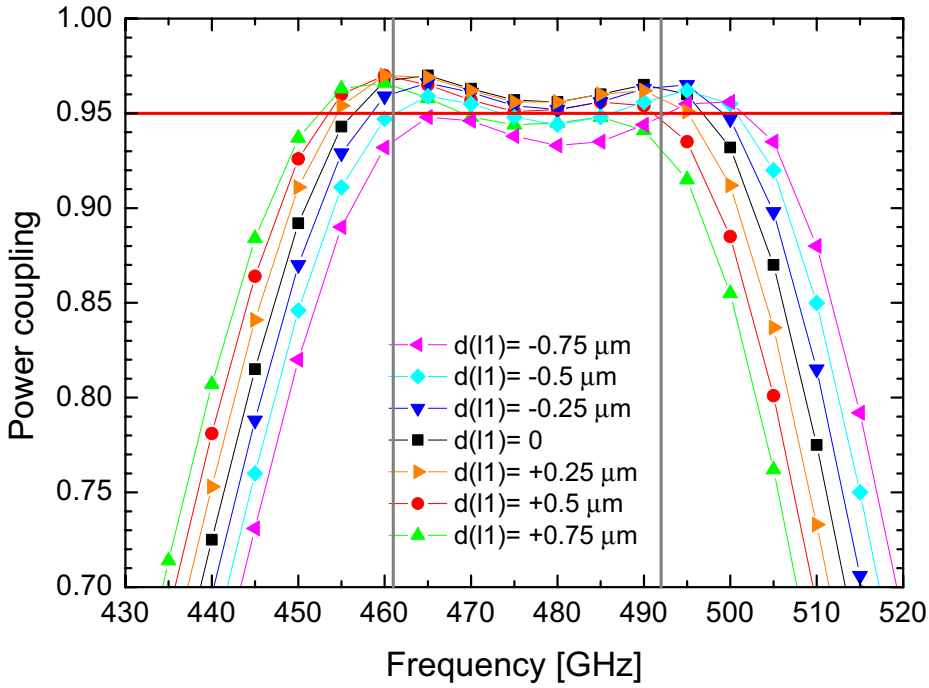


Figure 2.16: Array of power coupling curves for a different three-step transformer circuit (see text), with variation of the inductor length l_1. The length has been varied up to $\pm 0.75\,\mu$m ($\pm 8\%$) around the design value $9.5\,\mu$m.

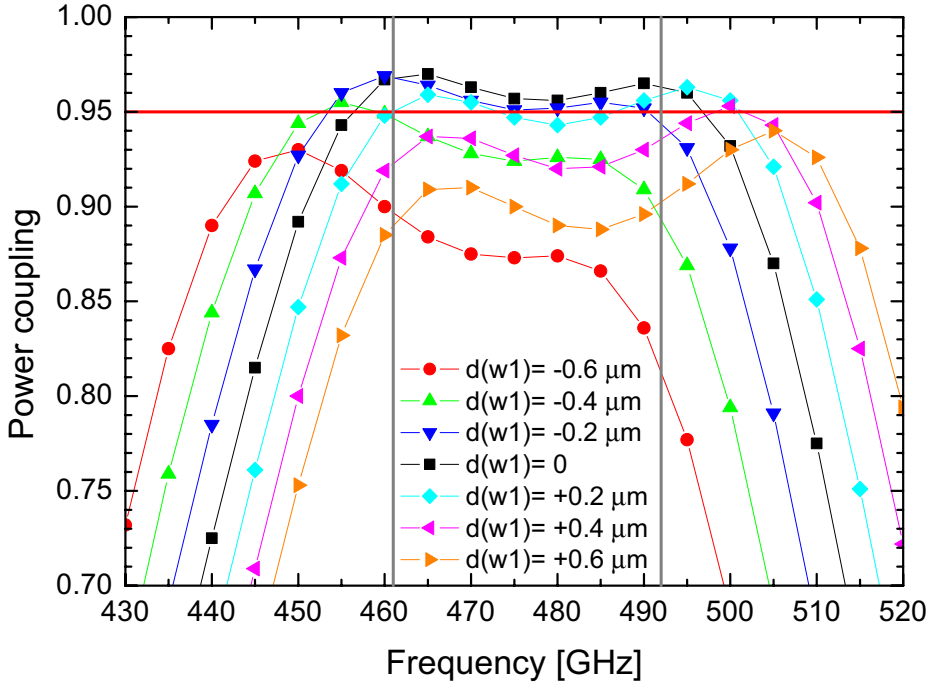


Figure 2.17: Array of power coupling curves for same three-step transformer circuit as in Fig. 2.16, now with variation of the inductor width w_1 (see text). The width has been varied up to $\pm 0.6\,\mu$m ($\pm 20\%$) around the design value $3\,\mu$m.

capacitance (Eq. 2.21). Only the $\pm 5\%$ variation just about stays above the 95% power coupling requirement for the two important frequency positions and, consequently, defines the requirement to reproducibility of the junction area definition process (of this thesis).

Fig. 2.16 and Fig. 2.17 illustrate the power coupling behavior in case of fabrication inaccuracy during definition of the top electrode of the integrated tuning circuit. Here variation of the inductor microstrip line length l_1 and width w_1 is investigated for a different type of SMART device (type `490ebl_ap_bs200_A081_sn_19` with design values $l_1 = 9.5\,\mu$m and $w_1 = 3\,\mu$m). l_1 variations reflect the overlay accuracy of the tuning circuit relative to the junction while w_1 deviations are a result of sizing errors of the lift-off features. In Fig. 2.16 the largest l_1 deviation values $\pm 0.75\,\mu$m approximately correspond to typical mask aligner alignment errors. It is obvious that this deviation yields power coupling values slightly outside of the 95 % requirement for most frequencies positions and a small shift (≈ 5 GHz) in center position.

With regard to higher frequency application, i. e. at THz frequencies, the inductor length scales $\propto$ frequency (see Eq. 2.21) and therefore up to $3\times$ better alignment will be required. Variations of w_1 on the other hand have a more prominent influence and stress the necessity for a definition process not only with a better overlay accuracy than mask aligner based photolithography can provide but, additionally, very high resolution. Accuracy of at least $0.2\,\mu$m is needed, as else noticeable performance degradation becomes visible. The largest deviation values $\pm 0.6\,\mu$m cause a 10–15 GHz shift in center frequency (larger w_1 values shift the power coupling curves to higher frequencies and vice versa) and power coupling drops well below 90% at 461 and 492 GHz. The frequency shifts are caused by the variation of the impedance Z of the inductor microstrip line (see Eq. 2.15).

With regard to the CMP fabrication process an investigation of the power coupling dependence on the tuning dielectric thickness variations is important. Dielectric thickness variations are normally not of concern for a SNEP process because the deposition process is very reproducible. With a CMP process, though, the dielectric layer undergoes a planarization and thinning process which inevitably introduces thickness variations across the wafer (Chap. 4.1.3). In Fig. 2.18 the dependence of the power coupling on tuning dielectric thickness variation is depicted. Noticeable influence can already by seen for a thickness variation $> \pm 10$ nm and thus sets stringent requirements to the CMP process. The planarization process must, firstly, be uniform yielding small thickness variations across the wafer and, secondly, needs to have a precise end-point determination so that layer removal is finished at the required layer thickness.

In summary, UV photolithography needs to be replaced by more powerful e-beam lithography for definition of the critical features junction area and tuning circuit. Already at 475 GHz a significant beneficial influence on device performance with respect to the power coupling level as well as the center frequency position is to be expected. A relative junction area reproducibility of $\Delta A_J/A_J \leq 5\%$ for a $0.64\,\mu\text{m}^2$ area and an overlay accuracy of the tuning circuit with regard to the junction position of $< 0.3\,\mu$m is required. Additionally, the CMP process should

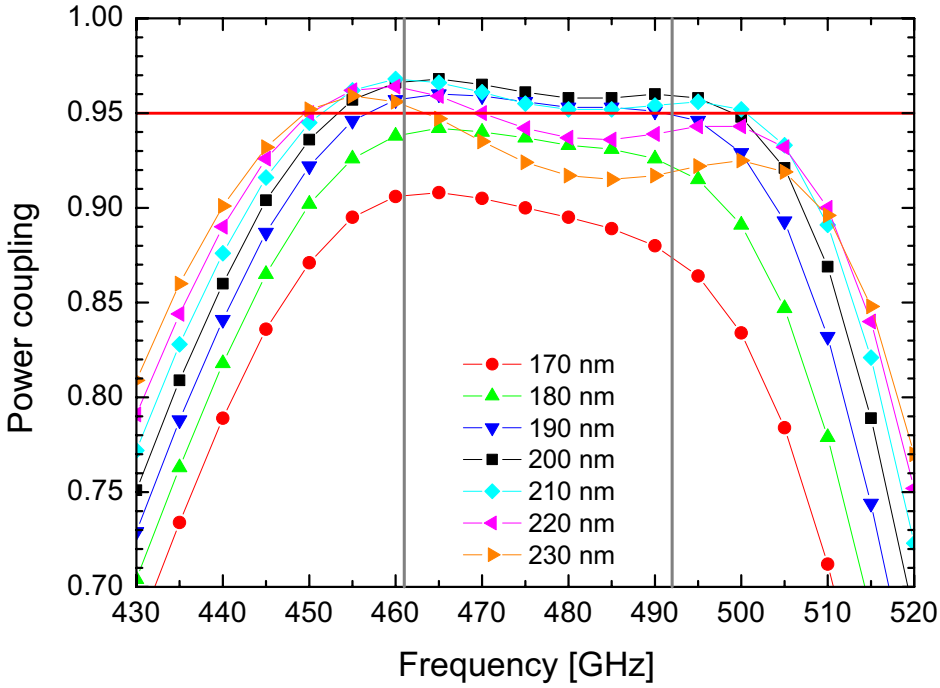


Figure 2.18: Same illustration as in Fig. 2.17 but now with variation of the tuning dielectric thickness. The dielectric thickness has been varied up to ± 30 nm ($\pm 15\%$) around the design value 200 nm.

demonstrate a global planarization uniformity better than ± 20 nm for all of the devices on a wafer.

3

Development of e-beam definition based processes

This chapter focuses on the e-beam lithography based definition processes for junction area and top electrode of the integrated tuning circuit. At first the hardware and software setup of the KOSMA e-beam system will be introduced and then is followed by description of process development work. The section on the junction area definition process additionally includes a detailed discussion of the subsequent reactive-ion etch (RIE) process which cuts out the junction from the surrounding layers. As it turns out the RIE step is the limiting factor for reproducible junction area definition.

3.1 KOSMA electron beam lithography system

The KOSMA e-beam lithography system is based on a self-modified Cambridge S240 scanning electron microscope (SEM). The system is controlled by a PC running customized AutoCAD software and was developed for fabrication of the superconducting hot-electron bolometer devices [17]. Hardware interaction is controlled through AutoCAD trace objects organized in four different layers within the AutoCAD drawing. The traces positioned in the "Litho" layer symbolize the lithography objects and the traces of the "Size" layer define the writing field position and size, and thus the writing magnification and resolution. The traces of the "Stage" layer control the x-y stage positioning (the reason for this is explained below) and scanning magnification during mark recognition. The traces of the "Marken" layer are positioned on the UV lithography / lift-off defined alignment marks and serve the registration of the e-beam objects relative to existing structures on the wafer. Typically there is one trace of each kind per SIS device.

A typical layout for junction e-beam is illustrated in Fig. 3.2 which shows the AutoCAD objects superimposed onto a part of the 490EBL mask. As the UV lithography defined objects, e.g. those defining the RF chokes, are also designed

Figure 3.1: Photograph of the KOSMA e-beam lithography system. The system is based on a Cambridge S240 SEM and uses self-developed software and hardware integration [17]. Three computers monitors from left to right visualize x-y stage control, frame grabber imagery and the AutoCAD-based lithography environment.

with AutoCAD, the e-beam objects and control elements can easily be integrated into the circuit layout.

Due to e-beam's inherent limitation of the writing field size, patterns have to by "stitched", i.e. the wafer needs to be mounted on a motorized x-y stage for translation from one writing field to the next. Standard values for the writing field size is $40 \times 40\,\mu\mathrm{m}^2$ for high-resolution lithography objects, e.g. for junction definition, and $160 \times 160\,\mu\mathrm{m}^2$ for larger scale structures such as the integrated tuning top electrode definition. This corresponds to writing magnifications of $2500\times$ yielding 10 nm pixel spacing and $625\times$ yielding 40 nm pixel spacing, respectively.

Before writing of the objects can begin, a precise calibration of the x-y stage translation through initial global mark recognition is essential. Without mark recognition the linear encoder equipped x-y stage's absolute (mechanical) precision of approximately $2\,\mu$m is not sufficient for precise stitching. On a per wafer basis it is important to determine the exact writing field size, i.e. the linear scale in both scan axis, and to compensate for measured variations with the scale calibration routine of the e-beam software prior to lithography. Additionally, the electron beam current is measured with an electrometer[1] by focusing the beam into a Faraday cup which is provided by the wafer holder. Relative beam current stability must be better than 10 %, otherwise dose variations are noticeable and therewith junction area reproducibility impaired.

[1] KEITHLEY 614. http://www.keithley.com

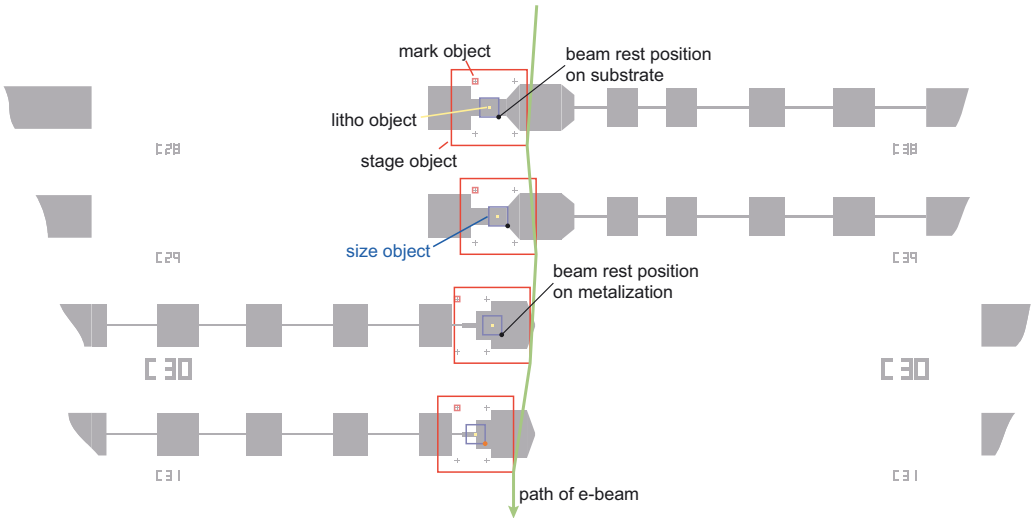


Figure 3.2: AutoCAD objects needed for hardware interaction for the e-beam lithography software, superimposed onto four devices of the 490EBL mask layout.

During lithography a final mark recognition is performed by the operator for each individual writing position, i.e. per device, in order to minimize overlay accuracy errors to better than 250 nm. For registration of an e-beam object relative to the waveguide probe an alignment mark has to be included by a preceding UV lithography step. This alignment marks typically are crosses of 10 μm long and 1 μm wide lines. During fabrication of the SIS devices these alignment marks should be included in the layer on which the junction has to be registered to, i.e. during the RF choke definition. In case an additional e-beam object is to be very precisely registered onto an existing e-beam defined object, e.g. the bolometer bridge onto the heat sinks during definition of HEB devices with required positioning accuracies of around 100 nm, the first lithography step should provide additional alignment marks in the vicinity of the second writing position. With this registration accuracy is further improved because residual scaling errors are minimized.

3.2 Definition of junction area

3.2.1 Options for e-beam definition

Eligible junction definition schemes must solve two essential problems. First, is the ability of patterning, i. e. through lithography and reactive-ion etch processes, the niobium top layer on a very fine scale in order to yield the counter electrode of the junction.[2] Second, it is necessary that the junction insulation process, i. e. the dielectric deposition, results in a reasonably planarized surface without the need of opening small vias through the dielectric which have to be precisely aligned onto the counter electrode [4].

[2]That is for a standard niobium device which only requires a single RIE step through the top niobium layer.

Figure 3.3: Initial e-beam definition and reactive-ion etch test with negative image ma-N2405 resist for real device features with junction areas depicted (light-microscopic image at 1000× magnification).

Dependent on the targeted junction area the fabrication process has to deliver reproducibly (see Chap. 2.3), several competing processing schemes are possible:

For junction areas in the $1.0\,\mu\mathrm{m}^2$ to $0.8\,\mu\mathrm{m}^2$ range, definition through a self-aligned niobium etch-back process (SNEP, [24]) can be performed through e-beam writing of a negative tone resist via a mix & match process, e.g. described in [55], leaving behind the e-beam exposed resist regions after development.

SNEP is the well established scheme for UV lithography-based junction definition. Its big advantage is that the utilized (photo-)resist serves dual purpose, hence reducing to number of fabrication steps: The structured resist serves, firstly, as an etch mask for the junction during reactive-ion etching (RIE) of the trilayer and, secondly, as an lift-off mask for subsequent insulation of the junction electrode (see Fig. 1.7). Critical for successful lift-off is the thickness of the deposited dielectric material (SiO or SiO_2) in comparison to the thickness of the resist used. In order to achieve a clean lift-off of the combined resist and SiO_x cap on top of the junction, processing experience demands a initial resist thickness of about $0.8\,\mu$m or more, when typical dielectric layer thicknesses in the 200 nm range are required. One must also bear in mind that, dependent on the plasma conditions and the resist used, RIE can noticeably reduce the thickness of the resist and thus further impair dielectric lift-off.

Altogether this limits the achievable resolution of e-beam and therefore reproducible minimal junction area to about $0.8\,\mu\mathrm{m}^2$, when a resist such as ma-N2405 is used for with SNEP [67].[3] This coincides with initial ma-N2405 resist e-beam

[3] MICRO RESIST TECHNOLOGY GMBH, supplier of ma-N2400 series negative e-beam resists:

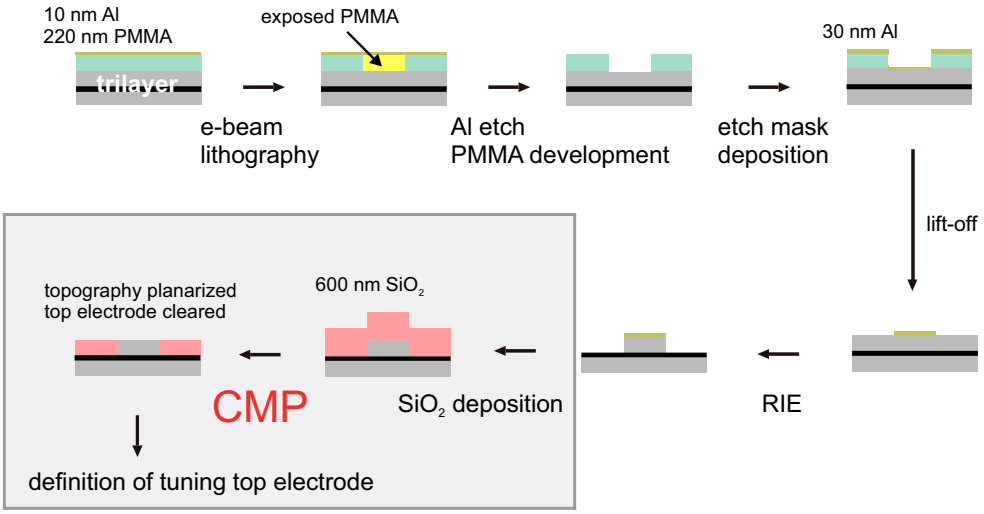


Figure 3.4: Process sequence required for e-beam based junction definition. Subsequent CMP related processing is given additionally in order to yield a complete picture.

definition and reactive-ion etch tests carried out during this thesis (Fig. 3.3), but as this resolution isn't high enough for given design goals (e.g. for HIFI Band 2 devices and beyond), this concept has not been pursued to yield functioning SIS devices.

Junction areas below $0.8\,\mu\mathrm{m}^2$ cannot be reproducibly fabricated through a simple one-step SNEP and require more elaborate fabrication schemes. The resist of choice for high resolution lithography typically is a thin ($\leq 200\,\mathrm{nm}$), positive tone PMMA[4] layer. These properties implicate that the junction area written by the lithographic process is defined as a hole in the PMMA layer and thus makes additional processing steps to transfer the defined pattern to the actual RIE etch mask necessary.

As motivated in Sec. 1.4.1 it was decided to develop an e-beam / CMP fabrication scheme which relies on a chemical mechanical polishing process step for planarization of the junction insulation / tuning dielectric. Fig. 3.4 gives an overview of the process steps related to junction definition including CMP. In the following the junction definition processes, i. e. e-beam definition and the reactive-ion etching, will be discussed. Detailed processing recipes are given in App. A.

3.2.2 PMMA processing

PMMA-based resists are the standard for high-resolution e-beam lithography and have been in use at KOSMA for (diffusion-cooled) superconducting HEB fabrication prior to here presented process development [17, 71, 72]. Consequently,

http://www.microresist.de

[4] Polymethylmethacrylate

resist	AR-P669.04 (PMMA, 600k, 4%)
thickness	220 nm (4000 rpm, bake 120°C, 3 min)
charge dissipation layer	DC-sputtered aluminum, 10 nm
exposure parameters	150-250 µC/cm^2 (dose dependent on junction size and circuit layout), beam 14.0±0.2 pA @ 20 kV
Al layer removal	buffered phosphoric acid etch (2 min, 1:3)
development	AR 600-56 (4 min), stopper AR 600-60 (0.5 min)

Table 3.1: Summary of important e-beam parameters for definition of the junction area (the specified AR chemicals are from ALLRESIST).

essential PMMA processing parameters could be adopted for the SIS process development.

For junction area definition a simple process with a single-layer PMMA[5] of 220 nm thickness with similar parameters to HEB definition is used (see Tab. 3.1). This yields high enough resolution and acceptable processing temperatures when compared to P(MMA-MMA) bilayer resist definition as the PMMA bake-out can be kept to a rather low temperature of 120 °C for 3 min on a hot plate. Higher temperatures would compromise the tunnel barrier layers already deposited on the wafer as they would lower the R_N product the junctions.[6]

Prior to this bake-out the thickness variation in the spun-on PMMA layer resulting from substrate bowing which, in turn, is induced by the vacuum chuck mounting of the spinner is improved by letting the layer re-flow for 1 min without applied vacuum (substrate bowing results from using the thin—and therefore flexible—quartz substrates on which the waveguide devices are fabricated on and, e. g., is not a problem with more rigid silicon wafers). For the same reason the PMMA bake-out on the hot plate is performed without any vacuum applied.

3.2.3 E-beam exposure of PMMA

The optimum e-beam dose for PMMA with given processing conditions (Tab. 3.1) is a function of area size, the number of junction areas to be defined per device and the surrounding metalization pattern underneath. Due to two effects—they will be discussed in the following—reproducible junction definition requires a fixed set of empirically evaluated exposure parameters for each new mask layout in which

[5] AR-P669.04, 600k, 4 %. ALLRESIST GMBH. http://www.allresist.de

[6] Annealing at temperatures < 150 °C is an option in case a trade-off between lowered R_N product for improved DC I-V characteristic subgap leakage current is desired.

junction area and number as well as device geometry are set into relation to each other.

Reproducibility of e-beam lithography is affected by the proximity effect, which is caused by electrons backscattered from the metalization and substrate, and charging of the resist through the incident electrons, which deflects the electron beam. Backscattering results in an several micrometer diameter large halo around the e-beam focus spot where the PMMA receives additional dose. As the employed e-beam lithography software lacks correction routines, the exposure dose is made junction area dependent for compensation. The received dose is progressively increased for smaller junction areas from 200 μC/cm^2 for areas around 1.0 μm^2 to 260 μC/cm^2 for areas at 0.5 μm^2 (with an acceleration voltage of 20 kV). Later is the smallest area size which can be defined adequately reproducible according to the requirements given in Sec. 2.3.3 for current state of process development (see Sec. 5.2.2). Additionally, two-junctions devices obey an empirically established, different area to dose relationship as lithography at the first junction position already contributes some additional dose to the PMMA at the second junction position. It is found that the junction area at the second writing position must receive 15 % less dose for the LERMA two-junction devices (15.5 μm distance).

The metalization pattern of the waveguide feed contributes to area size fluctuations if not compensated for as it influences the charging effects. Besides small scale charging at the writing position, the significant influence stems from the beam rest position in relation to underlying metalization layers (the lithography software keeps the beam at position corresponding to the lower right corner of the size field as no hardware beam blanking is currently used during lithography, see Fig.3.2). In case this rest position coincides with the waveguide feed metalization onto which the junction area is defined, the deposited charge is more efficiently dissipated away from the writing position, thus resulting to less detrimental charge build-up and a lower optimal dose value needed.[7]

In order to reduce the influence of charging effects during writing and to increase imaging contrast during mark recognition a conductive, 10 nm thin aluminum resist discharge layer is sputter-deposited onto the PMMA layer prior to lithography. The wafer clamping onto the SEM sample stage then provides a grounding connection. The effect of the aluminum layer on the dose to junction area relation must, again, be empirically deduced (it lowers the optimal dose). The Al is removed prior to development of the PMMA with a buffered etch solution containing phosphoric acid (App. A.2).

3.2.4 Etch mask

PMMA is a positive tone resist, i.e. the exposed and developed junction area pattern is defined as a hole in the PMMA layer, and therefore a pattern transfer is

[7] The combination of the insulating nature of the PMMA resist layer as well as the the fused quartz substrate intensifies the charging effects.

necessary prior to RIE. This is achieved through deposition and subsequent lift-off of an etch mask.

Throughout the e-beam process development three different etch mask materials have been evaluated. At first dielectric material etch masks were evaluated, following the PARTS / e-beam process scheme from on which the here presented process development is based on. Initially, SiO was considered to be a good choice as the collimated SiO vapor emanating from the evaporation source (a baffled box) seemed advantageous for lift-off of the sub-micron area structures. Evaluated SiO thicknesses up to the lift-off predetermined maximum possible thickness of 100 nm, though, showed that SiO is not sufficiently resistant enough even for single-layer niobium etching (see below Sec. 3.2.5).

E-beam evaporated SiO_2, in contrary, has successfully been implemented into the junction fabrication for the single-layer niobium etch process. With etch mask thickness greater than 70 nm SIS devices with good junction area reproducibilities down to 0.64 μm^2 were fabricated (for results see Sec. 5.2.2).

However, fabrication of the embedded trilayer type Herschel Band 2 devices requires a more robust metal etch mask due to the more energetic trilayer etch process. Here a three-step RIE process is required to completely etch through the junction trilayer. For this 50 nm aluminum is sputter-deposited and is supplemented by 20 nm gold on top as a protection against the alkaline photoresist developer used during subsequent definition of the "RIE windows" explained above.

Because the lift-off properties of this etch mask are better than those of SiO_2, the Al/Au etch mask presently is also preferred for junction RIE of the single-layer niobium RIE devices, i.e. for the 490EBL devices. 20 nm Al is sufficient for this etch process. Although it has been discussed that an erodible i.e. "soft" etch mask material promotes anisotropic etch behavior [4], this cannot be confirmed on the basis of here evaluated RIE recipes. Additionally, the aluminum layer is a useful visual indicator for endpoint detection of the polishing process during CMP as it is visibly removed by the alkaline polishing fluid.

3.2.5 Reactive-ion etching (RIE) of junction areas

The junction RIE process has not been part of the development efforts of this thesis, but as it turns out that it is the crucial component for successful submicron junction device fabrication and has continuously evolved, RIE shall be discussed more thoroughly in the following.

Anisotropic RIE

The most important requirement to the reactive-ion junction etch process is to realize an as accurately as possible anisotropic etch and thus enabling an one-to-one transfer of the etch mask dimensions into the layer(s) beneath. As fluorine radical-based plasma chemistry is utilized for removal of the niobium layers, isotropic

etch behavior is the inevitable consequence. Several options are commonly, i.e. simultaneously pursued in order to reduce under-etch and hence increase junction area reproducibility to an acceptable level.

First, is to use an as low as possible process pressure. In a simplified view this increases the self-bias potential of the wafer / RF cathode and therefore boosts the kinetic energy and therewith perpendicular momentum of the incoming fluorine radicals and ions as well as decreases the number of collisions of these particles among each other. Both effects reduce the lateral movement of the incoming particles and promote anisotropic etching. With a conventional parallel-plate type reactive-ion etcher, e.g. like the one used for this work, the lower limit of process pressure is mainly defined by the region of stable plasma burning, feasible flow rates in relation to pumping capacity and tolerable RF power. This most commonly leads to a low-pressure limit of a few Pa. The standard pressures employed during this work are either 1 or 4 Pa for niobium etch and 1 Pa for the argon sputter-etch steps of the Al-Al_2O_3 barrier layers during RF choke definition (Sec. 5.1).

Second, is to add an additional gas component to the etch recipe to generate a side wall passivation either through polymer deposition or oxidation of the etched layers. Dependent on the material to be etched this either is a fluorine containing, polymer precursor molecule, e.g. CCl_2F_2 or CHF_3, or O_2 for oxidation process. Due to the ion bombardment of the etching species the deposited material is removed on the areas perpendicular to the incident particles, thus confining the passivation layers to the non-affected side walls. Either a side-by-side process with simultaneous side wall passivation through deposition of polymers or oxidation or a sequential process with alternating etch and deposition steps can be used.

Third, is to cryogenically cool the substrate during etching. This reduces the lateral movement of the particles scattered from the wafer surface and inhibits lateral particle movement and therewith promotes anisotropic etch behavior.

Evolution of RIE recipe at KOSMA

A fluorine chemistry-based recipe with plain NF_3 already has been used for several years for single-layer niobium junction etch during the older SNEP-based processes with junction areas in the 1–2 micron range. This recipe has been utilized for the first few e-beam / CMP wafer for simplification reasons. An enhanced etch recipe, a gas mixture additionally containing polymer-generating CCl_2F_2 for side wall passivation, has likewise been developed for the fabrication of embedded trilayer devices with normal conducting aluminum tuning circuits [49, 26]. Herewith thermal decoupling from the RF cathode is necessary which is provided by a PTFE (polytetrafluoroethylene) disk. This recipe has been adopted without modification for processing of all subsequent e-beam / CMP wafer up to the 490EBL series and leads to the results presented in Sec. 5.2.2.[8] Although the

[8] Only the etch time is adjusted to the differing niobium layer thickness (which is thicker for CMP devices than for SNEP, see Sec. 5.4.2).

recipe's anisotropy is larger than with the plain NF_3 etch (which, in fact, can be considered purely isotropic) there still is room for improvement. Additionally, CCl_2F_2 is considered harmful to the ozone layer due to its chlorine content and therefore cannot be not readily obtained any more.

For this reason, starting with 490EBL processing, a newly developed recipe based on a SF_6 and CHF_3 mixture and lowering the processing pressure from 4 Pa to 1 Pa—the minimal pressure achievable with stable plasma burning for the barrel-type RIE employed—is being evaluated. Preliminary results indicate that this recipe satisfies the requirements for an anisotropic etch recipe for submicron junction area definition even better and, when used in conjunction with the planned introduction of an ICP (inductively-coupled plasma) reactive-ion etcher, has the potential to enable reproducible junction definition below $0.5\,\mu m^2$ in the future (see Sec. 6.1.2).

RIE sequence

RIE is performed in a custom-made parallel-plate reactor. The etcher is load-locked, it features a liquid-cooled RF cathode and can accommodate substrates up to 3 inches in diameter. The process pressure controlled by a downstream butterfly valve with automated closed-loop down to 1 Pa and the etcher has 4 flow-controlled gas lines for SF_6 or optionally NF_3, CHF_3, Ar and O_2.

Before the junction top electrode is cut out from the niobium top layer or the whole junction layer stack cut (RF choke or embedded trilayer junction etch) through RIE, two complementing etch masks need to be defined: In addition to the junction area definition a rectangular, secondary photoresist window, being a boundary to the tuning dielectric, is defined on each device through photolithography (e. g. see Fig. 5.10). This keeps the total etched area small as compared to the whole wafer area, and should increase the radial etching uniformity, because otherwise macro and micro loading (depletion) effects of the reactive-ion species might occur. Conventional UV junction lithography doesn't require this additional photolithographic step, as the etch window is herewith defined simultaneously with the junction etch mask.[9]

After preconditioning of the RIE chamber, the wafer is placed onto a hot plate prior to loading into the etcher in order to hard bake the secondary photoresist etch mask of the tuning dielectric windows and to remove moisture from the wafer surface. The etch process itself is either manually timed in case a simple one-step niobium etch is performed, e.g. the 490EBL process, or automated through a PC during the argon sputter-etch sequences for RF choke definition definition.

Two methods are used for endpoint determination of the etch process. First is a direct, quantitative reflection measurement of the metal surfaces which only can be performed ex-situ under a microscope and, second, a qualitative, visual inspection

[9] Historically, this also eliminated area-sensitive adhesion problems of the deposited SiO tuning dielectric. In a SNEP scheme the RIE photoresist window defines the lift-off area of the deposited dielectric and thus minimizes area induced stress.

of the wafer surface's reflectivity through a porthole in the process chamber during etching. For a simple niobium etch process latter method seems sufficiently precise for micron area junction definition. The increase in reflectivity is easily observed and etching typically is terminated 30 sec. after brightening of the large monitor fields positioned at the edge and the center (center field first introduced with the 490EBL mask, see Fig. 5.9 for illustration) of the circuit layout in order to ensure complete removal of the niobium. In doing so it must be considered that a all evaluated RIE recipes exhibit a faster etch rate at the wafer's edge.

First method is used before and after the etch process in order to verify the complete removal of etched layer through comparison of the measured reflectivity difference with pre-determined values. The reflection measurement is carried out by means of a microscope equipped with a PC-controlled CCD camera system. For this images from several positions on the wafer are taken and the integrated 12 bit gray value intensity levels of typically 20x20 μm^2-sized fields measured within the Optimas image analysis software[10]. The measurement positions are located in the same monitor fields as above.

During transition from the niobium layer onto the Al-Al_2O_3 barrier layer whilst simple niobium etch reflectivity typically increases by $\approx 12\,\%$ and can be therefore easily measured.

[10] OPTIMAS CORPORATION. http://www.optimas.com

3.3 Definition of top electrode of tuning circuit

In principal, two fabrication schemes are possible for e-beam definition of the top electrode of the tuning circuit. First is a RIE based process which uses an etch mask—in the simplest case a negative tone resist—and RIE to define the top electrode features from a metalization blanket layer. Second is a lift-off based process which uses positive tone resist for definition of the tuning circuit features and then deposition and lift-off of the metalization layer. Latter process has been used at KOSMA in conjunction with UV photolithography.

Because the KOSMA e-beam lithography system is based on a commercial SEM and requires a time consuming stitching procedure with manual mark recognition for each individual device, it was mandatory to reduce writing time for the much larger top electrode features. Thus an e-beam resist with much higher sensitivity, i. e. $10\times$ that of PMMA, was to be selected for process development. In order to profit from existing processing experience the lift-off scheme was preferred and, consequently, a positive tone resist used.[11]

Due to the writing time limitation one important change to photomask design is made necessary. As only the top electrode features themselves are defined, the waveguide feed / RF choke definition must fabricate both metalization sides which is, e. g., different from the 490EBL process introduced in Sec. 5.1 and illustrated in Fig. 3.2. The e-beam / lift-off process then defines the metalization on top of the existing structures with an additional contact area on the second waveguide feed. During e-beam lithography of the top electrode the same alignment mark should be scanned as previously used for junction area e-beam definition. The device layout must consider this and minimize the distance between the alignment mark and writing position, while taking the writing field sizes of the lithography system into account (see Sec. 5.3.1).

3.3.1 AZ5206 photoresist processing

The UV photoresist AZ5206, equivalent to diluted AZ5214[12], is also capable of e-beam definition and perfectly suits these requirements. It provides roughly 15 times greater sensitivity than PMMA (specifications are $6\,\mu\mathrm{C/cm^2}$ at 20 kV) and adequate resolution < 250 nm when spun-on with 580 nm thickness. Initial fabrication results demonstrate that, unlike UV photolithography, the e-beam exposure yields significantly undercut resist profiles, presumably caused by backscattering of electrons. In contrast to UV photolithography, which requires resist layers of more than one micron thickness, the here chosen AZ5206 processing conditions lead to sufficiently thick resist layers for a clean lift-off of the typically 380 nm thick top electrode metalization layer.

[11] Of the available e-beam resists no adequately sensitive negative tone resist with sufficient resolution ≤ 250 nm was found anyhow.

[12] AZ Electronic Materials, Clariant. http://www.azresist.com

resist	AZ5206
thickness	580 nm (4000 rpm, bake 90°C, 1.5 min)
charge dissipation layer	thermally evaporated Cu, 10 nm
exposure parameters	6.0-7.0 µC/cm^2 (dose dependent on line width), beam 14.0±0.2 pA @ 20 kV
Cu layer removal	diluted and filtered Fe(III)Cl_3 solution (15 sec., 10 drops on 40 ml H_2O)
development	AZ400 K (75 sec., 1:3)

Table 3.2: Summary of important e-beam parameters for definition of the integrated tuning circuit top electrode features (the specified AZ chemicals are from CLARIANT).

E-beam exposure modifies a Novolak resin such as AZ5206 in a different manner than UV radiation due to the higher activation energies involved. For this reason a "strong" developer, e. g. AZ 400K (diluted 1:3 with H_2O), is required to solubilize the e-beam exposed regions. Tab. 3.2 sums up the most important processing parameters used for top electrode definition. Just as with PMMA the resist bake is performed without vacuum applied in order to avoid the problems associated with substrate flexing (see Sec. 3.2.2).

3.3.2 E-beam exposure of AZ5206

A thin metalization layer is deposited onto the resist layer prior to e-beam exposure in order to reduce charging effects. In particular, image contrast during mark recognition improves drastically when the $3\times$ thicker AZ5206 layers are used. Different from PMMA processing a thermally evaporated, 10 nm thick Cu layer is used. The UV sensitivity of AZ5206 prohibits the use of a higher-energetic sputter-deposition process which creates a sufficient amount of UV photons to pre-expose the resist.

In a manner equivalent to e-beam junction area definition the feature dose values are made dependent on the widths of the microstrip lines to be defined for simple proximity effect compensation. Lines $\leq 2\,\mu$m are given 10% more dose than wider features (see Tab. 3.2). The Cu layer is removed prior to development with a very diluted Fe(III)Cl_3 solution, see recipe in App. A.2 for exact description of the process conditions.

4

Development of chemical mechanical planarization process

Generally speaking, chemical mechanical polishing (CMP) can either be understood as enhanced chemical etching or enhanced mechanical grinding. With its principle being used in glass polishing for centuries and wafer fine polishing in the semiconductor industry for several decades, CMP was introduced by IBM as a process for planarization of multi-layer structures in semiconductor manufacturing in the mid 1980's [54]. As the name indicates, its action relies on two components: First, is the mechanical, grinding interaction provided by the relative motion between polishing pad and object surface (i. e. the wafer) as well as the abrasives (e. g. silica) in the slurry, i. e. the polishing fluid. Second, is the chemical, etching component resulting from the slurries ionic character. During the polishing process the wafer is held by a rotating carrier, i. e. the polishing head, and is pressed face down onto the likewise rotating polishing pad (Fig. 4.1).[1]

Planarization of the interlayer dielectric (ILD) and metalization layers is of major concern to the industry, as topography build-up during fabrication generates step coverage problems with increasing numbers of circuit levels (Fig. 4.2). These can produce short circuits between the wiring layers or create film discontinuities. Additionally, topography is not tolerable for achieving the CD (critical dimension) requirement of current circuit design with high-resolution DUV lithography tools.[2] Remarkably, CMP can achieve small and large scale planarization, i. e. reduction of surface topography on a nm and cm scale respectively, when used with specially adapted polishing parameters. Therefore the introduction of CMP had great impact on modern semiconductor fabrication as it paved the way to

[1] This holds true for rotary type pad motion used with the polishing / lapping machines employed during CMP development at KOSMA and which is primarily used in the semiconductor industry. In addition to this traditional approach, linear belt and orbital pad motion polishers are becoming popular.

[2] The resolution increase of modern stepper or scanner tools is, on the one hand, a result of lowering the wavelength used in the monochromatic light sources, e.g. currently at 193 nm, and, on the other hand, only achievable through minimizing the optics NA (numerical aperture). These optics have the disadvantage of very shallow depth of focus thus necessitating planarized surfaces.

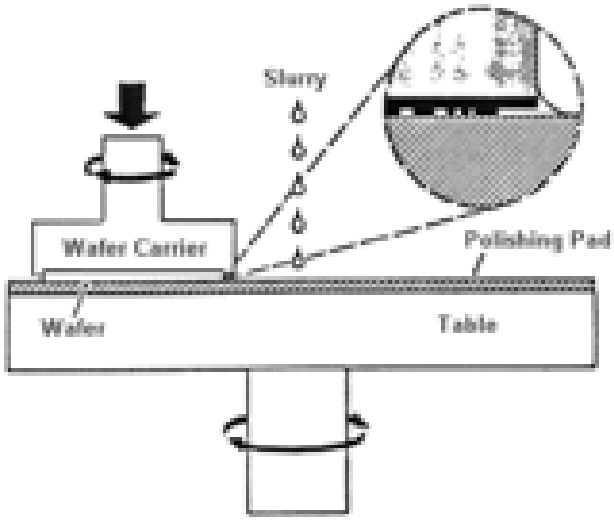


Figure 4.1: Schematic side-view of a CMP setup.

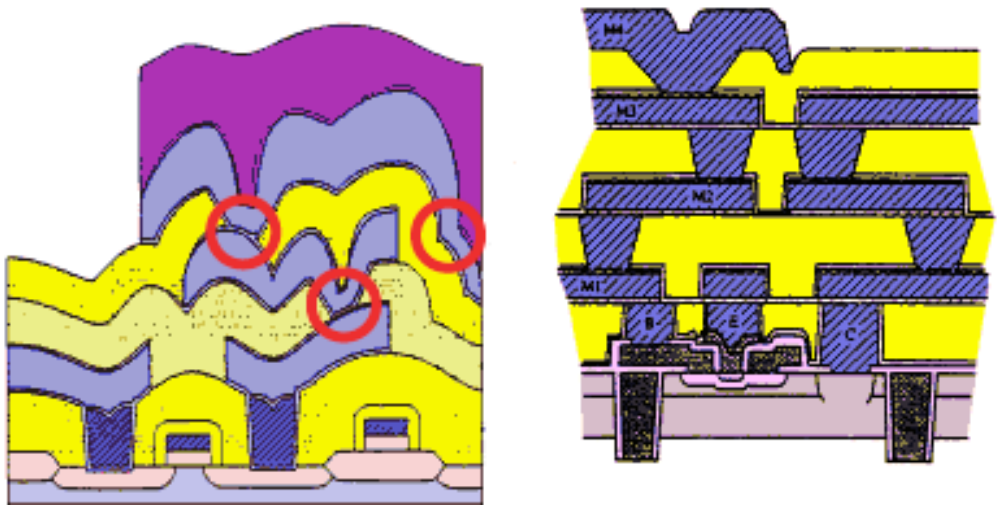


Figure 4.2: Schematic cross-sections of multilevel *semiconductor* circuits. Left illustration depicts detrimental topography build-up for a fabrication without CMP. Possible circuit failure points are indicated. Right illustration depicts the result of introducing CMP steps (dark and light colored areas are metalization and dielectric layers, respectively).

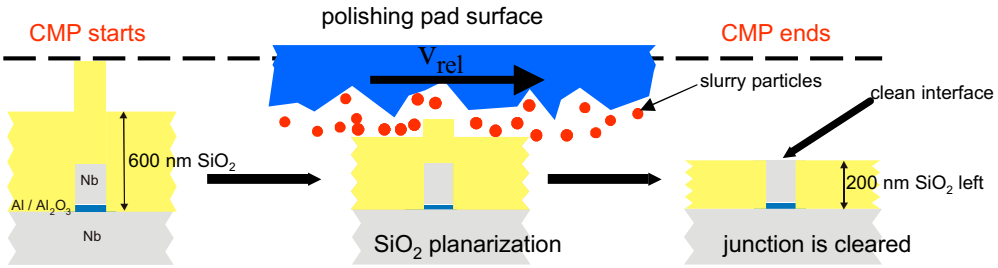


Figure 4.3: Planarization of the tuning dielectric during CMP (schematic cross-section through the tuning circuit dielectric / junction insulation area of a Nb-Al/Al_2O_3-Nb SIS device and the contact area of the polishing pad, illustration is not to scale)

modern ULSI[3] circuits [54]. CMP to date still proves to be the best method for planarization. For a comprehensive introduction to the CMP process Ref. [70] is recommended.

Benefiting from its CMP know-how IBM subsequently developed the PARTS (planarized all-refractory technology for low T_c superconductivity) process for integrated Josephson circuits which aimed at mass production of (fast) superconducting circuits (these development efforts have been terminated since then due to the lack of commercial demand) [44]. The PARTS process uses CMP for planarization of dielectric layers, i. e. the junction insulation, and combines it with the Nb-Al/Al_2O_3-Nb trilayer technology developed earlier [24, 34].

In the following a short introduction to important variables of the planarization process will be given. The efforts for development of the CMP process for planarization of the tuning circuit dielectric and its integration into junction fabrication will then be summarized and finalized with a description of the current CMP setup being used at the KOSMA micro fabrication lab. The established procedures and some representative data on how CMP reduces device topography of real devices are presented at the end of this chapter.

4.1 Planarization of tuning circuit dielectric

The PARTS scheme enables e-beam definition of junction areas and has the capability of outperforming competing SNEP-based schemes for deep submicron areas and therefore was chosen as basis for an enhanced SIS device fabrication process at KOSMA (see discussion in Sec. 1.4.1).

Applied to SIS device fabrication the dielectric blanket layer is planarized and its thickness reduced through CMP until the desired value in the tuning circuit region on top of the waveguide feed of all devices is reached (Fig. 4.3). Device fabrication at KOSMA uses RF sputtered SiO_2 as dielectric material.

[3] Ultra Large Scale Integration

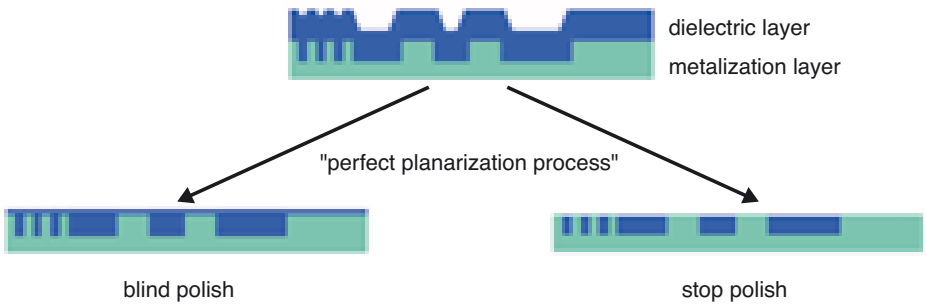


Figure 4.4: Principle classification schemes for an ideal CMP process (schematic cross-section through wafer surface). The stop polish scheme is employed at KOSMA. Circuit sketches adapted from [77].

The CMP process can be performed either following a "stop polish" scheme where the planarization process is terminated on an underlaying layer or as a "blind polish" scheme with termination within the dielectric layer (Fig. 4.4). Later process variant requires an additional final SiO_2 RIE etch-back step to remove the remaining dielectric layer after planarization is achieved in order to enable contacting to the junction. Due to this additional processing step, the blind polish variant was not investigated during this PhD thesis.[4]

Due to device structure the utilization of a "stop polish" scheme implicates that the layer thickness of the top Nb layer of the trilayer stack (or the whole trilayer thickness in case of embedded trilayer devices) must match—i. e. be at least as thick—the required tuning dielectric thickness during definition of the RF choke / waveguide feed metalization. Otherwise the junction top electrode surface cannot be cleared from the dielectric layer through the CMP process (Fig. 4.3). Timely termination is critical and necessitates precise control of the material removal rate (MRR) during the planarization and subsequent layer thinning steps. Optical and / or mechanical metrology methods (e. g. by ellipsometer or color chart and profilometer, respectively) can be applied ex-situ at various stages in order to precisely monitor progression of the CMP process, in case the MRR is not stable enough for one-step polishing as with the KOSMA process.

The planarization feature size dependency of CMP requires some circuit layout modifications in order to make the devices CMP compatible which will be discussed later on (Sec. 5.4.2).

[4] It can be speculated that this method might not be able to deliver the same junction insulation performance as the stop polish approach because the RIE process does not exhibit the material removal and re-deposition characteristics of CMP.

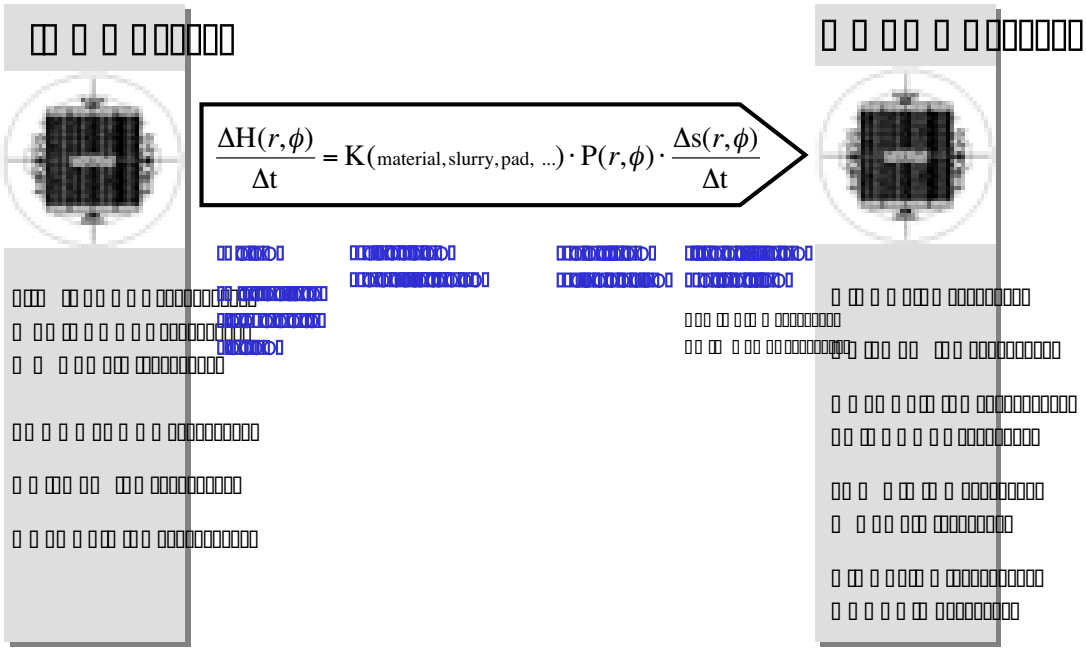


Figure 4.5: Important input and output variables to the CMP process. The Preston equation gives a simple model for the material removal rate dependency on linear pad velocity, relative to a point (r, Φ) on the wafer surface, and applied back pressure.

4.1.1 Preston polishing model

CMP of SiO_2 requires a alkaline, typically NH_4OH or KOH buffered (pH > 10), polishing fluid (slurry) in order chemically soften the dielectric surface through hydration of the Si-O bonds. The mechanical interaction is provided by abrasives in the slurry (typically silica particles with diameters around 100 nm) and the polishing pad. The relative motion of the wafer surface and the applied pressure are the main process parameters for material removal. Although the mechanical and chemical interactions at the wafer and polishing pad surface involve complex hydrodynamics, the material removal rate (MRR) of the polishing process can be adequately described by the simple Preston equation (1927) [56]:

$$MRR \propto P(r,\Phi) \cdot v(r,\Phi) \tag{4.1}$$

P is the applied (back-)pressure which results from the applied down-force on the polishing head and v is the linear pad velocity relative to a point (r, Φ) on the wafer surface (see Fig. 4.5).

At a closer look it is found that the Preston coefficient K given in Fig. 4.5 sums up the material and chemical parameters of the wafer surface, slurry and pad, and actually is a (weak) function of the down force. Nevertheless, current refined models still use the original Preston equation as a starting point [63, 64, 9].

The underlying mechanism of the planarization process is illustrated in Fig. 4.6. First of all a protruding feature on the wafer surface will deform the compress-

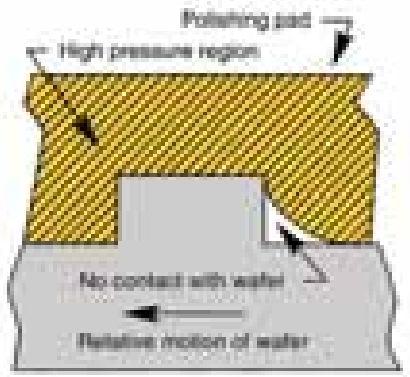


Figure 4.6: Surface feature induced polishing pad deformation (schematic illustration). The high pressure region in front of the feature's leading edge is responsible for the planarization process (figure adapted from [54]).

ible polishing pad. Then the relative motion of feature to pad will cause a high pressure region on the feature's leading edge and, consequently, material is removed at a higher rate than at the feature's trailing edge. In agreement to this simplified view it is indeed observed that surface feature are planarized from their edges, e. g. profilometer scans show how the feature's steps are rounded during the planarization process (for an example see Fig. 4.15).

4.1.2 Optimizing global planarization characteristics

The pad's compressibility and elasticity module influence planarization behavior [9, 54]. As a result of the pad surface's deflection, planarization efficiency becomes feature width, height and pattern density dependent (Fig. 4.7). The planarization characteristics are mainly determined by the pad deformation length which is the length to which the pad can conform or react to a surface feature. In case the distance in-between surface features is smaller than the planarization length of the polishing pad, the process planarizes these as one large-scale structure. Consequently, isolated features typically planarize faster than grouped (with higher pattern density).

For an optimized CMP process the planarization efficiency, and therefore the MRR, must be as equal as possible for all existing surface features. "Soft" pads generally yield excellent local planarization, i. e. lowest surface roughness, due to their small deformation length, but show inferior global planarization characteristics for large scale (wider) features. In case the pad deformation length is in the order of the feature height, model calculations predict a direct proportionality between these two variables [85].

Additionally, pad compression and, subsequently, the related effects increase with applied back pressure. Therefore process development always focuses on utilizing "hard" pads in combination with low back pressures (typically $< 8\,\mathrm{N/cm^2}$, 10 psi) in order to reduce the polishing pad compression to an as low value as

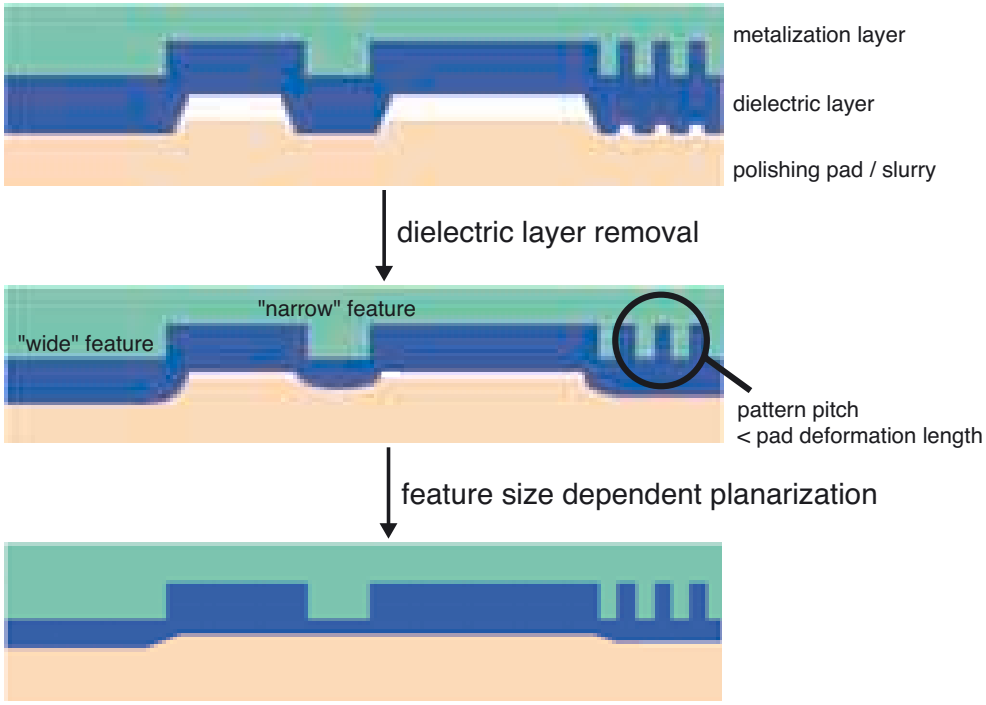


Figure 4.7: Schematic cross-section through polishing pad and wafer interface during CMP (face down orientation as during polishing). A real polishing pad exhibits compression which leads to pattern density and feature size dependent planarization efficiency. Thus perfect local and only incomplete global planarization can be achieved under real conditions. Circuit sketches adapted from [77].

possible.[5] A supplementary soft pad touch up polish can be used in case dielectric surface roughness is a problem. The KOSMA CMP process only employs one hard planarization pad.

A rotary type polisher requires a co-rotating wafer carrier (polishing head) for uniform material removal. The ratio between the angular frequencies of pad and carrier must be unity as otherwise the speed integral over one wafer rotation, and at the same time the MRR, increases along the wafer's radius [54].

The geometry of the wafer carrier also plays an important role for the planarization results. During the polishing process the wafer is positioned into a recess at the carrier's underside. The amount the wafer surface extends above the surrounding contact surface is referred to as the "wafer extension" and determines the wafer-pad contact mode, e. g. direct contact, semi-direct contact or hydroplane sliding (Fig. 4.9).

The cause for this lies in the pressure distribution between wafer and the retaining ring. Especially the semi-direct mode is interesting for application. Due to the roughness of the pad surface and the wetting slurry film the retaining ring starts to take over some of the applied back pressure for small wafer extensions $< 100\,\mu$m,

[5] The situation actually is more complicated because the pad's compressibility itself is pressure dependent.

i. e. it acts as an additional contact surface to the pad. It is observed that this load distribution constricts the complex dependencies in the Preston equation to a simple linear relationship between the slurry silica content (by mass) and the MRR for a wide velocity range and given back pressure [9, 8].

4.1.3 Deposition of dielectric layer

The initial dielectric film thickness is determined by the material removal necessary for sufficient planarization. This thickness must be evaluated for every circuit layout as it depends on the lateral feature size and height dependent planarization efficiency at the point of interest. For principle understanding, the CMP process can be simplified to a sequence of two independent steps: First, is the planarization of the wafer topography and, second, the bulk material removal until the process is terminated.[6] Whereas the duration of the first step and with it the necessary amount of dielectric thickness reduction is predetermined by the (ideally speed optimized) planarization efficiency of the process, proper process development focuses on minimizing the need for bulk removal. Because the CMP process cannot improve the initial global thickness uniformity of the dielectric, care has to be taken for an uniform as possible deposition process.

The initial thickness of the deposited dielectric layer is primarily empirically evaluated to yield the minimal necessary value, but following dependency between the current feature height h_c, its initial height h_i and the already removed dielectric thickness d_r aids process development:

$$h_c(d_r) = h_i \, e^{-cd_r}. \tag{4.2}$$

Here c is a pad deformation dependent constant [9]. Dependent on exact process conditions, a initial dielectric thickness to h_u ratio ranging from 1.5–3 is typically employed in order to yield sufficient planarization.

4.2 Planarization process development

First a short introduction to the process prototyping activities prior to this thesis' work will be given. Results from these studies will not be discussed here and only be referred where needed. Then the current design and setup of the CMP process and the operation procedures as are now used at a regular basis for e-beam junction fabrication are presented in detail.

4.2.1 Process prototyping with modified lapping machine

The studies from [8, 9, 4] at Stony Brook, SUNY were chosen as a starting point for CMP development due to the fact that they were developing a Josephson circuit

[6] Of course, there is a continuous transition from planarization (most commonly with substantially higher MRR) to pure bulk removal in reality.

Figure 4.8: Prototype CMP setup during the initial stages of this PhD work, resulting from foregoing diploma thesis [58]. The polishing machine is a lapping machine (Logitech PM4) modified with self-constructed wafer carrier, motorized polishing head and slurry delivery line. The pictured polishing head (old monolithic version) consists of a brass body combined with a (white) wafer carrier made of Delrin™ (an acetal homopolymer & copolymer thermoplastic) which has been superseded by new designs (see Fig. 4.12 and Fig. 4.13).

fabrication process based on PARTS and e-beam lithography.[7] Process development at KOSMA started out with a diploma thesis in which principle, empirical understanding was gained and the feasibility of this process within available resources demonstrated [58].[8]

The prototype CMP setup consisted a standard, commercially available PM4 lapping machine from Logitech, which was modified for the CMP process with a self-constructed wafer carrier and motorized polishing head construction (Fig. 4.8). The setup was positioned outside of the cleanroom due to continuing lapping activities [60]. These positive results led to here presented PhD thesis which carried on with process development, advancing it to sufficient performance for integration into an e-beam lithography based SIS device fabrication (with the e-beam development work discussed in Chap. 3).

An important early finding was that the fragile fused quartz wafer, on which the waveguide-based SIS devices are fabricated on, are too difficult to handle and, most importantly, not robust enough for safe CMP processing. Therefore process development successfully focused on bonding the quartz wafer onto a 2 inch sil-

[7] Josephson and SIS devices are essentially the same, in particular both use Nb-Al/Al_2O_3-Nb trilayer technology and require submicron area junctions.

[8] Besides from quartz and silicon wafer backlapping there was no processing experience with CMP and the outcome of these early experiments could not be foreseen.

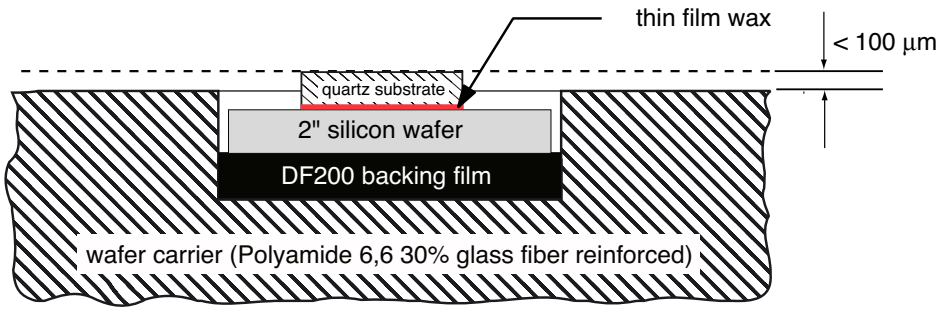


Figure 4.9: Schematic cut through wafer carrier with mounted quartz wafer. The recess depth of the carrier is matched to the total thickness of the backing film and quartz / silicon carrier wafer combination in order to yield a wafer extension of approximately 100 μm. Thin film wax is used to bond the 270 μm thick quartz wafer to the 290 μm thick silicon carrier wafer yielding a thin 1–3 μm adhesion layer. The wafer combination is held onto the wetted sponge-like backing film solely by surface tension. See App. C for a technical drawing of the wafer carrier with measurements.

icon wafer for higher mechanical strength during polishing (i. e. a "piggy-back" method, see Fig. 4.9 and Fig. 4.13) [60]. This had the additional advantage that the resulting geometry was close to the one used in [9] and thus helped in rationalizing process development by using the published processing parameters, notably wafer extension and back pressure, as a starting point (at Stony Brook 2" silicon wafers are used as substrate material and thus no additional reinforcement is needed, see Sec. 4.2.3). For equal reason the (industry standard) consumables from Rodel were chosen (see Sec. 4.2.4).

At the time when CMP process development at KOSMA started, SiO was being used as standard dielectric material for UV-SNEP SIS devices. For that reason, first CMP experiments used SiO for the tuning dielectric / junction insulation layer, deposited through standard resistive evaporation [58]. Although devices with SiO as dielectric were successfully fabricated yielding high quality DC I-V characteristics, further development work clearly indicated that SiO film adhesion on the devices was not sufficiently high enough for safe CMP. In order not to degrade device yield during polishing it was therefore decided to switch to SiO_2 as dielectric material, which demonstrates significantly better film adhesion. From there on no yield decrease due to delayering of the dielectric has occurred.

Initially, e-beam evaporation was used for SiO_2 deposition, but this method suffered from irreproducibility of the total film thickness and inclusion of impurities with the system used.[9] Subsequently a RF magnetron sputter cathode was inte-

[9] It is difficult to achieve a stable low deposition rate during e-beam evaporation due to runaway heating effects in the SiO_2 pallet and subsequent large increase of material volatilization. The beam current must be constantly corrected manually in order to yield a stable deposition rate and, hence, reproducible film growth. The accuracy of the deposition rate monitor is impaired with proceeding deposition, though, as the electron beam spot slowly works its way into the pallet, yielding a nozzle like focusing of the SiO_2 vapor. The impurities result from the difficulty of adjusting the oscillating the e-beam spot on the pallet in order to reduce before mentioned focusing

Figure 4.10: IBS PT 350 CMP polisher with IBS polishing head and self-constructed wafer carrier underneath (black material, see Fig. 4.13) during a test run. The slurry delivery line is made up of the white slurry holding tank to the left and the diaphragm pump, placed at the left rear of the polisher, which secures constant flow rate.

grated into dielectric deposition system which greatly simplified the deposition process. As with any sputtering-based system the deposition rate is a clear function of applied RF power and a very stable deposition rate as well as thickness uniformity across the wafer is achieved. The deposition is intrinsically clean as the material removal is confined to the SiO_2 target through the magnetron construction. The established process parameters for deposition are given in App. A.1.

4.2.2 Dedicated CMP polisher

Based on the acquired empirical knowledge and achieved results it was concluded that it was time to purchase a dedicated CMP setup for installation in the micro fabrication laboratory. Due to the lack commercially available (resp. budget compatible) products a polisher with integrated polishing head drive was specified and designed in close cooperation with a commercial manufacturer.[10] Outcome of this cooperation is the IBS PT 350 CMP polisher with independently controllable pad and head drive rotational speeds in the range of 0–100 rpm (Fig. 4.10). From the start the roller arms, i. e. half-circle tangential arms which guide the polishing head during operation, were specified for the same polishing head diameter of 5"

of the SiO_2 vapor without reaching the contaminated edge of the hearth.

[10] I-B-S Fertigungs- und Vertriebs-GmbH, manufacturer of lapping and polishing machines. Postal address: Villenstraße-Nord 2, Postfach 30, 82284 Grafrath, Germany. email: IBS-Scholz@t-online.de, phone: +49 8144 7656, fax: +49 8144 7857

Figure 4.11: Close-up view of IBS PT 350 CMP polisher with monolithic polishing head (Fig. 4.12) during process. The electric motor powered roller for friction based forced rotation of the head is visible at the right end of the sweep arm. This setup was used for most of the results presented here.

so that the proven monolithic polishing head construction (consisting of a stainless steel load and polyamide wafer carrier, Fig. 4.11 and 4.12) could be taken over from the prototype setup. This guaranteed a smooth transition of polishing results during process switch-over from the Logitech to the IBS polisher while using the same processing parameters.[11] In contrary to the prototype setup, which used a flexible, axial drive coupling from the DC motor to the polishing head body (Fig. 4.8), the IBS polisher uses one DC motor powered roller for friction based forced rotation of the polishing head (Fig. 4.11).

In comparison to the Logitech PM4, the polishing pad capability was increased from 300 mm to 350 mm diameter in order have sufficient potential for development of larger diameter wafer polishing in the future. Polishing head guidance is achieved by two rollers of either a sweep arm station, which can be oscillated with an amplitude in the range of 0–8° or a fixed roller arm station at three possible locations (Fig. 4.11). For example, the second station can be used for in-situ pad dressing with a conditioning block.

The polishing machine comes with an piston-action polishing head with detachable loading weights (in Fig. 4.10 a 24 N load is used, see Tab. 4.1 for possible selections). As with the simple, monolithic construction the underside of the head is a self-constructed wafer carrier (Fig. 4.13). This head has not played an important role during fabrication yet (June 2003), but the additional functionality certainly needs be exploited in the near future (see further discussion in Sec. 6.3).

[11] As explained previously, the wafer carrier geometry has the biggest influence on the planarization characteristics.

Figure 4.12: Monolithic polishing / head wafer carrier construction. The loading force is fixed by the weight of the stainless steel (V4A) body to an optimized value of 26 N. The black wafer carrier (100 mm diam.) is a precisely turned and lapped disk of mechanically and chemically resistant polyamide material (see Tab. 4.1) and bonded to the steel body (white silicon rubber sealing can be seen at the edge). The recess is 1.27 ± 0.01 mm deep and lined with Rodel DF200™ backing film.

4.2.3 Design and construction of wafer carrier

A correct geometry of the wafer carrier is vital to the CMP process as it influences the pressure distribution ratio between the wafer surface and retaining ring, therewith determining the planarization behavior (Sec. 4.1.2). The studies at Stony Brook helped during the wafer carrier design of the KOSMA polishing heads. This results to similar geometrical layout for the different wafer carriers evaluated during CMP development, all aiming at the cited beneficial semi-direct contact mode polishing regime [9].

In particular, the recess depth is designed to yield a small wafer surface extension of 100 μm or less. The wafer carrier's diameter of 100 mm leaves room for an approx. 1" wide retaining ring (contact surface) which is comparable to the Stony Brook setup published in Ref. [9].

The development efforts undertaken during carrier design can be categorized into three points of interest:

1. Optimization of carrier recess depth
2. Optimization of loading weight
3. Search for best carrier material

Figure 4.13: Placement of the quartz / silicon carrier wafer combination into the self-constructed wafer carrier attached to the underside of the IBS polishing head. The recess is lined with Rodel DF200 backing film. This latest version includes grooving of the contact surface in order to enhance slurry flow towards the wafer and is not yet qualified for processing.

The first task is made complicated by the use of a compressible and deformable backing film on the recess surface. As early experiments indicated, this is important for achieving an even MRR across the wafer surface by smoothing out the pressure distribution from the loading weight [60]. The Rodel DF200™ backing film[12] compensates for any roughness and, to a certain extend, any residual non-coplanarity the recess surface has in relation to the polishing pad. The DF200™ film is specified to be $635 \pm 50\,\mu$m thick which is not precise enough for recess depth calculation by straightforward summation of the quartz wafer, silicon wafer and adhesion layer thicknesses. For this reason the recess depth has to be matched on a per batch basis to the DF200™ film. The recess depth values given in Fig. 4.9 and Tab. 4.1 are measured with a digital gauge to one micron precession by comparing the absolute heights of the wafer combination placed onto the wetted DF200™ film with the contact surface. It is observed that a backing film thickness of around $760\,\mu$m for the current batch of DF200™ film to be assumed in order to achieve the correct wafer extension values which is well outside the specifications given.

Due to the compressibility of the backing film these values are assumed to be significantly larger than those taken on during polishing, when the backing load is

[12] N. BUCHER AG, supplier of Rodel CMP products (ILD1200 slurry, IC-1000 pads and DF200 backing film) and PVA sponges in R&D quantities. Postal address: Pfadackerstrasse 9, 8957 Spreitenbach, Switzerland. email: nbucherag@swissonline.ch, phone: +41 56 4181 990, fax: +49 56 4181 999

polishing plate	350 mm diam. 0-100 rpm rot. speed range
polishing head	piston with recoil moment 5” outer diam. 0-100 rpm rot. speed range
loading force selection	1× 20 N / 1× 24 N / 2× 9.5 N 58 N (11.4 N/cm^2 back press.) total
wafer carrier	PA 6,6 (30% glass fiber reinforced) 100 mm outer diam. 52 mm recess diam. 1.295 ± 0.005 mm recess depth 18 mil DF200 backing film
wafer extension	approx. 100 µm
pad conditioner	Logitech 1ACCS-0700 40 µm diamond 5” diam. 34 N loading force

Table 4.1: Technical specifications of the IBS350 PT 350 CMP setup with new IBS polishing head (Fig. 4.13). The back pressure is calculated in relation to the quartz wafer area. The wafer extension is measured in the unladen condition for a 290 μm silicon wafer and 270 μm quartz wafer combination on wetted Rodel DF200 backing film.

applied to the wafer. This may be an explanation for the observation that a recess depth of less than 50 μm leads to a vanishing MRR. Additionally, this has the consequence that the real pressure ratio distribution between wafer and contact surface is undetermined and thus wafer back pressure (Tab. 5.1) generally are difficult to compare.

For obvious reasons the wafer thickness becomes important for polishing process and must be specified with narrower tolerances than for non-CMP fabrication. The specifications for the supplier of the fused quartz wafer[13] now are set to 270 $\pm$ 10 μm as compared to 250 $\pm$ 50 μm previously.

With a monolithic head design the total mass of the polishing head sets the back pressure value. Due to the different requirements to the load and wafer carrier material a two-piece construction is made necessary. The load body should be a high density (metal) construction in order to reduce the polishing head size and lower the center of gravity in order to yield more stable mechanical polishing characteristics. In contrast, criterion for material selection for the wafer carrier is that it should be softer than the silicon wafer in order to reduce the risk of grinding or chipping the silicon wafer edge, as the silicon wafer can slightly move in the recess during polishing. Additionally, the material should be abrasion-proof and

[13] LINOS AG. http://www.linos.com

chemically inert to the alkaline slurry and, finally, precisely machinable on a lathe.

First generation polishing heads were a brass load and Delrin™ (an acetal homopolymer & copolymer thermoplastic) construction but the easy machinability of the brass body had to be dropped for a chemically far more resistant V4A stainless steel in order to avoid possible contamination problems during handling. Noticeable wear of the Delrin™ carrier initiated a search for a more suitable material which is found with polyamide PA6,6, 30% glass fiber reinforced.[14] This material exhibits very good chemical and mechanical resistance while being adequately machinable. No measurable wear after more than 30 CMP processes is observed.

Due to the two-piece construction care has to be taken to ensure a center of gravity on the head's centerline. Following successful procedure has been worked through with the staff at KOSMA's fine mechanics workshop in order to ensure plane coplanarity of all surfaces:

1. turn polyamide disk (and outside retaining ring for new head design) on lathe (11 mm thickness, less causes deformation)
2. saw grooving and bevel edge of disk on contact surface side / retaining ring
3. turn stainless steel load body on lathe
4. join polyamide disk / retaining ring with load body
5. lap polishing head construction on Logitech PM4
6. turn recess into polyamide disk on lathe

Total error of manufacturing reproducibility and planarity deviation for recess depth turning is less than 20 μm, which seems adequate for the CMP process. Tab. 4.1 sums up all important data concerning the polishing machine and polishing head.

4.2.4 Polishing pad and slurry

With the Rodel IC-1000/Suba IV™ the same type of industry standard, dual layer polishing pad is used as in [9]. The low compressibility of the IC-1000™ top layer makes this pad especially suited for planarization processes while the softer Suba IV™ layer underneath secures global uniformity similar to the DF200™ film. Perforation in the top layer functions as a slurry reservoir during polishing and secures constant slurry delivery to the polishing interface. The polishing pad is dried after processing and, as only one type of polishing pad is employed, can be kept on the polisher protected by a dust cover.

[14] GOODFELLOW, supplier of metals, polymers, etc.. http://www.goodfellow.com

Rodel ILD1200™ slurry is used, which is a alkaline KOH based polishing fluid containing fumed 130–210 nm diameter silica particles as abrasive component. The slurry is diluted with ultra pure / de-ionized water in order to yield a 3% (by mass) silica content to a sufficient amount (750 ml) prior to the CMP process. The slurry holding tank is equipped with a magnetic stirrer in order to reduce slurry particle agglomeration (see Fig. 4.10, and additional comments in Sec. 6.3). Constant slurry flow is achieved by a diaphragm dosing pump and ensures reproducible processing conditions. The slurry flow is adjusted to yield an evenly wetted polishing pad. There is no filtering in the slurry line.

The polishing process glazes the pad surface and reduces its (microscopic) roughness which, consequently, reduces the MRR and strongly affects the planarization characteristics. Additionally, pad planarity is affected through abrasion by the wafer carrier and must be correct. Especially the pad influence on the MRR should stay constant for the duration of each polishing step so that the dielectric layer removal can be extrapolated more precisely. For prevention, pad conditioning steps have to be carried out either in-situ, i. e. during the polishing process on an additional station, or ex-situ, i. e. in a sequential manner, before this deterioration is noticeable. The required frequency must be empirically found. Pad conditioning requires a tool with hard material that must not contaminate the polishing pad. The KOSMA process uses a Logitech diamond pad conditioner in an ex-situ process (see Tab. 4.1 for conditioner data and Tab. 4.2 as well as Tab. 4.3 for conditioning process relevant data).

slurry preparation	
1. mix	prepare 750 ml solution per batch
2. stir	turn on magnetic stirrer (≥ 30 min prior to process)
3. flush slurry line	activate diaphragm pump with maximum flow setting (0.5 min)
pad preparation	
4. rinse	750 ml H_2O, spin off / N_2 blow
5. pre-conditioning step 1	position conditioner at 1/3 radius 5 min @ 80 rpm (pad) / 80 rpm (head) continuous H_2O flow (total 250 ml)
6. pre-conditioning step 2	position conditioner at 2/3 radius 5 min @ 80 rpm (pad) / 80 rpm (head) continuous H_2O flow (total 250 ml)
7. soak	H_2O, keep wet for process (250 ml)

Table 4.2: CMP startup procedure for a dry polishing pad. The H_2O is ultra pure / de-ionized.

4.3 Guide to operation

SIS waveguide devices are fabricated on fused quartz wafer because of the RF chokes (see Sec. 2.2.2). The wafer used at KOSMA are less than 300 μm thick to ensure heat-sinking during trilayer film deposition and tunnel barrier oxidation. As the wafer's thickness and mechanical characteristics prevent successful CMP processing, the wafer is bonded to a stronger 2" diameter, 290 μm thick silicon carrier wafer for the CMP process. Very thin adhesion layers in the 1–3 μm range are reproducibly achieved with Logitech LCON-195 thin film wax, ensuring a coplanar alignment of the wafer combination with respect to the wafer carrier.

Following procedure is used to bond the wafer to the silicon carrier:
The silicon wafer is heated on a 100°C hot plate, a small piece of wax is molten on it and evenly spread out to approx. 20 mm diameter. Air bubbles in the wax layer must be avoided because they, firstly, reduce adhesion and, secondly, can deteriorate the planarization uniformity locally, probably by promoting wafer flexing. Therefore the fused quartz wafer is placed on the silicon carrier and moved to the edge of the wafer with tweezers. With the backward movement remaining air bubbles then are stripped from the wafer's underneath. After centering the wafer on the silicon carrier a 500 g (1.2 N/cm^2 back pressure) loading weight is carefully placed on top and the hot plate is simply switched off for a slow cool down in approx. 10 min.[15] For the same reason a short bake-out is employed prior to every subsequent polishing step so that the wax is enabled to re-flow into shear

[15] a simple, cylindrical brass body with a 24 mm diam. PTFE cap on the supporting surface

1. pad conditioning	5 min @ 1/2 radius position (analog startup procedure)
2. polishing head preparation	H_2O rinse of contact surface / wafer recess (ensure cleanliness of backing film)
3. pad charging	1 min, with slurry feed and polishing head 20 rpm (pad) / 24 rpm (head)
4. cure wax bonding layer	15 sec. HP @ 100°C [*not used for step no. 1*]
5. CMP preparation	wet wafer combo and backing film (H_2O)
6. process polish	3 min [*reduce to 0.5 min for final CMP steps*] position at 1/2 radius 20 rpm (pad) / 24 rpm (head)
7. slurry removal	1 min [*reduce to 0.5 min for final CMP step*] continuous H_2O flow (250 ml)
8. soak pad	keep pad wet for next step / wafer (H_2O)
9. in-between wafer combo clean / dry	keep wafer wet 0.5 min H_2O (UA), 0.5 min IPA (UA) spin dry (N_2, IPA blow)
10. metrology	measure dielectric thickness calculate remaining polishing time
final clean [*used after last step*]	scrub wafer combo (2 % NH_4OH, PVA sponge) H_2O rinse, 1 min H_2O (UA), 0.5 min IPA (UA) spin dry (N_2, IPA blow)

Table 4.3: Description of the established CMP sequence. This sequence typically is run 4–6 times to complete the planarization process. The quartz / silicon carrier wafer combination stays together until CMP is finished. The curing step removes air bubbles in the thin film wax bonding layer which can occur due to the shear forces during polishing. Additionally, the wax film re-flows to the quartz wafer edge in order to fix the damage to its consistency made by previous UA cleaning step. CMP is finalized with a manual NH_4OH scrub. (abbr.: HP = hot plate, UA = ultrasonic agitation, IPA = Isopropanol, PVA = Polyvinyl Alcohol)

force induced discontinuities within the layer and to form a closed interface at the wafer edge (where the alkaline property of the slurry slightly affects the thin film wax).

Following lists the actions required during a CMP run:

1. chip: bond quartz wafer to silicon carrier
2. slurry: prepare sufficient amount
3. polishing pad: initial cleaning and conditioning
4. CMP sequence *[repeated 4–6 times]*
   (a) wafer carrier: clean
   (b) polishing pad: condition and soak with slurry
   (c) **planarize chip**
   (d) chip: intermediate clean
   (e) inspection: metrology, calculate duration
   (f) chip: cure wax layer
5. post-CMP clean with NH_4OH
6. end-point confirmation: inspection and metrology
7. chip: remove from silicon carrier

Tab. 4.2 and Tab. 4.3 describe the initial steps for preparing the polishing machine and polishing pad and the established process sequence of one CMP run with all relevant data, respectively. In addition, the CMP process is also given as part of the complete 490EBL process recipe in App. A.1.

Due to the fact that the observed bulk MRR on top of the determining tuning dielectric regions is not reproducible enough from wafer to wafer, a one-step, blind polish approach cannot be performed.[16] Consequently, the CMP process has been optimized to a rather low mean bulk MRR around 40 nm/min and is carried out in 4–6 individual steps of up to 3 minutes length. The dielectric layer's thickness is determined after each step from whereupon the next polishing step's duration is decided. The last step typically has a duration of no longer than 0.5 min.

Altogether three complementing methods are used for determination of the dielectric thickness and confirmation of end-point achievement. These are based on profilometer measurements with a mechanical stylus[17], determination of the interference colors of the tuning dielectric and visual confirmation of junction top electrode clearance through inspection with a light-optical microscope.

[16] See Sec. 6.3 for further discussion and approaches for resolving this issue.
[17] Alpha Step 100

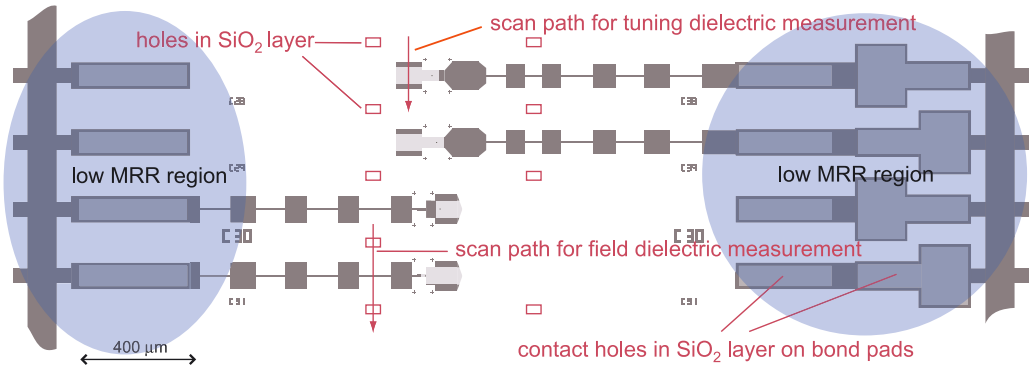


Figure 4.14: Illustration of a small portion of the 490EBL circuit layout showing the device features to be planarized by CMP (devices C28–C31). Openings in the dielectric blanket layer are defined in-between the devices ("field dielectric" position) and an the bond pads (contact holes). Profilometric scans of the field dielectric holes and the tuning dielectric topography allow calculation of the remaining dielectric thickness at the junction position for each device measured. The toned areas mark regions with large scale features that locally lower the MRR. The second half of the RF chokes and the integrated tuning circuit top electrode is defined after CMP.

A profilometer scan is the preferential measurement method as it achieves a resolution of less than 5 nm and, as it is cross-calibrated with other processes, delivers reliable absolute values. Since the dielectric is deposited as a blanket layer, i. e. covering all of the circuit's surface, holes are defined in this layer in-between the devices ("field dielectric") and on the bond pad structures, where they additionally serve as contact openings for later deposited metalization (see Fig. 4.14 and Sec. 5.4.2). Definition is achieved through an UV photolithography process with image reversal resist and lift-off of the resist features after deposition and prior to the CMP process. In contrary to the large scale bond pad features which only can be used for initial thickness measurement the field dielectric features are small enough ($50\,\mu\text{m} \times 30\,\mu\text{m}$) to keep a sufficiently steep edge profile during most of the planarization and thus aid the profilometer measurements.

After every CMP step the dielectric thickness uniformity is calculated from decrease of the holes depth for at least 15 uniformly distributed devices. It must be noted that the measured dielectric thickness, and subsequently the calculated bulk MRR, does not represent the exact value at the determinant tuning circuit position of the measured device (the MRR on top of the device is much higher during initial planarization stages, see Fig. 4.16). Nevertheless the remaining dielectric thickness at the junction position is computable to approx. $\pm 10\,\text{nm}$ error through measurements of the field holes depth and the profile on top of junction dielectric (as illustrated in Fig. 4.14). Parallel color determination by visual inspection through a light-optical microscope and comparison with a color chart double-checks these values (see color chart in App. A.3).

Finally, after the last or last but one CMP step, clearance of the junction top electrodes can be directly observed on the large area ($\geq 4\,\mu\text{m}^2$) junction top elec-

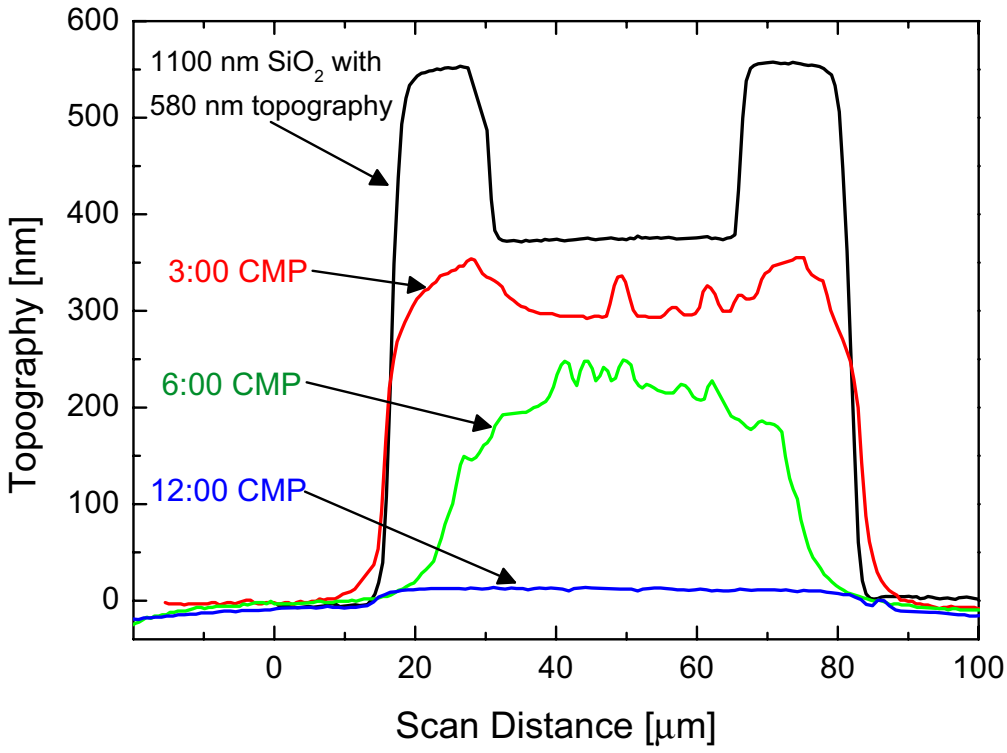


Figure 4.15: Composite of four profilometer scans across a device (i. e. SiO_2) at four different stages illustrating the planarization process. The four identical scan paths go across the tuning dielectric, i. e. the junction insulation window, of one identical embedded trilayer type device (chip PSK-4) before, during and after the CMP process. For orientation the profilometer scan path is illustrated in Fig. 4.14 for a standard trilayer devices. See text for additional information.

trodes. The aluminum RIE mask, which is left in place after RIE definition of the junction, provides a large image contrast difference when compared to the niobium top electrode material underneath and is immediately attacked by the alkaline slurry when the covering dielectric layer is removed. Herewith a precise and independent indication for the remaining dielectric thickness at the junction is given as the layer thickness error of the metalization layers is only a few percent.

Fig. 4.15 shows a composite of four profilometer scans across the tuning dielectric region of one embedded trilayer type device at four different stages of the planarization process. It is evident that the underlying, structured metalization layers produce a 580 nm high topography and that the depth of the RIE structured junction insulation window corresponds to the trilayer thickness of approximately 200 nm. The planarization process was terminated after 12 min. total polishing time. The waviness of the intermediate scans results from adhering slurry particles on the SiO_2 surface which are not removed until the final NH_4OH scrub.

Fig. 4.16 reveals CMP typical planarization behavior at exemplary device D36 of standard trilayer type chip 490EBL-2, whose global planarization result is presented later on in Fig. 5.11. The decrease of tuning dielectric planarization rate (MRR on top of the tuning dielectric area) with proceeding total polishing dura-

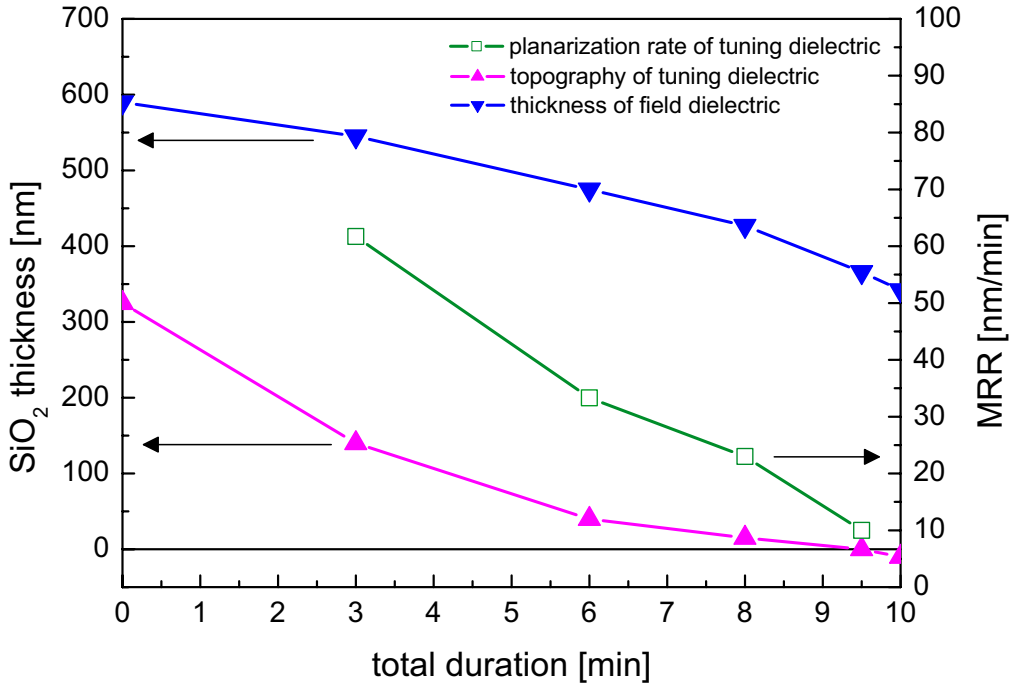


Figure 4.16: Reduction of dielectric thickness at field position and tuning dielectric topography with increasing total polishing duration for exemplary device D36 of chip 490EBL-2. The corresponding material removal rate for planarization of the tuning dielectric topography is given on the right ordinate. Initial SiO_2 thickness is 590 nm and initial topography height resulting from underlying metalization is 325 nm. Corresponding profilometer measurement scan paths are again illustrated in Fig. 4.14.

tion is clearly visible, as well as the planarization process underlying unequal material removal at the tuning dielectric and field dielectric measurement positions is demonstrated. Initial dielectric thickness is 590 nm which is 1.8× larger than the 325 nm trilayer thickness value. Generally speaking, the developed planarization process is optimized for an initial dielectric thickness of only 1.5× more than existing device (topography) height.[18]

Two different chip cleaning processes are used after polishing, dependent on the sequence number of the CMP run (Tab. 4.3). In-between (intermediate) cleaning after all but the last CMP step is essentially only a drying process with a short ultrasonic agitation process in H_2O and subsequent drying with IPA (isopropanol) and N_2 on a wafer spinner. The wafer combination is kept wet during transfer from the polisher to the cleaning beakers in order to reduce the amount of particle sticking the wafer surface. Although this clean does not remove all slurry particles from the wafer surface it provides a sufficiently residue-free surface for the profilometric measurements (Fig. 4.15) while reducing the risk of mechanical defects.

[18] With here presented 490EBL-2 chip the trilayer thickness was unintentionally reduced due to re-calibration of the niobium sputtering rates thus increasing the initial dielectric to topography ratio.

For complete removal of adhering slurry particles after completion of CMP a more thorough cleaning process has been developed which involves physical particle removal with a PVA (polyvinyl alcohol, a high-porosity, hydrophilic material) sponge. After CMP the sudden drop in pH during removal from the pH = 10.5 slurry environment causes the slurry particles to lose their positive surface charge and promotes sticking to the wafer surface. For this reason a pH raising solvent, i. e. a mild 2% NH_4OH solution, is used during scrubbing so that the particles do not stick back on the wafer surface. After a thorough H_2O rinse the cleaning is concluded by before mentioned intermediate clean procedures.

5

Results of device fabrication

During the final stages of process development e-beam junction definition and CMP planarization has been integrated into regular device fabrication of the HIFI Band 2 mixer as well as the 475 GHz SMART devices. While development of the HIFI Band 2 devices fabrication process is outside of the topic of this PhD thesis and shall only be given as reference [19, 59, 20], the 490EBL process will be described in detail. The 490EBL process is representative for standard Nb-Al/Al_2O_3-Nb type devices with all-Nb tuning circuits. In particular, the circuit layout of the 490EBL photolithography mask (e. g. needed for large scale structures such as the RF chokes) will be discussed with regard to CMP process compatibility. Because the 490EBL circuit layout incorporates latest CMP planarization know-how, the planarization capabilities of CMP will be discussed regarding a wafer using this layout. Nevertheless RF performance results for a typical HIFI Band 2 device will demonstrate the capabilities of the the e-beam / CMP process and are be presented at the end of this chapter.

DC I-V characteristics play the central role for analysis of SIS device and consequently fabrication quality. At first the measurement method for efficient analysis of all junction areas on a wafer is explained. E-beam definition quality, expressed through junction area reproducibility, then will be exemplified for a standard Nb-Al/Al_2O_3-Nb type wafer with all-Nb tuning circuits, e. g. like the 490EBL devices, and then for an embedded trilayer type wafer of HIFI Band 2 mixer device development. Presentation of e-beam definition of the tuning circuit top electrode follows.

Concerning CMP the optimization of the planarization process is discussed and a typical planarization result for a 490EBL wafer will be presented. DC I-V characteristics of Band 2 mixer devices then will demonstrate the significant beneficial influence of CMP on device characteristics.

RF evaluation of the devices, i. e. evaluation of noise temperature and RF bandwidth, shows that the e-beam definition process of the tuning circuit top electrode causes deterioration of the superconductor material quality. Comparison with devices which use conventional UV photolithography for the tuning circuit but e-beam junction area definition, rule out a negative influence of e-beam junction

definition on the device quality. RF results of HIFI Band 2 mixer devices, which consequently omit the e-beam definition step for the tuning circuit, will demonstrate that the e-beam / CMP process scheme does produce high performance SIS mixer devices under this constraint.

5.1 490EBL fabrication process

The latest fabrication scheme to utilize e-beam definition and CMP planarization is the 490EBL process. This process uses the photomask described in Sec. 5.4.4 for definition of the 475 GHz devices for KOSMA's SMART and, in collaboration with LERMA, the backup devices for the HIFI Band 1 (480–640 GHz) of the Herschel Space Observatory. The 490EBL devices rely on conventional UV photolithography for tuning circuit top electrode definition (see Sec. 5.3 for explanation). As the both frequency bands stay below the niobium gap frequency ($\approx$ 690 GHz), fabrication uses standard Nb-Al/Al_2O_3-Nb technology with plain niobium tuning circuits.

In the following the fabrication scheme will be sketched with help of Fig. 5.1. A detailed listing of all process data, i. e. the complete processing recipe, can be found in App. A.

Starting with a 25 mm diameter fused quartz substrate (INFRASIL, LINOS[1]) of 270–290 μm thickness a Nb-Al/Al_2O_3-Nb trilayer (150 nm Nb base / 8 nm Al / 230 nm Nb top) is sputter-deposited as a blanket layer. In doing so the Al layer is in-situ oxidized in the load-lock to form the 1–2 nm thin Al_2O_3 tunnel barrier before sputtering of the top Nb layer. The required $R_N \cdot A$ product of the barrier is set using the empirical, (equipment-)calibrated Pa·s relation (e. g. discussed in detail in [46]). For the 490EBL devices a 10 min O_2 exposure at a static pressure of 1.6 Pa yields the prescribed 16 $\Omega\mu m^2$ (14 kA/cm^2).

The RF choke at the junction side of the device is defined with image reversal UV300 contact lithography (MJB3 mask aligner[2]) using AZ 5214 photoresist[3] and subsequent reactive-ion etch (RIE) of the trilayer. The trilayer is etched in a three-step in-situ process very similar to junction RIE of the embedded type HIFI Band 2 devices [19]: First, the Nb top layer is reactive-ion etched with the SF_6/CHF_3 based anisotropic process. Then the Al/Al_2O_3 layer is sputter-etched with Ar and after that the Nb base layer etch follows using the same parameters as for the Nb top layer.

After junction area definition through e-beam lithography and subsequent etch mask deposition and lift-off, the niobium junction top electrode layer is reactive-ion etched with the SF_6/CHF_3 recipe (see Chap. 3.2.5). Then 600 nm SiO_2 is deposited onto the whole wafer through RF sputtering for the tuning circuit dielectric and junction insulation layer with the thickness being approximately the

[1] LINOS PHOTONICS GMBH & CO. KG. http://www.linos.de
[2] SÜSS MICROTEC. http://www.suss.com
[3] AZ ELECTRONIC MATERIALS, CLARIANT. http://www.azresist.com

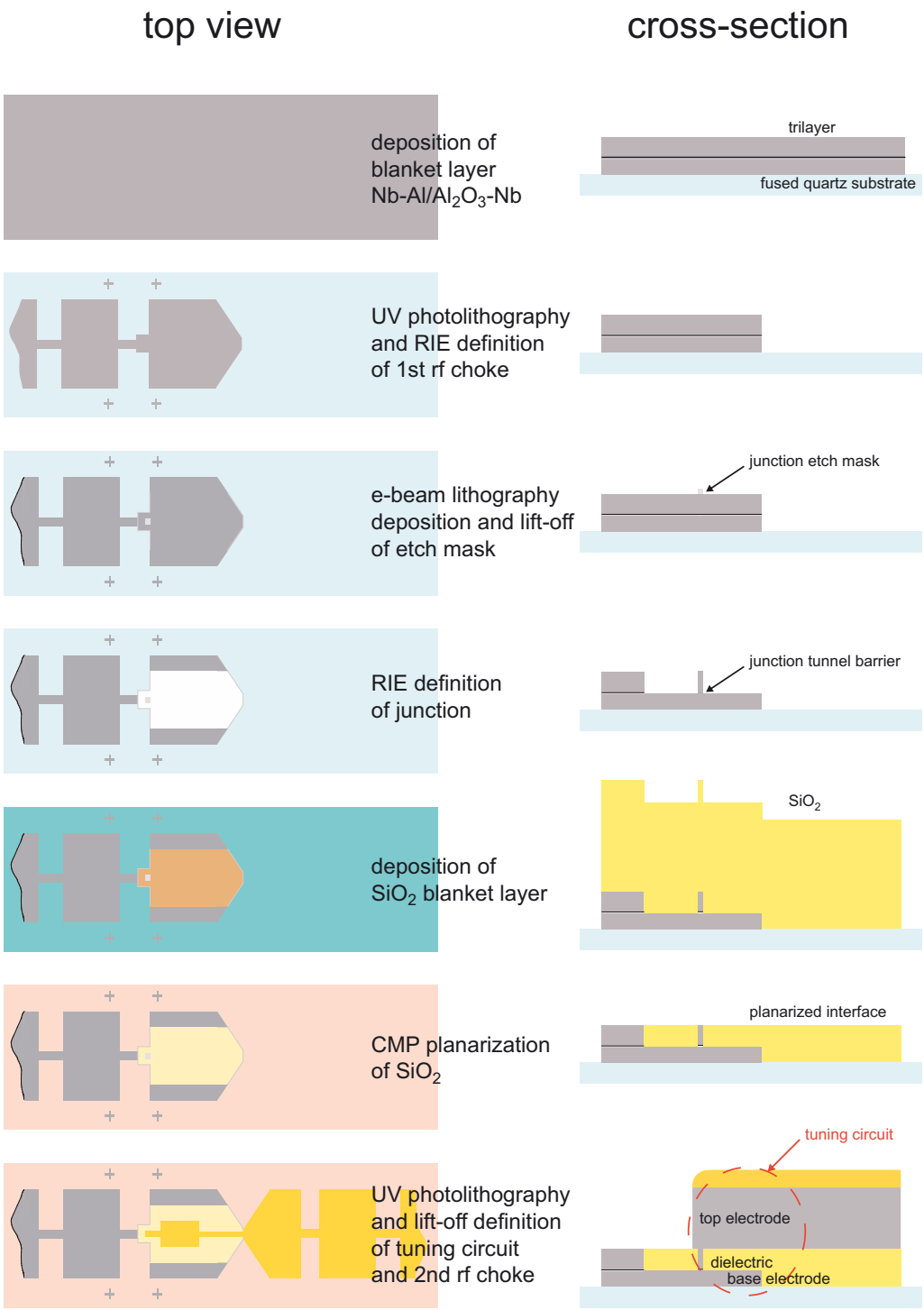


Figure 5.1: Schematic fabrication process sequence for the 490EBL devices. Left column shows a top view onto the junction area of a device and right column shows a cross-section through the layers. For clarity reasons some processing steps are omitted.

CMP required 1.5× the height of the topography generated by the metalization layers underneath. Lift-off defined holes are used for profilometric dielectric layer thickness control during the CMP process as explained in Chap. 4.

Next follows the CMP process during which the fragile quartz wafer is stuck onto a 2" diameter, 290 μm thick silicon wafer. CMP is terminated with the remaining dielectric thickness being 200 ± 20 nm for the integrated tuning circuit to work as designed. Then follows the definition of the top metalization of the device. This includes the integrated tuning top electrode, the second half of the RF choke and waveguide probe, the bond pad reinforcement layers and alignment marks for dicing. This is carried out through UV photolithography and subsequent sputter deposition of the metalization layer and lift-off. The 350 nm thick Nb layer is supplemented by an additional 30 nm gold layer for bond adhesion and passivation.

5.2 E-beam definition of junction area

Before the fabrication results relating to achieved junction area reproducibility are presented and discussed, it is necessary to explain the utilized methodology for precise and efficient submicron area measurement.

5.2.1 Measurement procedure

In order to control and verify junction area reproducibility of the fabrication process, a precise and effective measurement method which delivers reliable data for every single of the typically 200–250 junctions on a wafer has to be conceived. As pointed out in Sec. 2.3.3, relative junction area accuracies should be 5% for 0.6 μm^2 and this consequently demands a measurement procedure which is accurate to only a few percent.

On-line wafer inspection through an optical microscope is very important for fabrication monitoring and is used for fast checking of the e-beam written junction area definition in PMMA in order to determine whether any significant process flaws have occurred and for inspecting overlay accuracy. This method can not provide sufficient precision for process development, though. Even at 1000× magnification[4] a submicron junction area of 0.64 μm^2 can only be measured with a 30% scatter, and thus this optical method does not provide the necessary resolution to optimize area reproducibility of fabrication.[5]

In contrast, SEM micrographs taken with the e-beam lithography system provide sufficient resolution and the well-calibrated measurement scale of the SEM translates into knowledge of an precise absolute area size (see Fig. 5.12). Assuming

[4] system based on a ZEISS AXIOSCOPE 100 equipped with a CCD camera and a PC running OPTIMAS image analysis software

[5] This empirical value is for measurement of the etch mask after lift-off. The accuracy of measurement of the precedent PMMA definition is even a factor 2 less due to the lack of image contrast. Of course, PMMA definition is the sensible point in time to judge junction definition, because at this stage e-beam definition can be repeated with a new PMMA layer.

an error in linear dimension measurement of 20 nm, the relative area accuracy is 4% for 1 μm^2 areas and 8% for 0.5 μm^2 and therefore meets the requirements for process development. Disadvantageous, though, is the time-consuming procedure involved with SEM operation and the necessity for adding a thin gold layer to improve image contrast. Especially latter point makes this method not feasible for online inspection during fabrication because the wafer then cannot be processed any further. Thus SEM micrographs can only be used for offline absolute scale calibration.

A significantly higher, albeit relative, area measurement accuracy can be obtained by measuring and comparing individual normal resistance values R_N of the devices during DC I-V characterization. I order to calculate the absolute device junction area values the knowledge of the wafer's $R_N \cdot A$ product or critical current density J_c is required from which the junction areas then can be calculated with the help of Eq. 2.5:

$$A_J = 100 \, \frac{\pi}{4} \, \frac{V_{gap}}{R_N J_c} \qquad [\mu\mathrm{m}^2], \tag{5.1}$$

while neglecting the the electron-phonon coupling factor. Here V_{gap}[mV] is the gap voltage and $R_N[\Omega]$ the junction normal resistance of the device measured at 4.2 K in a liquid helium (LHe) dipstick setup, and J_c[kA/cm^2] the statistically derived, critical current density value of the wafer (see below).

With a typical device resistance around 25 Ω for a high critical current density, submicron area junction and a conservatively estimated resistance measurement accuracy of 0.1 Ω, areas can be compared with a relative accuracy of approximately 0.4%. Advantageous over the imaging methods described above is that the actual, capacitance-defining tunnel barrier area of the junction is measured and not the top of the counter electrode. Therefore this method is primarily adopted for determination of junction area reproducibility within one wafer.

Setting a precise and reproducible J_c value during fabrication of Nb-Al/Al_2O_3-Nb tunnel junctions is difficult to achieve for the high J_c (> 10 kA/cm^2) required for a high-performance SIS mixer. The actual J_c value can vary up to $\pm$30% per wafer.[6] With only the junction R_N and V_{gap} being directly and precisely measurable quantities, it can be seen from Eq. 5.1 that J_c and A_J cannot be calculated independently from each other. The relative junction area uncertainty $\Delta A_J / A_J$ would mainly be determined by the relative error $\Delta J_c / J_c$ of the critical current density and, consequently, making calculation of junction areas with straight forward appliance of (5.1) too inaccurate for process control.

Therefore a statistical approach through linear regression is utilized in order to determine the J_c value for each fabricated wafer with more precision. For this purpose, devices with large junction areas $\geq 1\,\mu$m^2 specifically, incorporated into the mask design, are additionally DC characterized. Their reciprocal R_N is plotted against their nominal areas along with the data of all other devices of one wafer

[6] One of the reasons for developing SIS junctions with AlN barriers is that high J_c values can be fabricated more reproducibly due to the utilized non-thermal, plasma-based fabrication method [39]. Therefore these devices with AlN barriers may very well supersede the Nb-Al/Al_2O_3-Nb technology in the long term even for devices working below 1 THz, see Chap. 6 for more details.

as exemplified in Fig. 5.4. J_c then is calculated from the slope of the fit line under following assumptions:

1. there is a negligible variation of the J_c value across the wafer
2. the absolute area size deviation ΔA for the large area junctions is negligible
3. the largest junction areas are small enough not to exhibit self-limiting of the Josephson current

The validity of the first assumption cannot be investigated for here fabricated devices but it seems reasonable enough to assume sufficiently uniform Al base layer sputter-deposition and thermal oxidation processes during barrier layer fabrication. Second assumption is justified by investigation of the measured R_N spread from large junctions $\geq 1\,\mu\text{m}^2$ and SEM micrographs (e.g. see area reproducibility result for $1\,\mu\text{m}^2$ junctions in Fig. 5.5).

The validity of third assumption can be checked as given in Ref. [34] for the junction area sizes investigated here. Using a London penetration depth of $\lambda_L = 800\,\text{Å}$ and a critical current density $J_c = 1.4 \cdot 10^4\ \text{A/cm}^2$ (i. e. the 490EBL design value) in the approximation

$$\lambda_J \approx \frac{1.618}{\sqrt{2\,\lambda_L\,J_c}} \cdot 10^4 \qquad [\mu\text{m}] \tag{5.2}$$

this leads to a Josephson length $\lambda_J = 3.4\,\mu\text{m}$. Applying the identical "soft requirement" as in [34] this leads to a maximum allowable junction side length $L < 2\lambda_J = 6.8\,\mu\text{m}$. As the large area junctions used in this thesis have a maximum side length below $2\,\mu\text{m}$ (on the 490EBL mask $L_J \leq 1.7\,\mu\text{m}$), the self-limiting of the Josephson current is avoided.

In summary, this leads to following measuring procedure: R_N values are used to determine the area reproducibility and absolute area values are then calculated from these with the statistically derived J_c, backed by absolute scale calibration through SEM measurements. As the e-beam definition process proves to be intrinsically stable enough, only few SEM measurements are made necessary from time to time. The overall relative measurement accuracy of junction areas $\Delta A_J/A_J$ is therefore estimated to be always better than 2% for the junction areas measured for this thesis. For example, the total $\Delta A_J/A_J$ error resulting from the R_N measurement error and the J_c fit for the wafer discussed in Fig. 5.5 is estimated to be 1.5% in case the measurement error of the niobium gap voltage values is neglected.

5.2.2 Analysis of junction area reproducibility

Unlike CMP development the junction e-beam definition process has profited from previous experience made for HEB fabrication. Straight-forward implementation of existing e-beam lithography expertise resulted in significantly improved junction area reproducibilities for areas below $1.0\,\mu\text{m}^2$ right from the point in time

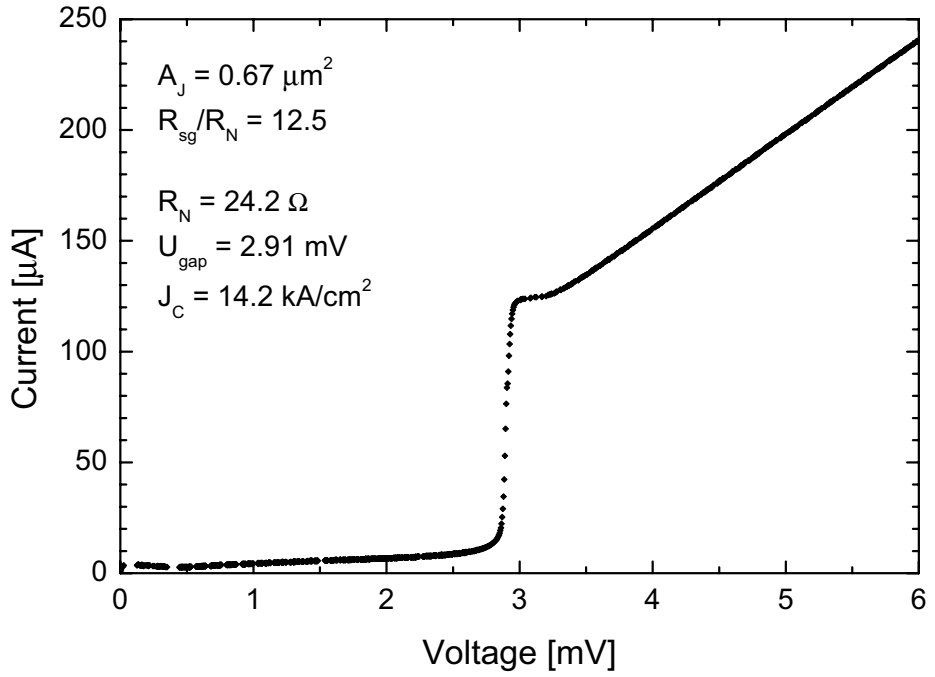


Figure 5.2: Typical DC I-V characteristic of an e-beam / CMP processed device of standard trilayer type with submicron area sized junction of high critical current density, measured in a LHe dipstick setup at 4.2 K (device 040401-CMP-ii-B19).

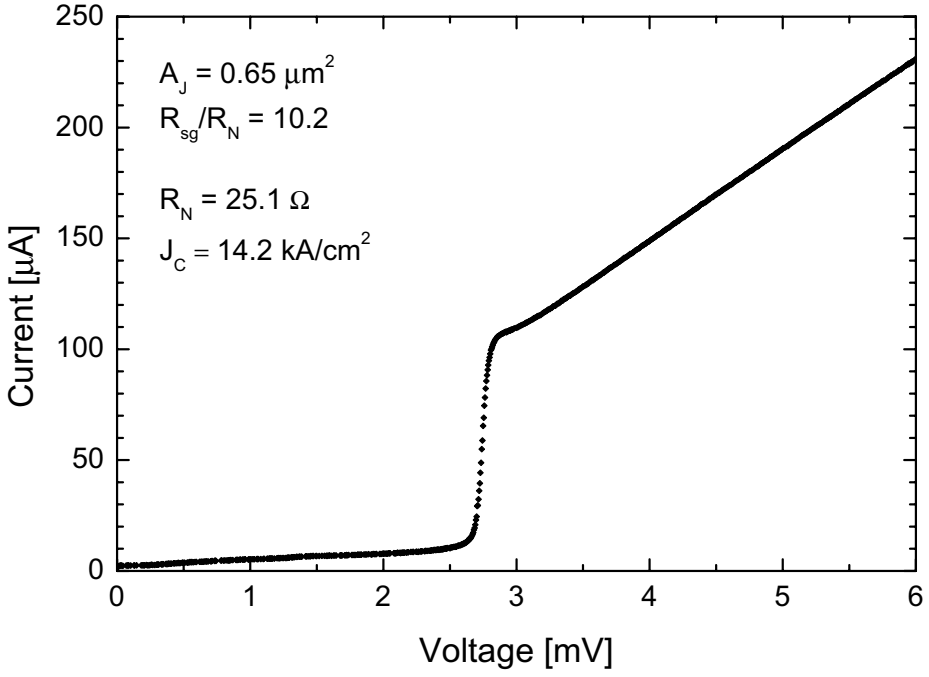


Figure 5.3: DC I-V characteristic of a device from the same wafer as the one presented in Fig. 5.2, now measured in a mixer block of a heterodyne receiver at 4.5 K (device 040401-CMP-ii-D05). The Josephson currents are suppressed by setting a magnetic field to the first minimum of the supercurrent.

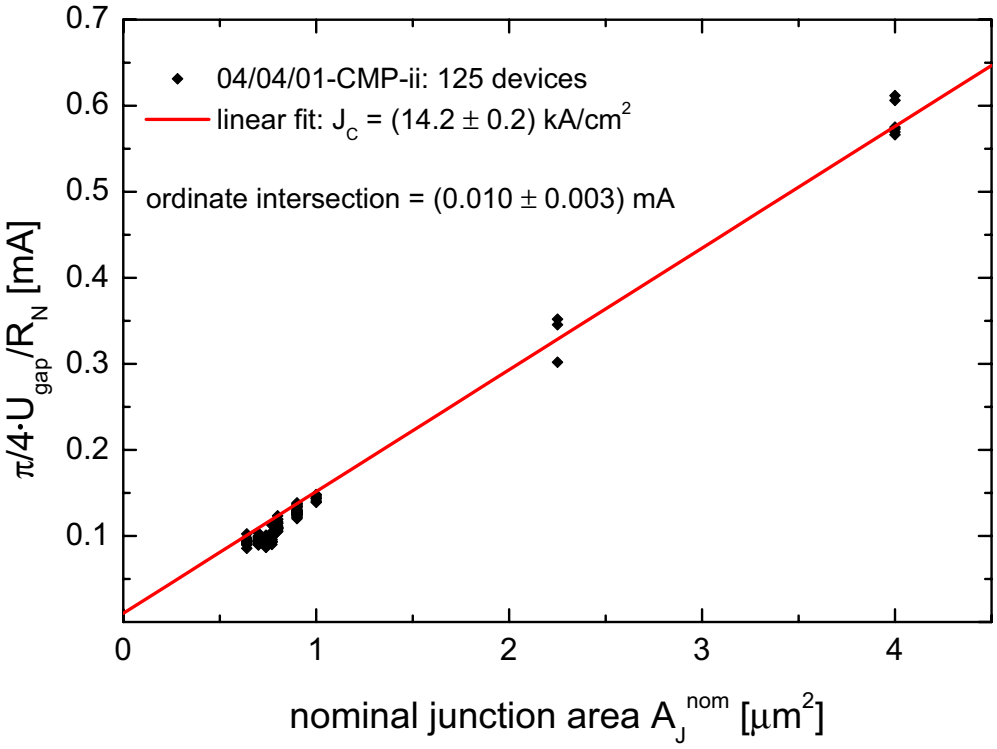


Figure 5.4: J_c determination plot for wafer 04/04/01-CMP-ii. J_c is obtained from the slope of the linear fit.

when the SiO etch mask material was exchanged with harder SiO_2 (as explained in Sec. 3.2.4). The main focus for optimization of e-beam lithography is laid on junction areas above $0.5\,\mu m^2$ because these sizes are presently required for device fabrication.

In the following a junction area reproducibility analysis shall be exemplified for one standard Nb-Al/Al_2O_3-Nb wafer (04/04/01-CMP-ii). This chip has the same trilayer thicknesses as the 490EBL chip and utilizes 50 nm SiO_2 for the junction etch mask.

Fig. 5.2 and Fig. 5.3 show typical I-V curves from two different devices of wafer 04/04/01-CMP-ii, one measured in a LHe dipstick setup and the other in a mixer block, respectively. For both devices the design junction area is $0.64\,\mu m$ and the stated actual areas A_J are calculated from the J_c value and Eq. 5.1. The J_c determination plot for all measured devices (125) of this wafer is given in Fig. 5.4. For both devices the calculated real junction areas lie very close to the design value.

For device B19 (Fig. 5.2) the calculated R_{sg}/R_N ratio of 12.5 is comparable to UV-SNEP devices of similar J_c. The actual subgap current for this device can be assumed even lower because the Josephson current at $V = 0$ has not been completely suppressed during this measurement. R_{sg}/R_N ratios above 10 are typically found for e-beam junctions and therewith are generally comparable to UV-SNEP devices of similar J_c. This seems to indicate that the e-beam exposure does not inflict any damage to the tunnel barrier.

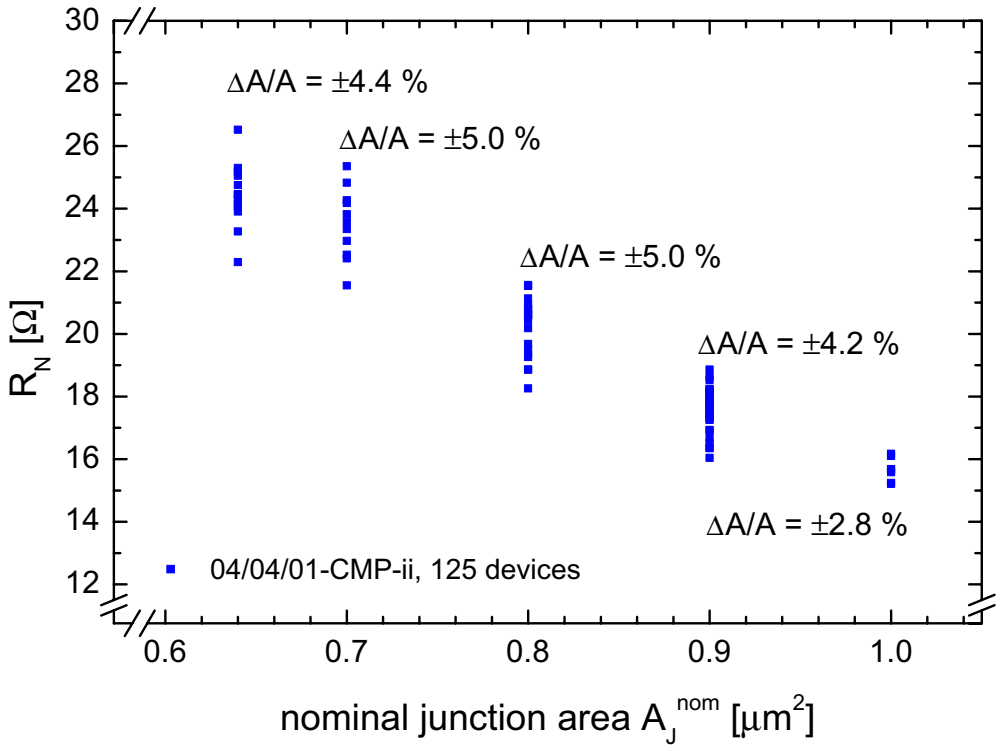


Figure 5.5: Demonstration of the relative junction area reproducibility for 125 standard Nb-Al/Al_2O_3-Nb type devices of wafer 04/04/01-CMP-ii. Junction R_N are plotted against nominal junction areas and the relative area distribution for each area slot is calculated. 50 nm e-beam evaporated SiO_2 was used as an etch mask [59].

The unusually high gap voltage value device B19 exhibits is likewise typical for devices fabricated with the e-beam / CMP fabrication scheme. When compared to standard UV-SNEP defined Nb-Al/Al_2O_3-Nb devices the gap voltage is on average 0.1 mV higher (e. g. see Fig. 2.2). The most probable explanation is thought to lie in a cleaner junction top electrode to wiring interface. In Sec. 5.5.2 this will be commented on in more detail for the embedded trilayer type HIFI devices as these benefit the most from this effect.[7]

The small, positive value of the ordinate intersection in Fig. 5.4 hints at real junction areas that are in average 0.07 μm^2 larger than their nominal A_J^{nom} values. Relating to the 0.64 μm^2 areas of 04/04/01-CMP-ii this small difference corresponds to an averaged systematically longer junction side length of approx. only 40 nm.

Fig. 5.5 visualizes the junction area reproducibility for all devices with $R_{sg}/R_N > 10$ of wafer 04/04/01-CMP-ii. For this purpose the device R_N are plotted against their nominal junction areas A_J^{nom}. With the statistically derived $J_c = (14.2 \pm 0.2)$ kA/cm^2 calculated from the plot in Fig. 5.4, the relative junction area repro-

[7]The seemingly lower gap voltage $V_{gap} = 2.75$ mV for mixer device D05 in Fig. 5.3 is predominantly a result of non perfect heat-sinking to the liquid helium bath of the receiver dewar and consequently the higher operating temperature. The 4.2 K LHe measured dipstick value for this device is a comparable $V_{gap} = 2.89$ mV.

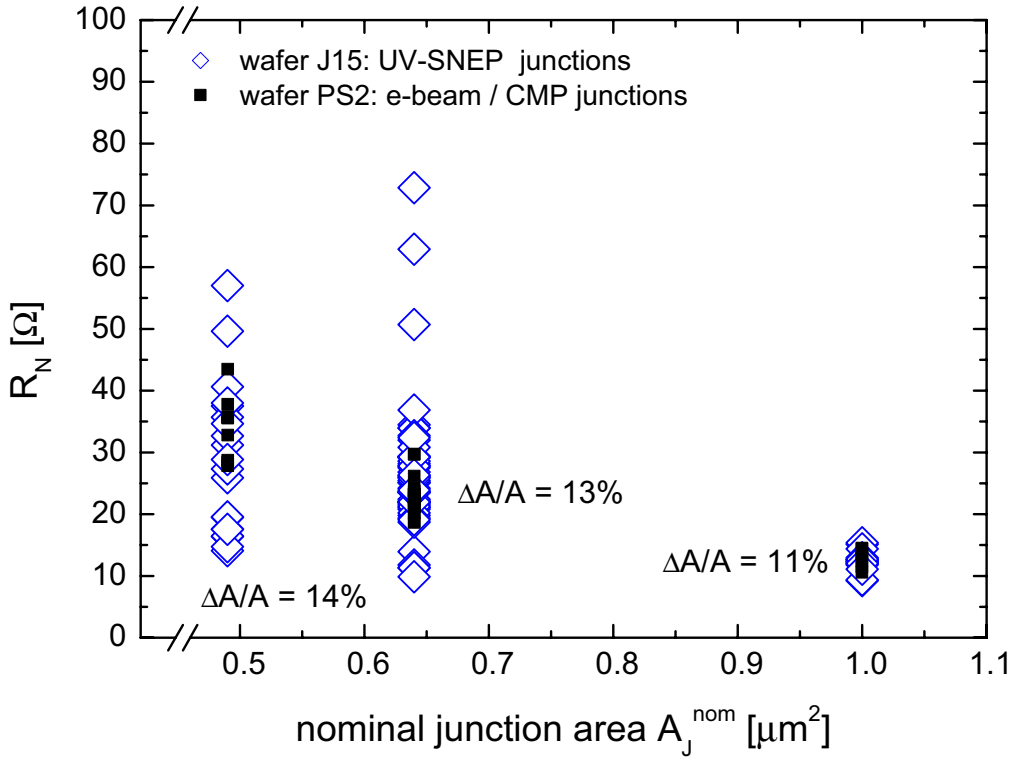


Figure 5.6: Comparison of junction normal resistance R_N spread (analog Fig. 5.5) for an UV photolithographic / SNEP defined wafer (J15) with an e-beam / CMP processed wafer (wafer PS2). Except for junction definition and insulation the fabrication of the embedded trilayer type devices is otherwise identical [59].

ducibility is calculated from the measured R_N spread for the 0.64, 0.7, 0.8, 0.9 and 1.0 μm^2 area slots. It is obvious that the junction areas reproducibility meets the design requirements stated in Sec. 2.3.3 for all investigated junction areas. Compared with a typical UV-SNEP result, such as Fig. 1.6, the dramatic increase in reproducibility and thus accuracy is evident.[8]

The adverse influence of the RIE process on area accuracy becomes evident for the embedded trilayer type devices which require a three-step RIE process in order to isolate the junction from the NbTiN base electrode. In Fig. 5.6 the junction area reproducibility of HIFI Band 2 devices of an e-beam / CMP processed wafer (PS2) are compared to devices of an UV-SNEP defined wafer (J15) with otherwise identical fabrication parameters. Here again the superior definition performance of the e-beam based process for areas below 1 μm^2 is clearly demonstrated [59]. Some data points for the 0.5 μm^2 UV-SNEP areas actually have been omitted for clarity reasons and lie outside of the ordinate scale (i. e. $R_N > 100\,\Omega$, indicating far too small junction areas). When compared to the result for wafer 04/04/01-CMP-ii in Fig. 5.5 ($\Delta A_J/A_J = 13\%$ vs. 4.4% for the 0.64 μm^2 areas), junction area reproducibility on wafer PS2 is inferior, with the probable cause lying in the more complicated RIE.

[8] Please note the different ordinate scales of the plots.

For the embedded trilayer type devices the feature size reproducibility of the e-beam process as well as the possibility to individually adjust junction areas however is taken to advantage in order to compensate for this non-ideal RIE characteristic to a certain degree. Until the RIE process is developed further, the defined areas are simply enlarged by an empirically determined amount in order to yield the nominal area values after RIE. As the analysis of the RF performance of a typical HIFI device will show in Sec. 5.6.2 this leads to a practical workaround procedure. In contrast, this procedure would be far less practical for UV photolithographic junction definition because for each iteration a new photomask is required which is expensive and inflicts additional leadtime. Additionally, relative junction area reproducibility then still would be significantly inferior to the e-beam process and thus clearly challenge this concept.

In summary, junction area reproducibility has gained significantly from e-beam definition. Now the RIE process is the limiting factor for junction area reproducibility and not the lithographic process as was previously the case with UV photolithography. In case standard Nb-Al/Al_2O_3-Nb devices with all-Nb tuning circuits are fabricated, where only a one-step RIE of the niobium top layer is required to cut out the junction top electrode, this leads to a junction area reproducibility which satisfies the $\Delta A/A \leq 5\%$ requirement motivated in Sec. 2.3.3 down to areas of $0.64\,\mu\mathrm{m}^2$. Fabrication of embedded trilayer type devices indicates that a more anisotropic RIE process is required in order to preserve the accuracy of e-beam definition. Until such an enhanced RIE process is available at KOSMA a feasible workaround for correct junction area definition, though, is made possible through the inherent flexibility of the e-beam process.

5.3 E-beam definition of integrated tuning circuit

The combination of e-beam lithography based definition and a lift-off process with a thin photoresist seems a very promising approach for enhanced fabrication of the tuning circuit top electrode. For typical top electrode metalization layer thicknesses of 380 nm (at KOSMA 350 nm Nb and 30 nm Au for most of the devices) a clean lift-off and subsequent accurate definition is readily achievable. The 600 nm thick AZ5206 resist layer leads to a resolution high enough to reproducibly define thin microstrip lines $< 2\,\mu$m. Line widths down to the overlay accuracy and junction diameter determined practical limit of 1.5μm can be defined to an accuracy of $\Delta w_i = 200$ nm. For example, Fig. 5.7 shows the resist definition of a 800 GHz shorted-stub tuning circuit with a minimal line width $w_{min} = 2\,\mu$m.

Furthermore no deterioration of the junction DC I-V characteristics even after multiple exposures on the same device is observed. For example deterioration could be indicated by an increase of subgap currents caused by e-beam charge induced barrier defects. The I-V curves presented in Fig. 5.2, Fig. 5.3 and Fig. 5.13 give an example for devices which have e-beam defined tuning circuits.

Fig. 5.8 shows an 800 GHz device with an end-loaded stub type tuning circuit after lift-off and demonstrates the excellent lift-off characteristics of the process.

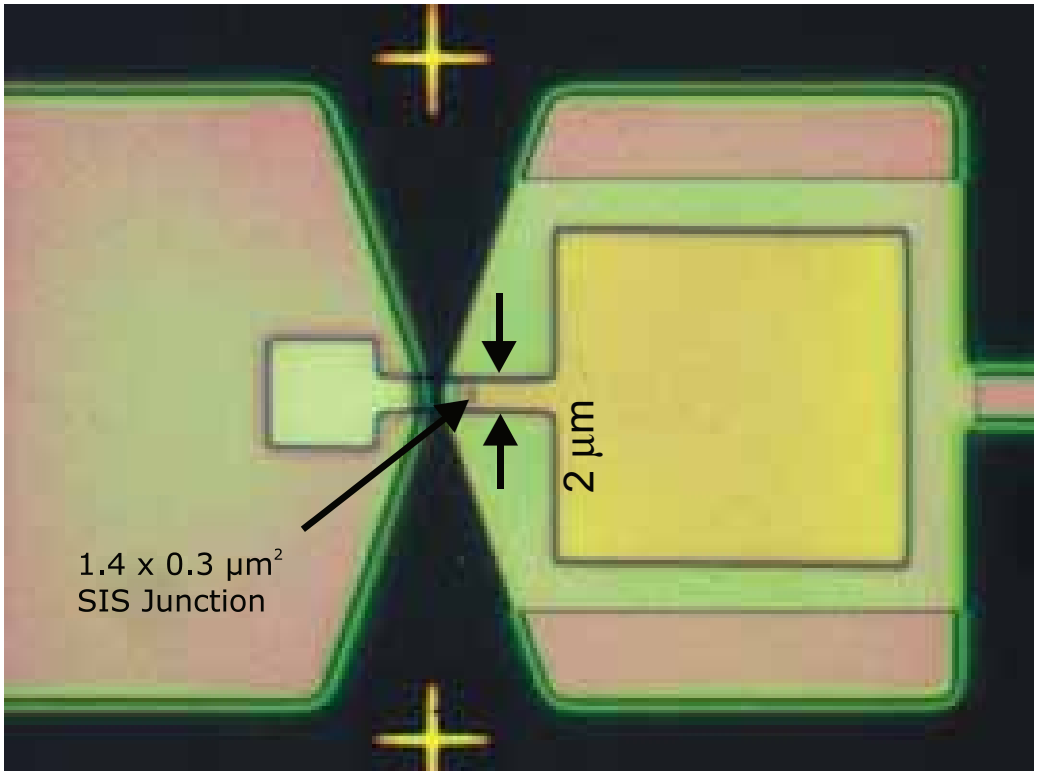


Figure 5.7: Light-microscopic image of the waveguide probe area of an 800 GHz SIS device (500× magnification). A shorted-stub type integrated tuning circuit top electrode has been patterned into the AZ5206 resist layer by e-beam [60].

Additionally, this image shows the effect the mark scan has at each device position. The alignment cross is completely exposed during mark registration which subsequently leads to metalization of the area after deposition and lift-off. Fig. 5.8 illustrates that the scanned alignment cross is positioned at an unfavorable position near the waveguide probes were the additional metalization would affect and disturb the EM field. Consequently, new mask design, e. g. the 490EBL mask (Fig. 3.2), places these crosses at positions outside this probe area with a lateral displacement large enough so that they are diced away during device singularization.

Because only the small scale top tuning circuit top electrode structures can be written by e-beam, the fabrication process must incorporate the complete waveguide feed and RF choke structures in one step, i. e. unlike the 490EBL process. For this reason a large contact pad feature has to be defined on the opposite waveguide feed structure. Luckily, no problems with series resistance were observed in the DC I-V characteristics resulting from dielectric residue left over on this contact area after CMP. Due to its lateral dimensions the contact area itself planarizes just as fast as the junction during CMP so that a cleared junction simultaneously leads to a clean contact area. Thus no additional via opening in the SiO_2 is required prior to top electrode definition.

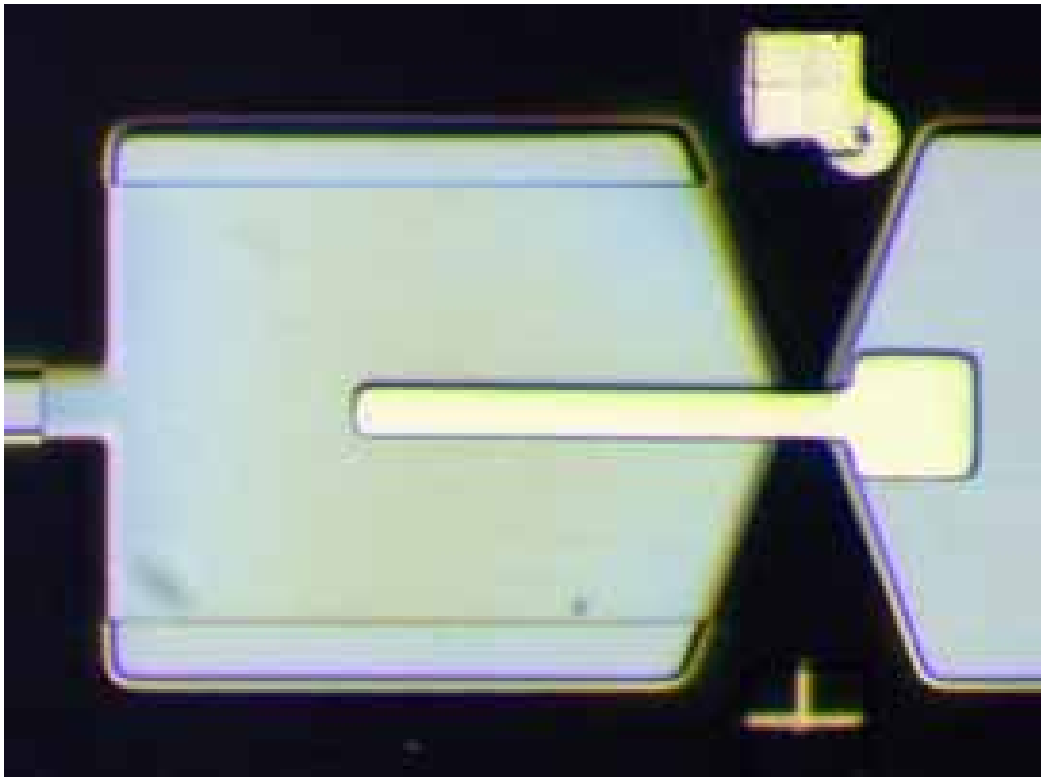


Figure 5.8: Light-microscopic image of the waveguide probe area of a 800 GHz SIS device after lift-off of the end-loaded stub type integrated tuning circuit top electrode metalization (500× magnification). The waveguide probe is 50 μm wide.

5.3.1 Alignment accuracy

In Fig. 5.7 it is evident how precisely the top electrode can be aligned with respect to the junction. In this example the 2 μm wide microstrip line feature is aligned onto the 1.4 μm wide junction (the junction is rectangular) with an accuracy of ≈ 100 nm which is far better than optical lithography can achieve reproducibly. In this case the overlay accuracy actually is below the resolution limit of the image analysis system.

For larger, lower frequency devices (< 800 GHz) achieved overlay accuracies are around 200 nm, because the alignment (and accuracy of the lateral dimensions) of the top electrode is determined by the precision of the scale and rotation calibration routines carried out before lithography. Because the position of the alignment marks is determined by the device, larger devices generally require alignment marks at a greater distance to the writing position and thus calibration errors have a greater effect (see Fig. 3.2). The accuracy of the lateral scale calibration routine is hardware limited by the DA converters used by the lithography system. For the $160 \times 160\,\mu\text{m}^2$ field size used, the achievable accuracy of 0.06% corresponds to a 0.1 μm uncertainty. Furthermore the rotation routine required to de-rotate the field of view is limited to 0.1° resolution which additionally can add an worst-case placement error of 0.3μm. Additionally, distortion effects of the e-beam scanning coils can have noticeable influence on accuracy and further investigation might be

required in order to minimize these for large structures.

For practical application the same alignment mark is used for e-beam definition of the junction area as well as for the tuning circuit top electrode in order to reduce sizing errors of the photomask which defines the alignment marks and the RF metalization features. Whereas any y shift is comparably uncritical for the tuning circuit functionality as long as the microstrip line completely overlaps the junction area, the x shift is critical as it determines the length l_1 of the crucial inductor element of a three-step transformer.

For the time being e-beam definition of the tuning circuit is not implemented into regular junction fabrication although process development clearly demonstrates a significant improvement in overlay accuracy and microstrip line dimensions. The reason for this is found in the very disappointing device RF performance measurements which indicate a problem with this process (see Sec. 5.6.1).

The most probable cause is assumed to be a contamination of the niobium layer of the top electrode of the integrated tuning circuit. It is supposed that this is a result of outgasing of the AZ5206 resist during sputter-deposition and a change of the resist type and / or additional measures such as resist hardening will solve this problem [59].[9] Current low frequency projects such as the 475 GHz SMART devices actually do not require the high resolution of the e-beam process and thus use conventional UV photolithography for the top electrode of the tuning circuit.

[9] AZ5206 resist is not being produced anymore and new process development will focus on using the thicker AZ5214 resist which will then diluted to yield the same layer thickness. AZ5214 is well proven for metalization lift-off processing.

pad	14“ diam. IC-1000-A3P/V/Suba IV PSA II CR
slurry	ILD1200 (diluted to 3%wt. silica, pH = 10.5)
slurry feed	6 ml/min, 90 degrees ahead of wafer
rot. speeds	20 rpm (pad) / 24 rpm (wafer)
rel. velocity	0.37 m/s
down force	26 N (5.1 N/cm^2 back press.)
typ. mean MRR	40 nm/min

Table 5.1: Polishing parameters of the CMP process with BS polisher and monolithic polishing head (Fig. 4.11). All specified consumables are from Rodel. The back pressure is calculated in relation to the quartz wafer area. The mean typical material removal rate (MRR) is measured at a field dielectric position during the final CMP steps, i. e. with nearly planarized surface features.

5.4 CMP planarization

Tab. 5.1 sums up the established main parameter set of the KOSMA planarization process as used during planarization of one exemplary 490EBL wafer (Fig. 5.11) and also for device fabrication of the HIFI Band 2 mixer devices. It is assumed that the given parameters should be applicable to geometrically similar CMP setups. As most CMP development work went into optimization of the mechanical setup as well as determining modifications to circuit layout this will be discussed more thoroughly in the following sections.

5.4.1 Polishing parameters

The driving force for improvement of the mechanical setup was the demand for lower wafer back pressures in order to improve initial planarity results with the prototype setup (Sec. 4.1.2). As experienced during process development with the Logitech polisher any non-stability in the polishing head rotation poses a practical lower limit for the applied wafer load and rotational speed range. The limited drive mechanism of the prototype setup was the crucial factor. All polishing failures which resulted in destruction of the chip (and making the polishing pad unusable) were related to unsteady rotational movement of the polishing head and, subsequently, causing the wafer combination to jump out of the wafer recess.

With the introduction of the IBS polisher and its friction based roller drive mechanism, rotation stability is vastly improved and makes lower wafer back pressures possible without the risk of the wafer combination leaving the recess. In numbers, the back pressure has been be reduced from 10.9 N/cm^2 to the current value of 5.1 N/cm^2 (25 mm diameter wafer) for the monolithic head construction while maintaining enough reserves for process safety and further load reduction in the future (Sec. 6.3). It is observed that less back pressure is additionally beneficial to

the wafer bonding layer as it reduces the friction-induced shear force on the thin film wax and thus lessens the need for the wax curing procedures after each CMP step.

As stated in Tab. 5.1 the rotational speed of the polishing head is set to a 20% higher value than that of the polishing pad in order to further stabilize the setup. Even though this is contradictory to the statement given in Sec. 4.1.2, the small wafer diameters permit such operational parameters with slightly unequal rotational speeds. Planarization results do not show any influence of a such set rotational speed ratio (e. g. Fig. 5.11).

5.4.2 Optimization of pattern density of circuit layout

Introduction of CMP to microfabrication requires some modifications to existing UV-SNEP circuit layout. As explained previously in Sec. 4.1 the polishing pad's mechanical characteristics result to pattern density and feature size dependent material removal which cannot completely be eliminated through careful tuning of the process parameters. With complex finite element based simulations of 2d planarization behavior being far beyond the scope of this work, the pragmatical approach of modifying existing circuit layouts in reaction to the outcome of parallel CMP development was opted. Luckily, only some minor modifications to the circuit layout are necessary when using a KOSMA waveguide devices layout.

Fig. 5.9 pictures the outline of the topography generating metalization features prior to CMP, here exemplified for the 490EBL mask layout. Generally speaking, five feature size categories are found in the SIS waveguide circuit layouts used at KOSMA which are polished / planarized with different MRRs. In descending order these are the global RIE areas for visual end-point detection, column grounding bond pads and lines, and on device level the bond pads, the RF choke / waveguide feed at the junction / tuning dielectric position of each device, and finally the junction (see inset of Fig. 5.9).

CMP process termination is determined by the planarization state at the tuning dielectric position and by confirmation of junction top electrode clearance, i. e. at the smallest feature sizes. The junction feature planarizes very fast due to its submicron size, but the surrounding RF choke end / waveguide feed features influence local pad deformation and thus the local MRR. Best planarization results can thus be achieved by keeping these features similar in size which, though, is difficult to realize for devices designed with largely different input frequency ranges (most of CMP and e-beam development was actually conducted with an old standard UV-SNEP 490/660/800 GHz mask, as e. g. wafer 04/04/01-CMP-ii, Fig. 5.5). 470 GHz range devices are significantly wider than their 800 GHz range counterparts, e. g. 100 μm vs. 50 μm, and planarize systematically slower. During fabrication with mask layouts containing devices of mixed frequency ranges this can lead to the painful decision of favoring one frequency range type while condemning the other useless or to significantly inferior performance due to deviating dielectric thickness.

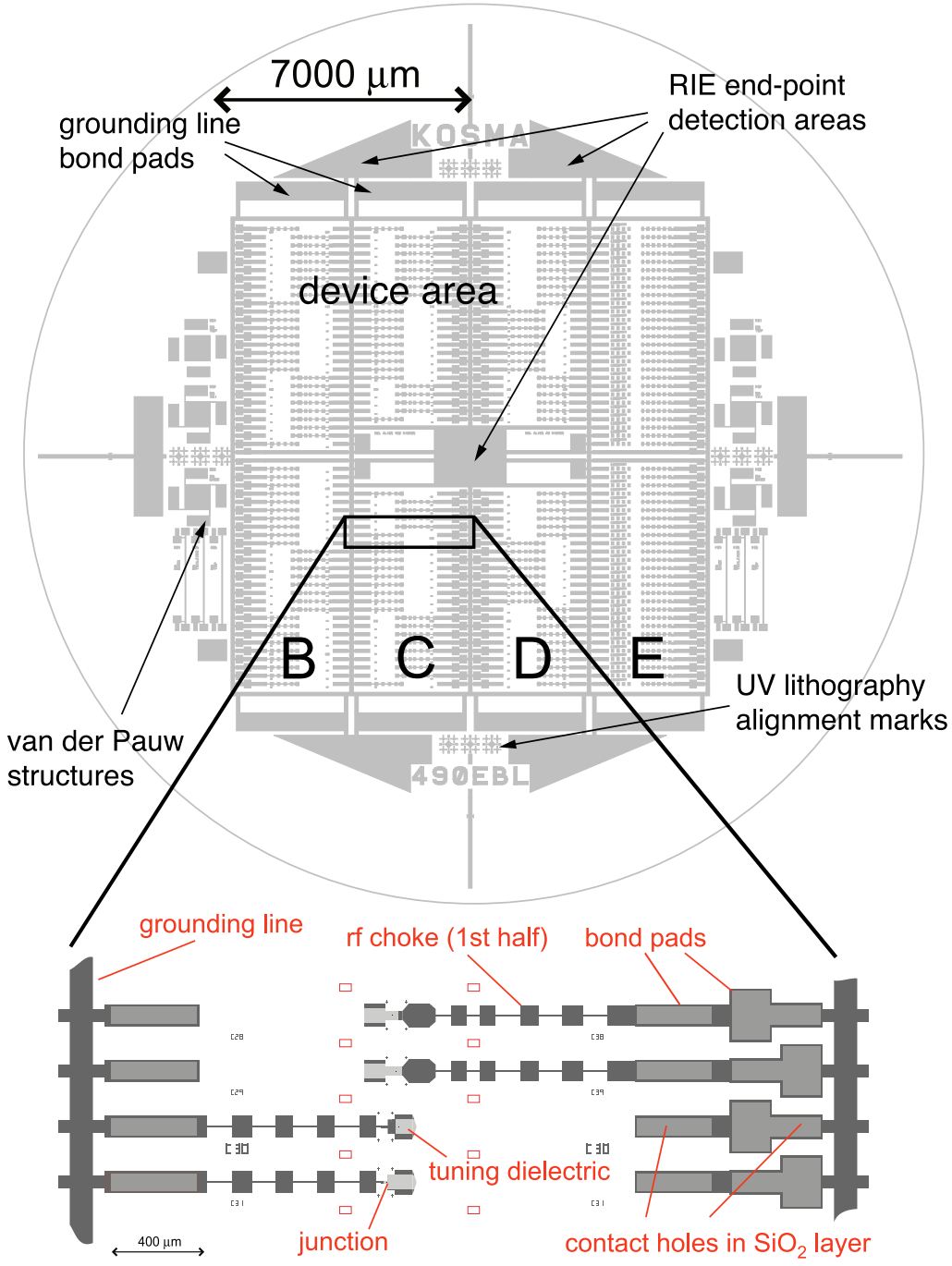


Figure 5.9: Outline of the circuit layout of the 490EBL mask on a 25 mm diameter wafer showing the device features prior to CMP. The area illustrated in Fig. 4.14 is given in an enlarged view and shows device relevant feature categories. The missing second RF choke half and the integrated tuning top electrode are defined after CMP.

Moving outward and to larger structures, the interior of the device columns exhibits an even pattern density from the outset, because bond pads and grounding lines are horizontally displaced by at least 1000 μm, which is significantly larger than any possible pad deformation. For device scale features a distance of 500 μm seems to be sufficient for this CMP process to suppress large feature induced pad deformation. Vertically, the fixed device pitch provides a constant pattern density. For the same reasons, as a minor modification to earlier non-CMP masks, the grounding lines at the columns ends are positioned in the same grid pattern and additionally are kept as narrow as the devices. The large column grounding bond pads have been moved a little more outward than on the earlier masks and know reside at approx. 500 μm distance from the device area. The RIE etch monitor areas are too far out to have any influence on device planarization or, at the center position, actually have no observable influence.

Intrinsic to a CMP process is a wafer diameter independent, approx. 2 mm wide edge zone where the MRR is significantly higher than elsewhere [9]. This could be verified during CMP development and, as a consequence, the diameters of the fused quartz wafer had to be increased from the standard 22 mm to 25 mm. With a device area constricted to a diameter of approx. 20 mm, a 2.5 mm wide edge exclusion zone is sufficient.

5.4.3 Modification to junction fabrication

At device level several modifications to device design and fabrication are made necessary in order to incorporate CMP. The thicknesses of the niobium junction electrode layers have to be adjusted depending on the type of device to be fabricated. In case a standard trilayer type device is fabricated, the top niobium layer thickness must be at least as thick as the requested tuning dielectric thickness. Current device design at KOSMA which incorporates SiO_2 as tuning dielectric typically demands a layer thickness of 200 nm and consequently the top niobium layer must be at least as thick (Sec. 2.3). In practice the top niobium layer is deposited with 230 nm thickness so that CMP can be terminated for a larger number of devices within the process window of $\pm$ 20 nm. For an embedded trilayer device the total trilayer thickness must match the targeted dielectric thickness value. It is obvious that such a device lays higher requirements to junction insulation because the barrier layer lies closer to the dielectric surface (and to the CMP process) than the other device type. HIFI Band 2 devices employ niobium layer thicknesses of 100 nm for the junction base electrode and 130 nm for the junction top electrode [59]. The results presented in Sec. 5.5 will demonstrate that the CMP process still yields very good junction edge insulation for these devices and no disadvantages resulting from the more constraint geometry are observed.

Additional processing is required in order to free the bond pad contact areas from residual dielectric prior to definition of the bond pad reinforcement layer and the second RF choke half / integrated tuning circuit. Earlier mentioned pad deflection and subsequent lower MRR over these large scale features results in 50–100 nm

204 SIS devices	128	KOSMA SMART receiver (475 GHz band)
	54	LERMA HIFI Band 1 backup (480 - 640 GHz)
	22	test devices (J_c, σ_n)
van der Pauw structures	6	square type
	6	thin line type

Table 5.2: Summary of 490EBL mask contents.

SiO_2 left over after CMP termination. Two approaches were successfully evaluated: At first a two-step photolithography and RIE clean with NF_3 was utilized to clean the contact areas, e. g. this was utilized during fabrication of wafer 04/04/01-CMP-ii. In order to simplify processing and, in particular, reduce fabrication steps, the second approach uses photolithography for definition of resist features on top of the contact areas during the same step the dielectric measurement features in-between the devices are defined. The resist is then used as a lift-off mask after dielectric deposition resulting to SiO_2 free contact areas. Fig. 5.9 displays the position of the contact holes at both ends of the waveguide devices (the right end has two bond pad areas where the larger outer bond pad is used for DC I-V characterization and is diced off prior to placement of the device into the mixer block). It is important that the contact holes do not stretch to the edge of the bond pads as otherwise the alkaline slurry will corrode the aluminum barrier base layer which can lead to delayering of the trilayer (a 10 μm margin is sufficient). The established CMP parameters allow selective dielectric material removal and do not affect the accessible niobium top layer.

5.4.4 490EBL mask layout

The 490EBL photolithography mask is the latest circuit layout developed for CMP based device fabrication at KOSMA and reflects the current state of CMP knowhow. As a result this mask has delivered the best planarization results to date (see Fig. 5.11) and will be a basis for future mask designs. The 490EBL layout includes 204 devices (columns B, C, D, E) and additional van der Pauw structures (columns A, F) for the resistivity and T_c determination of the metalization layers (see Fig. 5.9 and Tab. 5.2). SIS devices are organized into 128 devices for the KOSMA 475 GHz SMART mixers (columns B, C, D) and 54 devices as backup for the LERMA 450–640 GHz HIFI Band 1 mixer (column E). As 490EBL provides devices with constant device widths around 90 μm no penalty due to CMP related feature size dependency of planarization rates is observed.

Additionally, 22 test devices are evenly spread across columns B–D. These are used for the J_c calculation process as well as for control measurements of material properties (see Sec. 5.2.1 and Sec. 2.3.2, respectively). With exception of

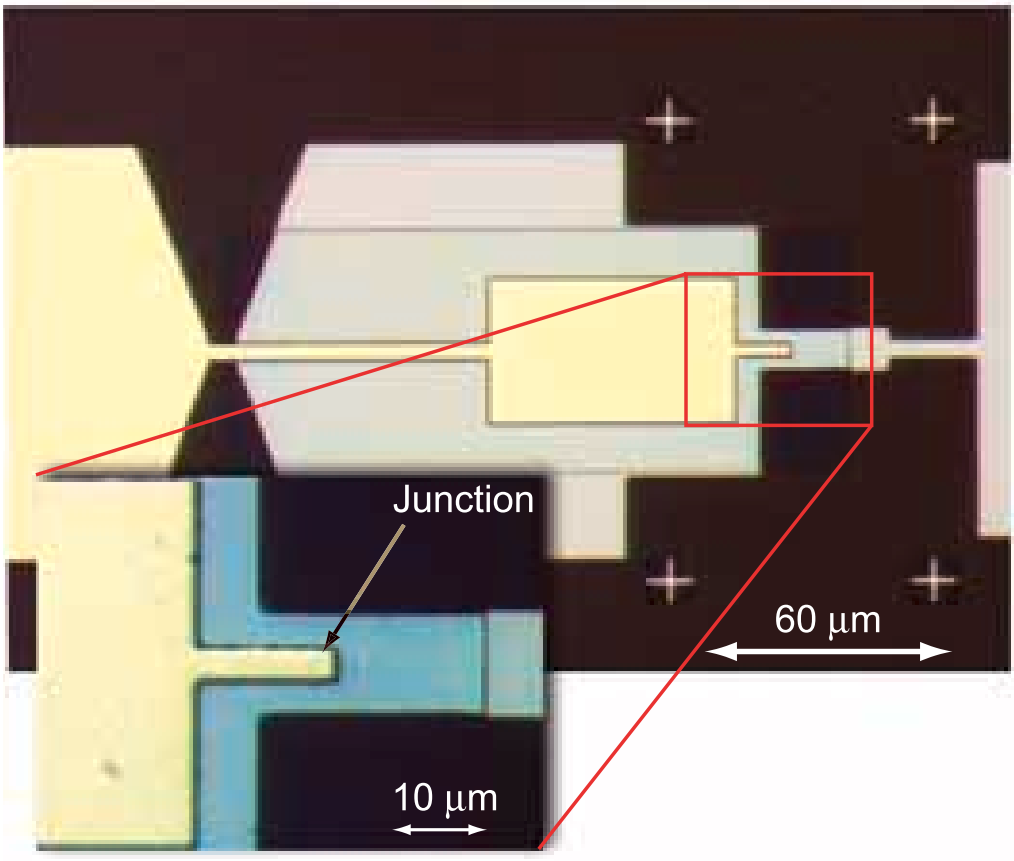


Figure 5.10: Microscopic images of device 490EBL2-D41 after completed fabrication (magnification is 200× for the overview and 1000× for the inset image, respectively). The inset image hints at a smooth junction top electrode to dielectric interface (junction position is indicated, see text).

the test devices all KOSMA devices have 0.64 μm^2 and 0.81 μm^2 areas and are single-junction three-step transformer tuning circuits. The LERMA devices use dual junction tuning circuits which are made necessary due to the very demanding fractional RF bandwidth specifications of 29%. Because of the dual junction tuning circuits larger 1.21 μm^2 junction areas can be used for these.

5.4.5 490EBL planarization quality

Fig. 5.10 images a microscopic view of device D41 of the same wafer after completed fabrication. The interference colors of both images show that local planarization is excellent for the tuning dielectric as no color variation is visible towards the metalization-substrate boundary. The inset image hints at a smooth junction top electrode to dielectric interface typical for CMP devices, because much less topography variations are visible on the tuning circuit top electrode surface than experienced with UV-SNEP fabricated devices.

Fig. 5.11 presents an global planarization result for a 490EBL mask based wafer (490EBL-2). Because 44 individual profilometer measurements of device tuning

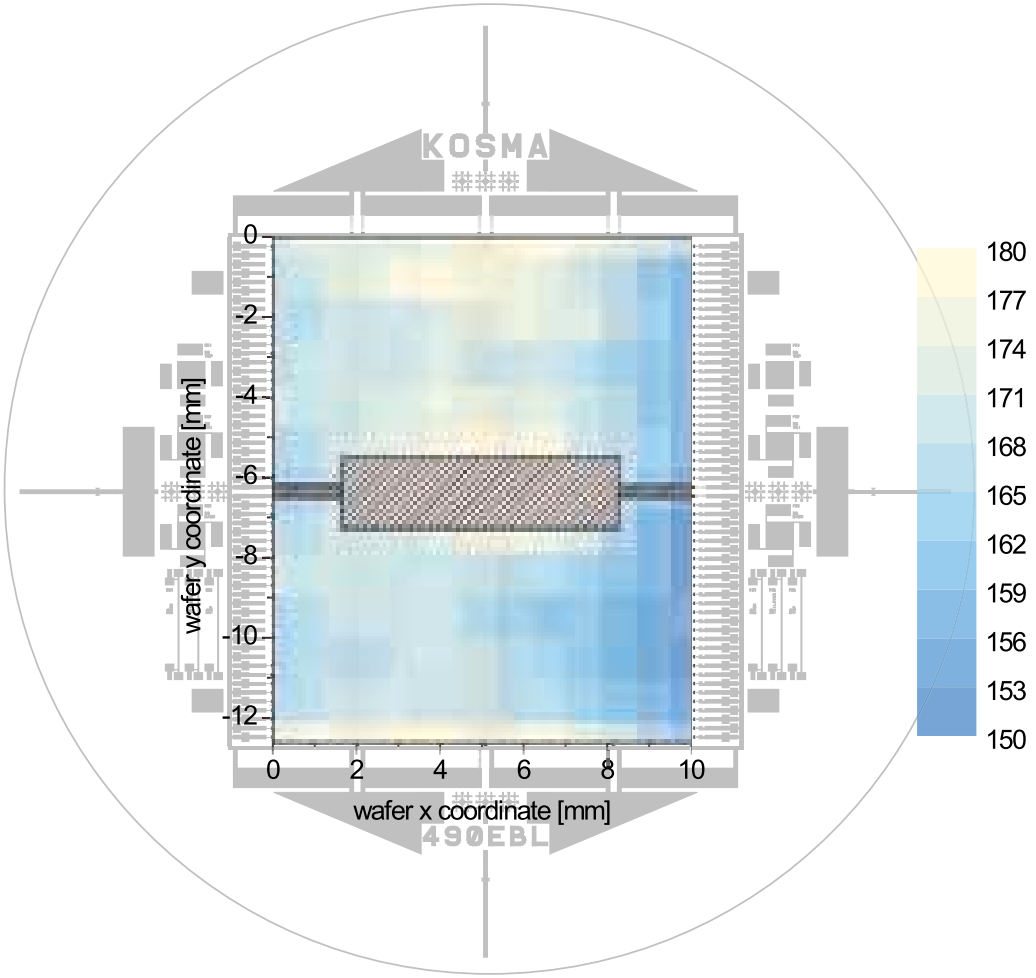


Figure 5.11: CMP planarization result of wafer 490EBL-2 (25 mm diam. fused quartz substrate) superimposed on the circuit layout given in Fig. 5.9. The SiO_2 thickness map (values given in nm) results from extrapolating profilometer measurements of the tuning dielectric for 44 evenly spread, individual devices. The values thus not necessarily correspond to the actual SiO_2 thickness at every point but show the interpolated dielectric thickness for a junction / insulation window type pattern. The hatched, device-free center area has been excluded from the extrapolation. Total polishing time of the 6 executed steps was 10.5 min with standard polishing parameters yielding a mean MRR of 41 nm/min (see Tab. 4.3).

dielectric thicknesses are extrapolated, the map does not represent uniform SiO_2 thickness variations but only the the values at the determinant junction position. The dielectric layer of this wafer has intentionally been over-polished to less than the required 200 nm in order to compensate for a calibration error during trilayer deposition. With the necessitated longer polishing duration in mind the achieved planarity of 165 ± 15 nm (all devices taken into account) can be judged to be an exquisite demonstration of the process capabilities. The planarization result indicates that the distance between the very large column grounding bond pad features and the device area should be enlarged for future mask layouts in order to increase planarization yield even further.

This representative planarization result demonstrates that the CMP process can be developed within a limited R&D type environment to enough maturity for integration into regular (e-beam lithography based) SIS device fabrication.

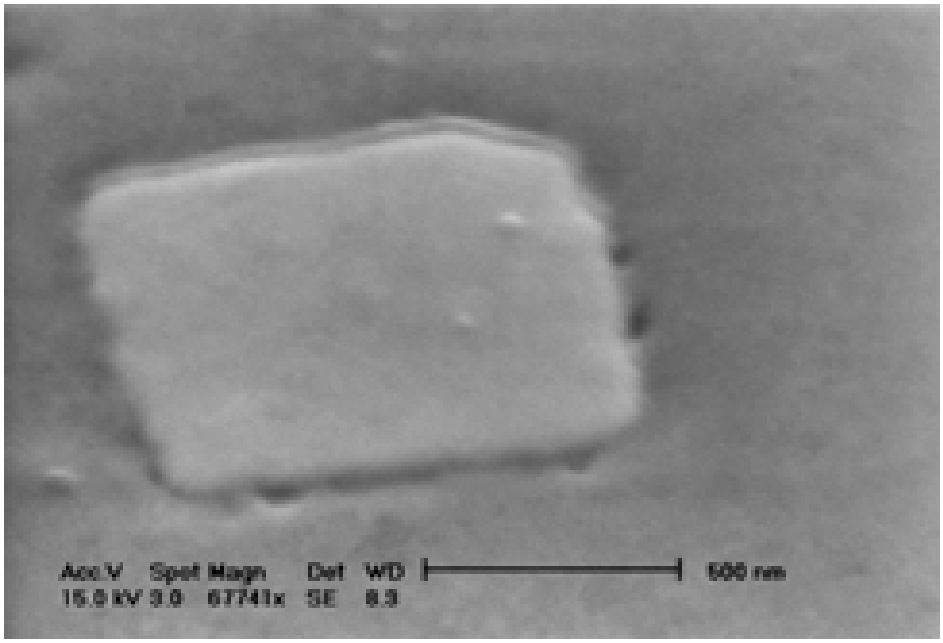


Figure 5.12: SEM micrograph of an 1.0 μm^2 area junction taken at 67k$\times$ magnification (tilted view). The micrograph shows the junction top electrode and the surrounding dielectric layer after completion of the CMP process. The surface was prepared with 10 nm sputter-deposited gold. The scale bar measures 500 nm. [SEM micrograph taken at 2. Physikalisches Institut, Universität zu Köln with kind assistance from Thomas Kemen.]

5.5 Improvement of DC I-V characteristics

The DC I-V characteristics of a SIS junction are a powerful tool in order to characterize the quality of fabrication. Besides the mainly definition related parameters junction normal resistance R_N (> 6 mV) and the voltage position of the self-induced resonances the Josephson currents have with the integrated tuning circuit (see Sec. 5.5.2), high quality devices should exhibit a large junction subgap R_{sg} (2 mV) to R_N ratio ≥ 10 (i. e. a low subgap leakage current), a high gap voltage V_{gap} and a sharp quasiparticle current onset. All of these values can be relatively easy determined in a liquid helium dipstick setup at 4.2 K.

During initial process development any negative influence of the CMP step on the DC I-V characteristics was closely investigated with standard niobium UV photolithography defined junctions. This approach was chosen because these devices are much faster to fabricate and therefor enable faster process development. The evaluation focused on the possibility of generating micro-shorts in the junction circumference during CMP and thus leading to inferior DC I-V characteristics.

In accordance with literature sources no such deteriorating effects are observed and devices with equally high quality I-V DC characteristics are fabricated [58]. Fig. 5.12 shows a SEM micrograph of a junction top after completion of CMP. Two properties catch the viewer's eye which can be interpreted as causative for the positive DC I-V results: First, it is visible that the interface between junction

Figure 5.13: Photograph of a DC I-V characteristic of a deep submicron area junction 11/25/98-C11 demonstrating the excellent device quality the process is capable off. The junction area, calculated with Eq. 5.1 and $J_c = 18\,\mathrm{kA/cm^2}$, $V_{gap} \approx 2.8\,\mathrm{mV}$ and $R_N = 121\,\Omega$, is only $0.1\,\mu\mathrm{m}^2$. 80 nm e-beam evaporated SiO_2 were used as etch mask. In addition to junction definition, e-beam lithography was used for the tuning top electrode as well. Measured at 4.2 K in a dipstick setup. Scales are 0.5 mV/div. and 5 μA/div., respectively.

and the insulating dielectric seems cohesive and thus hints at potentially good electrical insulation characteristics even for very small junction areas (where the importance of junction circumference gains in importance). Second, the clean top electrode surface is noticeable, indicating favorable film growth conditions for subsequent tuning top electrode layer deposition on a clean interface.

In the following sections some representative results will be given which document the polishing process related beneficial influence on device DC I-V curve quality. The CMP process not only enables e-beam lithography for reproducible submicron area junction definition but generally also improves the device's DC I-V characteristics in particular for smaller, submicron junction areas when compared to SNEP fabricated devices.

5.5.1 Leakage currents

After integration of e-beam lithography and CMP into junction fabrication, initial processing runs were dedicated to investigate the limits of the PARTS based process. For this purpose devices with junction areas down to $0.1\,\mu\mathrm{m}^2$ were fabricated and their DC I-V curve subgap leakage currents characterized. In summary, these very small junction areas can be fabricated with similar high quality, R_{sg}/R_N ratios as for micron area sized UV-SNEP devices. Fig. 5.13 shows an example DC

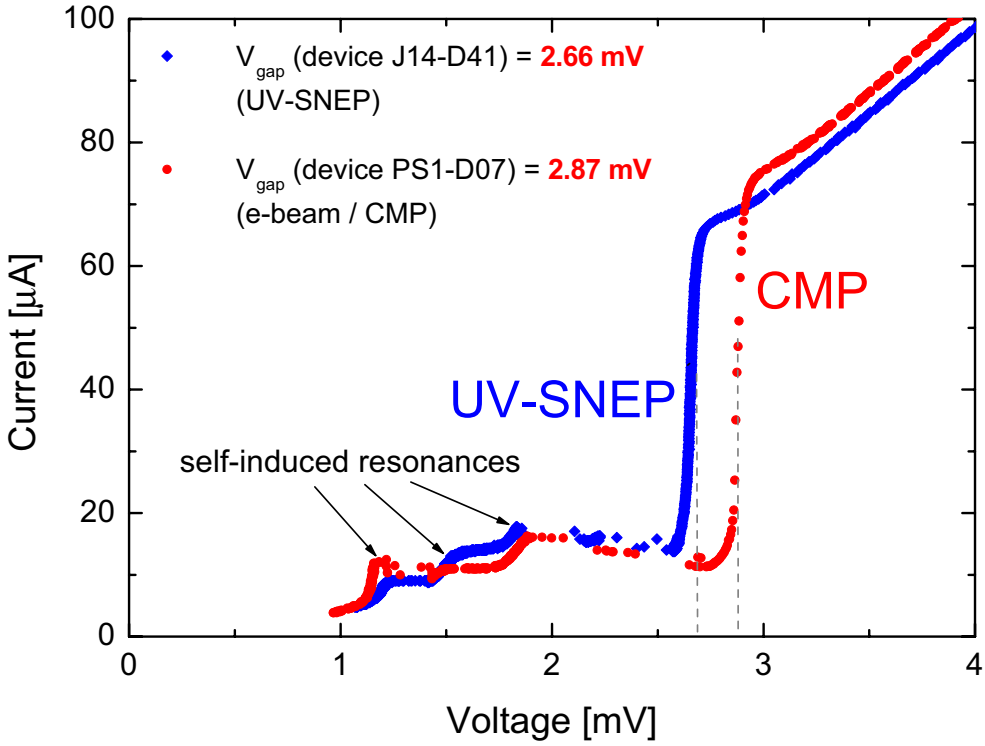


Figure 5.14: Comparison of typical DC I-V characteristics of two embedded trilayer type devices for HIFI Band 2 mixer development, measured at 4.2 K in a dipstick setup. Device D41 (wafer J14) is UV-SNEP defined and exhibits a characteristic, systematical lower gap voltage than device D07 (wafer PS1) fabricated with the e-beam / CMP process but otherwise identical fabrication parameters [59].

I-V characteristic of a junction with a calculated area of only 0.1 μm^2 and an excellent $R_{sg}/R_N = 18$. This clearly demonstrates the potential of this non lift-off based junction definition scheme. The fact that anodic oxidation of the junction sidewall (for passivation) does not have any noticeable effect on the R_{sg}/R_N ratios further emphasizes the good insulation characteristics of the CMP process.

5.5.2 Gap voltage

A very important beneficial aspect of the planarization process is particularly well seen with the HIFI Band 2 embedded trilayer devices which have NbTiN as tuning circuit base electrode material. The tunnel barriers of these devices rely on cooling through the niobium or aluminum tuning circuit top electrode material as the NbTiN / Nb interface below the junction hinders heat transport (see Sec. 2.1.1). Early UV-SNEP defined HIFI Band 2 devices suffer from low gap voltages, presumably caused by photoresist residue on the junction top electrode left over after lift-off of the dielectric [26]. E-beam / CMP fabricated devices demonstrate systematically higher gap voltages than these foregoing UV-SNEP fabricated devices. In Fig. 5.14 two typical DC I-V curves of junctions from both fabrication schemes

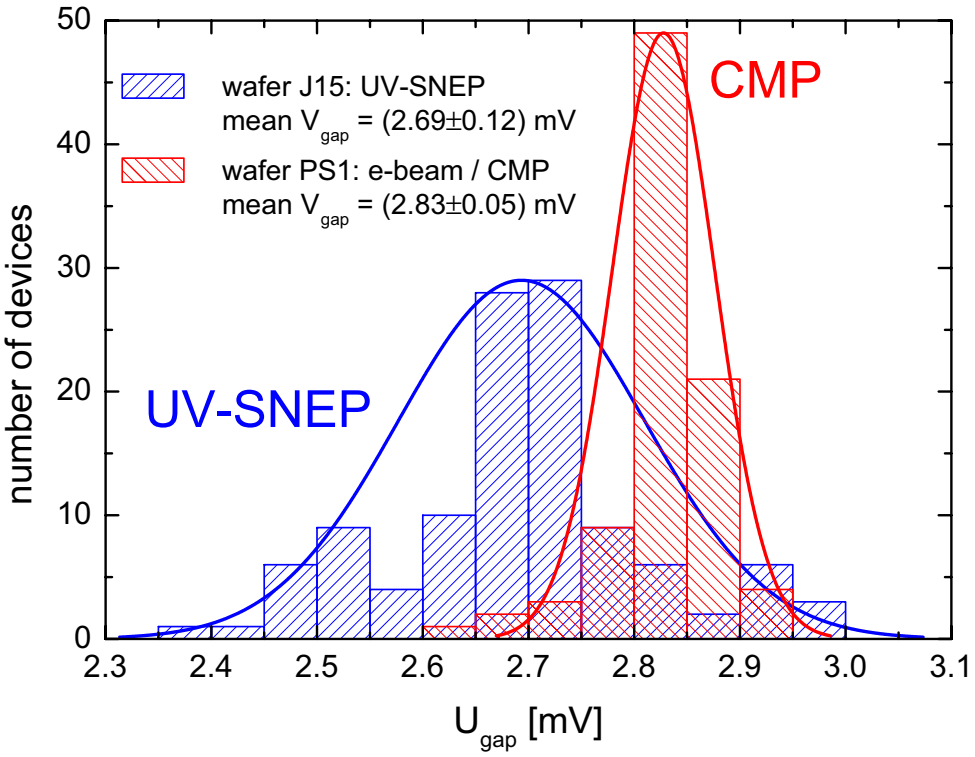


Figure 5.15: Comparison of the device gap voltage distribution for UV-SNEP fabricated wafer J15 with e-beam / CMP fabricated wafer PS1. The gap voltage errors are derived from the standard deviation of the gauss fits [59].

but otherwise identical fabrication parameters (e.g. layer stack, $R_N \cdot A$ product and junction area) are compared. In this example the e-beam / CMP processed device exhibits a gap voltage increase by over 0.2 mV. In agreement with the qualitative interpretation of Fig. 5.13 this hints at a significantly cleaner interface at the top of the junction electrode which has a greater effect for this type of device.

Fig. 5.14 contains one additional (non-CMP related) information which is used for device selection for mixer application: As the Josephson effect is not suppressed by a magnetic field self-induced resonances of the Josephson oscillations with the integrated tuning circuit are observed [48]. For the typical three-step transformer and waveguide feed / environment of a KOSMA SIS mixer these LC resonances have proven to be a precise indicator of the band center position of the tuning circuit when using the fundamental Josephson relation 1 mV $\hat{=}$ 483.6 GHz. Hence this is used for device pre-selection prior to RF measurements. Due to the hysteresis of the SIS DC I-V characteristic and the measurement electronics used, these current steps cover up the true subgap leakage currents [59].

The positive effect of CMP on the junction top electrode interface is also underlined by the fact that the gap voltage spread of CMP devices is significantly narrower than of UV-SNEP fabricated devices. Fig. 5.15 compares the gap voltage distribution of all devices from the UV-SNEP wafer J15 with the e-beam / CMP wafer PS1. As in Fig. 5.14 all devices are of the embedded trilayer type, i. e. for HIFI Band 2 mixer development, and are otherwise identically fabricated.

share of junctions with $R_{sg}/R_N > 10$	share of junctions with $R_{sg}/R_N > 15$	$\Delta A/A$ for $0.2\ \mu m^2 < A < 0.6\ \mu m^2$
84 %	38 %	±7 %
	80 junctions meas.	20 junctions meas.

Table 5.3: Total device yield in respect to R_{sg}/R_N of standard trilayer type wafer 01/19/99-CMP with critical current density $J_c = 9$ kA/cm^2. Junctions areas ranging from 25 μm^2 down to 0.6 μm^2 are taken into account. The achieved area reproducibility for the smallest areas is given additionally [60].

In addition to the systematically increased gap voltage the e-beam / CMP devices exhibit a noticeably narrower distribution of their gap voltage values. This, too, is best explained by a significantly cleaner junction to tuning top electrode interface with increased and more reproducible barrier cooling than can be generally achieved by a UV-SNEP process [59]. It must be concluded that the CMP process has the beneficial influence of removing photoresist residue which is inherent to SNEP fabricated devices.

5.5.3 Device yield

The CMP prototyping phase demonstrated that the number of device defects due to polishing induced scratching is very low. The dual use of the Logitech lapping machine for CMP as well as wafer backlapping with potentially yield-threatening alumina powders in a non-cleanroom environment surprisingly didn't prove to be a big problem during this phase. Typically only a few scratches were found on a chip and, because the critical device area, i. e. the insulation windows / tuning dielectric, is comparably small, devices hardly ever became defective. It was observed that most particles are a result of chipping at rough places on the edge of the fused quartz wafer and mostly are not a result of polishing pad acquired contamination [58].

Since moving the CMP process into the cleanroom and to the dedicated IBS polisher scratching due to acquired particles now is virtually non-existent and CMP leadtime due to the cleaning procedures could be significantly reduced. Additionally, the fused quartz wafer now used are specified to have polished edges and a slightly trapezoid cross-section (circuit side has smaller diameter). As a result chipping at the wafer edge and thus scratching now is essentially non-existent during CMP and has no influence on total device yield. Tab. 5.3 gives a yield analysis for a typical wafer with standard trilayer type devices and e-beam definition of both junction areas and tuning circuit for the prototype setup. Criterion for device selection here simply is a high quality DC I-V characteristic expressed by a

R_{sg}/R_N ratio greater than 10 without taking deviations from the targeted dielectric thickness into account [60].

At present development state the global uniformity of the CMP process still has the biggest affect on total device yield. Typically, a radial dependency of the resulting dielectric thickness is observed across the wafer after CMP. In practice a compromise for the CMP termination point must be found which partially leads to devices with affected tuning circuit performance due to an anomalous dielectric thickness. In worst case, i. e. for the extreme device positions in relation to the dielectric layer thickness distribution, either non-contactable junction top electrodes or short-circuited junction barriers are a result. The exact cause for the radial dependency is unclear and needs further investigation, especially because the resultant distribution characteristics are not reproducible and vary from wafer to wafer. In particular a more thorough examination of the influence of the slurry rate and flow dynamics underneath the wafer, which could be varied by modifying the wafer carrier's retaining ring geometry and / or the wafer back pressure, seems important. Also the effect the conditioning procedures have on the pad surface and the planarization result are not well understood and further analysis might lead to overall improved planarization uniformity and process reproducibility.

As predicted the local planarization behavior of the CMP process on a device scale is noticeably beneficial to device yield especially for the embedded trilayer type devices. Edge coverage problems of the wiring layer across the waveguide feed structures, where UV-SNEP definition commonly results to devices with open circuit DC I-V curves or weak link type defects at bias voltages above V_{gap}, now are virtually non-existent for the HIFI Band 2 devices which require 350 nm NbTiN as ground layer. It could additionally be demonstrated that UV-SNEP processed devices with normal conducting aluminum tuning circuits show a significantly increased device yield to 90% (DC criteria as used in Tab. 5.3, first column) after introduction of a short CMP clean-up process after lift-off of the dielectric [26]. For the same reason device yield for HIFI Band 2 mixer wafers also has improved after introduction of the e-beam / CMP process with the junction defining RIE process now being the biggest contributor to yield loss. For example, UV-SNEP defined wafer J15 (Fig. 5.15) shows a typical device yield of 55% for junction areas in the 0.64–1.0 μm^2 range while e-beam / CMP processed wafer PS8 exhibits an increase to 90% (DC criteria with a reduced $R_{sg}/R_N > 5$ due to leakier device nature).

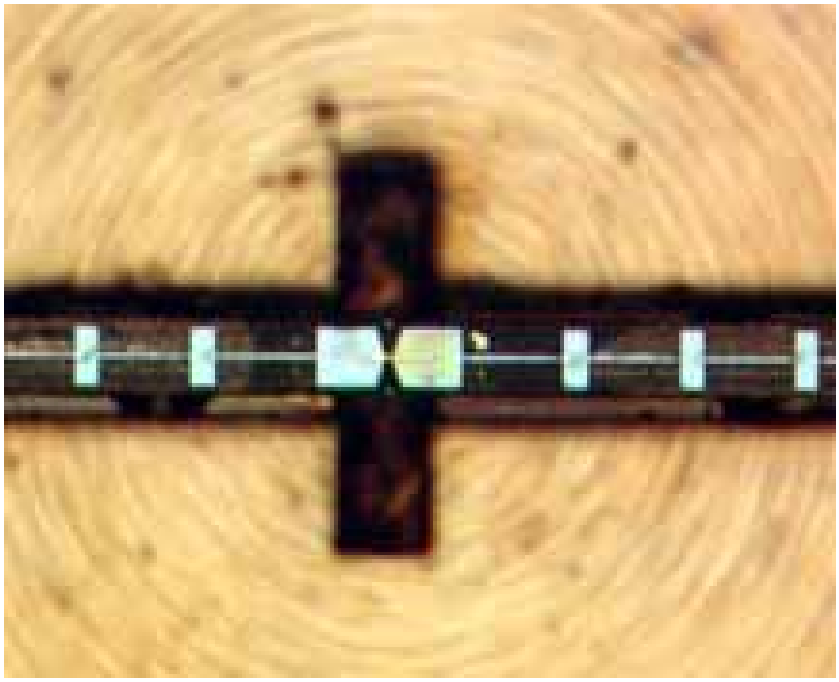


Figure 5.16: Microscopic photograph of an 800 GHz band e-beam / CMP device glued into a KOSMA waveguide mixer block (end-loaded stub type tuning circuit). The bow-tie antenna of the device is positioned centrally in the waveguide (dimensions $90\times350\,\mu m^2$) with 60 μm distance from the backshort.

5.6 Mixer RF evaluation

Preselected by their DC I-V characteristics, promising waveguide mixer devices are backside lapped (e. g. to 30 μm for quartz substrates at 800 GHz) and singularized by means of a dicing saw. The device is placed and glued into the mixer block, i. e. the waveguide environment, and electrically contacted through ultrasonic bonding (Fig. 5.16). The mixer block is connected to the feed horn and placed into a LHe cryostat for mixer operation and analysis of the heterodyne RF characteristics of the receiver setup. Most importantly the RF performance analysis of the receiver must yield the mixer noise temperature $T_m(\nu)$ and gain $G_m(\nu)$ which are needed for calculation and comparison of the mixers sensitivity.

In Fig. 5.17 a standard heterodyne receiver measurement setup is schematically presented. The mixer block assembly, the HEMT[10] amplifier, which is the first low-noise amplifier of the IF chain, and the bias-tee, which is needed to feed the bias voltage to the junction, are connected to the cryostat's cold-plate. The signal is combined with the local oscillator signal outside of the dewar window with the help of a beam-splitter. Typically, only 5% of the local oscillator power is coupled into the dewar whereas 95% of the signal power is passed through into the dewar.

The Y-factor method is used for determining the overall receiver noise temperature T_{rec}. Two noise sources which emit defined and unequal power levels are

[10] High Electron Mobility Transistor

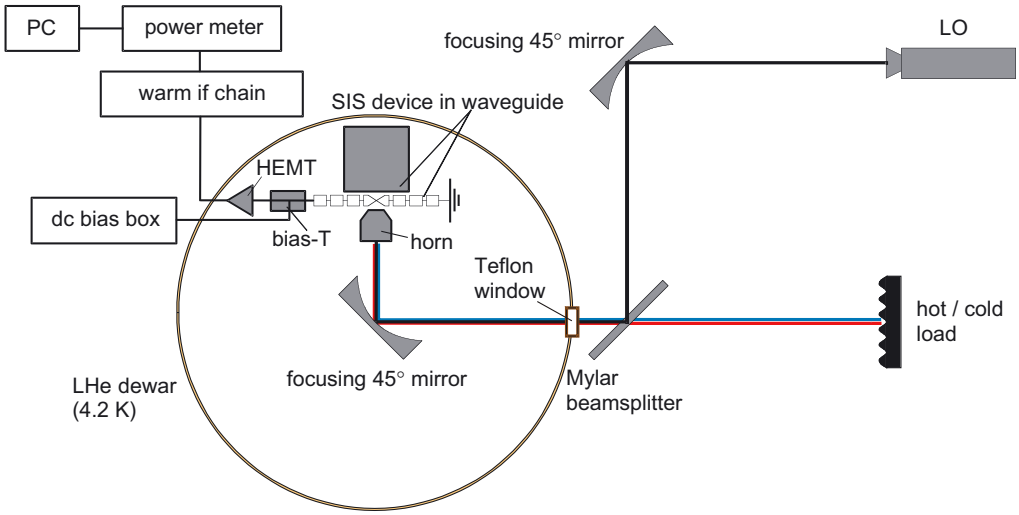


Figure 5.17: Schematic illustration of a heterodyne measurement setup for mixer characterization. The local oscillator (LO) is a Gunn diode with frequency doubler and tripler stage. Its power is combined with the hot / cold load signal at the mylar beam-splitter and focused into the dewar. The hot / cold load is microwave absorber material at room (295 K) or LN_2 (77 K) temperature. Illustration adapted from [72].

required. In practice, microwave absorbers at room (T_{hot}) and LN_2 (T_{cold}) temperatures are used. The receiver or system noise temperature then calculates from the ratio of the measured power values $Y = P_{hot}/P_{cold}$ under the Rayleigh-Jeans approximation to:[11]

$$T_{rec} = \frac{T_{hot} - Y \cdot T_{cold}}{Y - 1} \,. \tag{5.3}$$

For frequencies below 500 GHz this approximation is precise enough. For more accurate results at higher frequencies the Callen-Welton equation, which also includes zero point fluctuations, should be used [41].

From the measured T_{rec} and G_{rec} the T_m and G_m values then can be calculated with equation Eq. 1.1 when the contributions of all components in the signal path of the heterodyne receiver setup, e. g. optics losses and T_{if}, have been precisely calibrated. A thorough description of the KOSMA receiver setup with a complete characterization of the components, i. e. a noise breakdown, can be found in [26].

5.6.1 Comparison of device performance

A fair number of devices with e-beam definition of the junction and the integrated tuning circuit top electrode were measured at frequencies between 640 and 690 GHz as well as between 780 and 820 GHz. Mixer performance results of

[11] In the Rayleigh-Jeans approximation the radiation power is related to its physical temperature as $k_B T$ in one polarization.

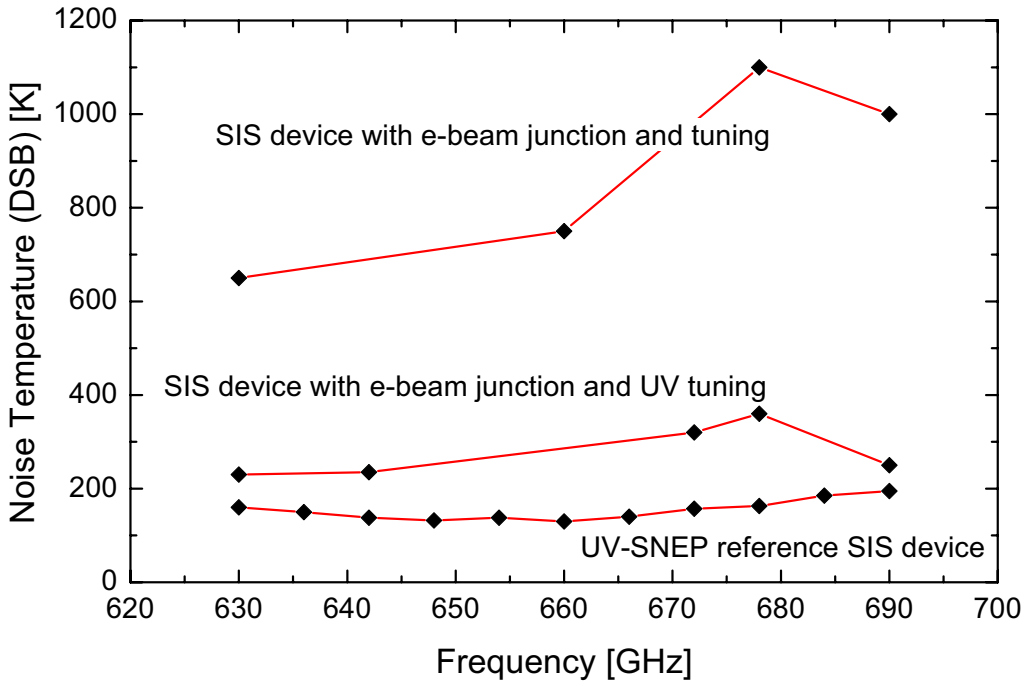


Figure 5.18: Comparison of uncorrected receiver noise temperatures of two typical e-beam processed devices with a UV-SNEP defined reference device (bottom line, from [27]). The top line shows a result from an standard Nb-Al/Al_2O_3-Nb type device with e-beam definition of the junction as well as the tuning structure. The middle line is shows the receiver performance of an device with e-beam definition only for the junction (wafer PS1, device D07).

these devices, though, all disappointed despite the superior definition accuracies and device I-V characteristics as compared to UV-SNEP devices.

Fig. 5.18 compares the typical uncorrected receiver noise temperatures in the 660 GHz range for such a device (top line) with an UV-SNEP reference mixer (bottom line) and a device with e-beam junction definition but UV photolithography for the tuning circuit (middle line). Noise temperatures are calculated with Eq. 5.3 and, as in principle the same optics setup and IF chain were used for the measurements [25, 32], the receiver noise temperatures allow a direct comparison of mixer performance. It is evident that the receiver noise temperatures for the device with e-beam junction and tuning circuit definition are 3–5$\times$ too high whereas the performance of the middle line device is more or less comparable to the UV-SNEP device. The somewhat higher noise temperatures of the middle line device can be explained by the extremely wideband design of this HIFI Band 2 mixer device (640–800 GHz) which inevitably forces a trade-off with maximum sensitivity.

Consequently one must come to the conclusion that the e-beam fabrication process of the integrated tuning circuit top electrode deteriorates device RF performance. As presented in Sec. 5.3 no noticeable effect on these device's DC I-V characteristics is observed during dipstick characterization. Closer examination of device performance and behavior during mixer evaluation ultimately points to a proba-

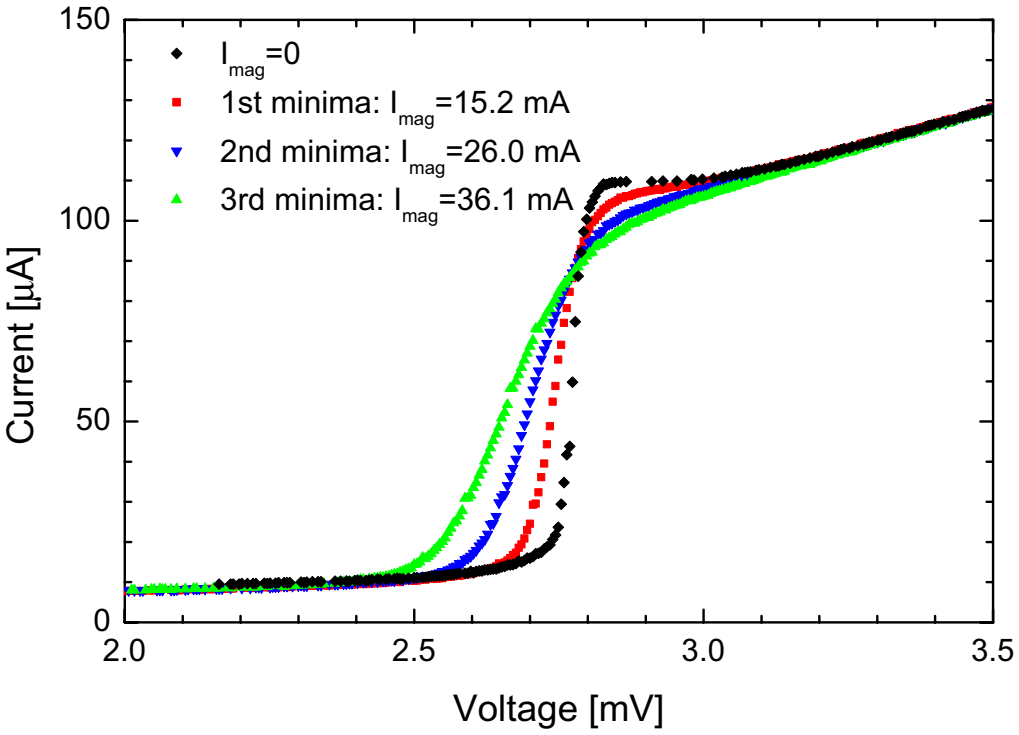


Figure 5.19: A close-up view of DC I-V curves of device 040401-CMP-ii-D05 shows the unusually large dependency of V_{gap} in respect to varying magnetic field strength, here expressed by the coil current I_{mag}. The magnetic field is adjusted to the denoted minima of the Josephson current.

ble degradation of the superconducting properties of the niobium top electrode material. Following points summarize the evidence underlining this assumption:

1. Devices with e-beam defined tuning circuit top electrode show a unusually large depression of the gap voltage when a magnetic field is applied during mixer operation for suppression of the Josephson effects. Fig. 5.19 shows a close-up view of such a device's DC I-V characteristics for different magnetic field strengths. The DC I-V curve for three different coil currents and the zero field stage are plotted in this figure. The currents have been set to yield the denoted order of minima of the critical current corresponding to stable receiver operation. Generally, the magnetic field has a stronger affect on the superconducting state of a superconductor of deteriorated quality and for these devices it is assumed that the inferior properties of the tuning circuit top electrode material can reach down into the junction top electrode. This on the other hand then should affect the superconductor energy gap value, and the resulting DC I-V characteristic of such a device consequently must exhibit a larger than typical decrease of the directly measurable gap voltage value for increasing magnetic fields.

2. The measured noise temperatures show a steeper dependency on the magnetic field strength, here likewise expressed by the (absolute) coil current, than usual for higher operating frequencies (Fig. 5.20). In this plot the num-

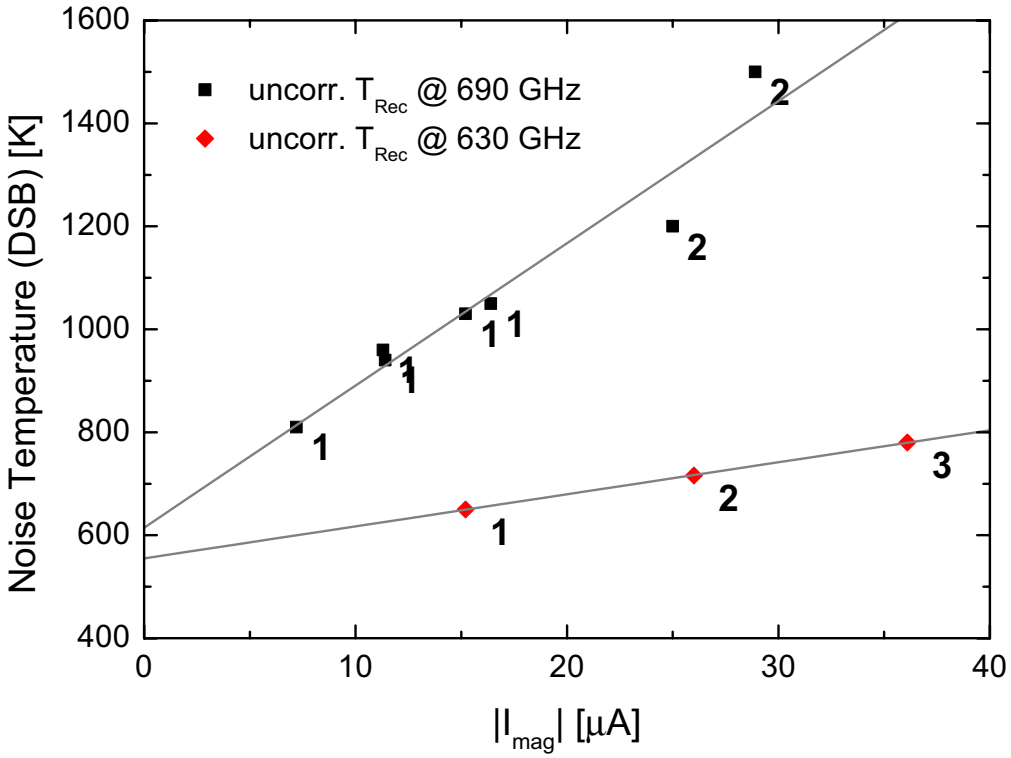


Figure 5.20: Uncorrected receiver noise temperatures (DSB) of device 040401-CMP-ii-D05 vs. absolute coil current of the superconducting magnets. The numbers denote the order of minima of the Josephson current. The corresponding (unpumped) DC I-V curves for the three lower data points are given in Fig. 5.19.

bers denote the order of minima of the critical current used during operation as in Fig. 5.19. The steeper slope of the linear fit of the data for the higher operating frequency affirms the assumption of a decreased energy gap superconductor and a consequently lowered onset of RF losses. This cannot be taken as a proof though, because the functionality of the tuning circuit, i. e. the frequency dependent power coupling, is embedded within this result. (As some currents had reversed polarity, a shift in the minima to current relation is observed because of the remanence field strength in the pole shoes of the mixer magnets.)

3. Finally, the quantum mixer theory allows a reverse calculation of the total losses of the tuning circuit resulting from a device's measured RF performance. These calculations are beyond the scope of this thesis and thus shall only be given in reference [32]. A typical fitted 4.2 K loss factor value for an excellent UV-SNEP device is 0.85, but in case of device 040401-CMP-ii-D05 this loss factor is calculated to be only 0.5. This is a significant indication for additional losses in the tuning circuit and has occurred reproducibly for several devices. As it is highly improbable that the base electrode of the tuning circuit can cause such an effect (it processed identically for all types of devices), only the tuning circuit top electrode material remains as suspect.

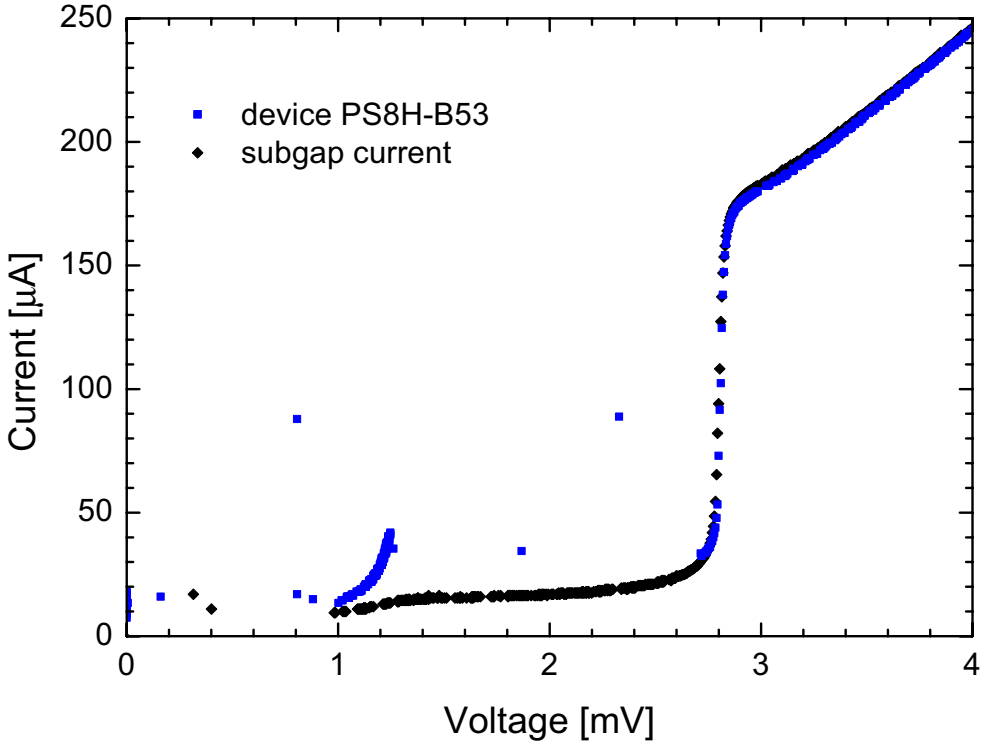


Figure 5.21: DC I-V characteristic of HIFI Band 2 mixer device PS8H-B53. A dominant resonance is visible at 1.25 mV. The subgap current level is visualized with an additional I-V curve (Josephson effects suppressed by magnetic field).

The simplest explanation for these observations is a contamination of the niobium layer during sputter-deposition. Some sort of outgasing behavior of the AZ5206 resist due to sputter-related heating might be a explanation.

As a result of this analysis development of the e-beam tuning circuit process has been halted for the time being. It is believed, though, that a change of the resist type and modification of some resist-related processing conditions will solve this problem. A non lift-off wiring definition scheme with negative e-beam resist also should eliminate this problem. All currently fabricated wafer batches which use e-beam lithography for junction area definition rely on conventional UV photolithography for the tuning circuit top electrode.

5.6.2 HIFI Band 2 mixer device performance

Presently the e-beam / CMP process is used for fabrication of the 490EBL and the HIFI Band 2 mixer devices. Because the 490EBL devices have not been RF characterized yet, the capabilities of the e-beam / CMP fabrication scheme shall be demonstrated on Band 2 mixer device PS8H-B53. This device is of an embedded trilayer type with a three-step transformer tuning circuit consisting of a NbTiN base and a Nb top electrode. Fig. 5.21 shows the DC I-V characteristic of this device. Junction properties are $V_{gap} = 2.81$ mV, $J_c = 13$ kA/cm^2 and a rather low

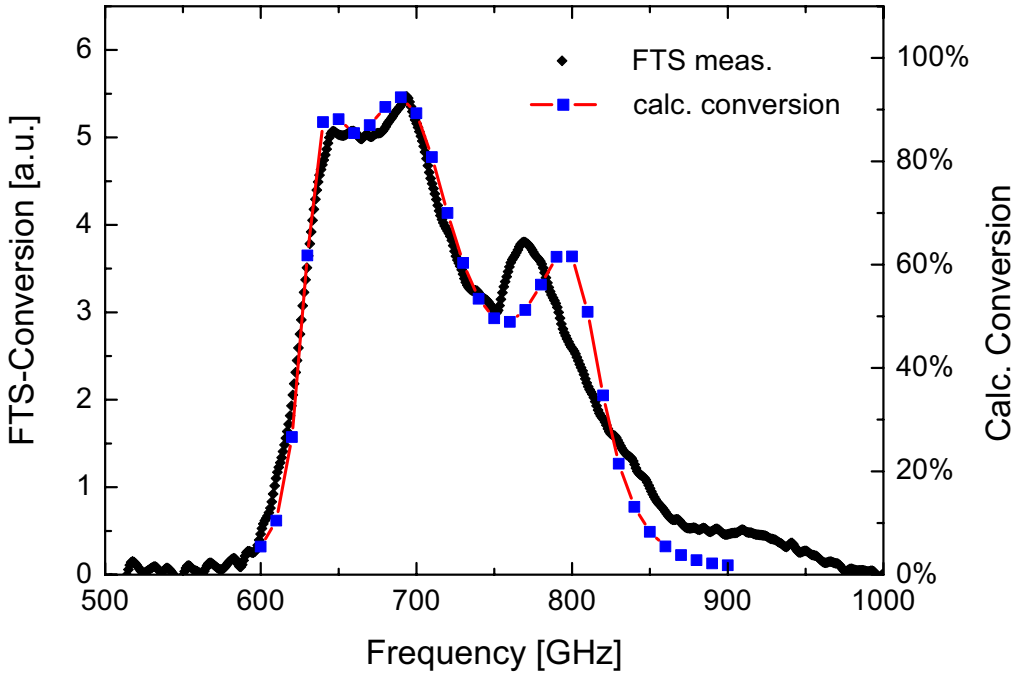


Figure 5.22: Comparison of a FTS-measured direct-detection frequency response (conversion) of device PS8H-B53 with a calculated conversion curve [76].

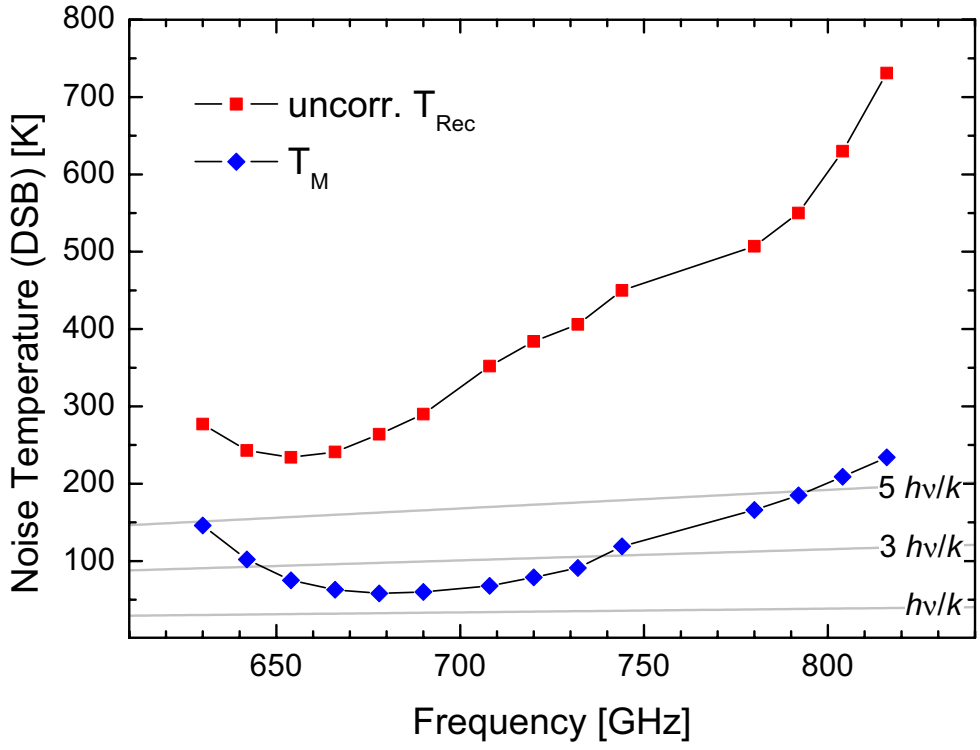


Figure 5.23: Uncorrected receiver and mixer noise temperatures (DSB) for HIFI Band 2 device PS8H-B53 measured at 2.8 K [76].

$R_{sg}/R_N = 7.6$. The low R_{sg}/R_N ratio is intrinsic to fabrication of embedded trilayer devices with NbTiN tuning base electrode at KOSMA and not a result of the e-beam / CMP process but seems to be related to the fabrication of the junction on top of the NbTiN layer. At $R_{sg}/R_N < 10$ the device RF performance is adversely affected (higher noise, lower gain) by the non-negligible subgap current.

Device PS8H-B53 is a good example for the flexibility of the e-beam junction area definition process because the PMMA junction area definition has been deliberately defined much larger than the design value. Based upon analysis of devices from previous processing runs the isotropic RIE behavior during junction etch of these embedded trilayer type devices needed to be compensated in order to yield correct junction areas. In this particular case the targeted $1.0\,\mu\mathrm{m}^2$ area makes an increase of junction side-length by $0.5\,\mu\mathrm{m}$ necessary.

Fig. 5.22 shows the conversion curve of a Fourier transform spectrometer (FTS) measurement. Although the ordinate scale of a FTS measurement does not directly correspond to an absolute value of sensitivity it gives clear indication of the RF bandwidth and frequency dependent device sensitivity. Additionally, a calculated conversion curve is scaled onto the measured curve. The best fit can be achieved for the parameters $J_c = 13\,\mathrm{kA/cm}^2$ and $A_J = 1\,\mu\mathrm{m}^2$ [76]. Due to the excellent agreement of both traces for frequencies up to $\approx 750\,\mathrm{GHz}$ this confirms that the actual junction area value is on target and, hence, underlines the reproducibility of the fabrication process.

Consequently, the high fabrication reproducibility is accompanied by good device performance. In Fig. 5.23 the uncorrected receiver noise temperatures and from them the calculated mixer noise temperatures are plotted for the specified HIFI Band 2 mixer frequency range. The best mixer noise temperatures T_m are less than twice the quantum limit and stays below 200 K for the complete Band 2 mixer range from 640–800 GHz [76].

6

Outlook – future work

6.1 Enhancement of junction area definition

Junction area reproducibility needs to be improved further, particularly for areas below $0.5\,\mu m^2$. THz SIS mixers require these small areas with the same area reproducibility as currently demonstrated for areas $\geq 0.64\,\mu m^2$ in order to achieve good performance. At THz frequencies an additional inductance contribution from current bending from the microstrip line into the small junction needs to be considered for precise calculation of tuning circuits. For these mixers it will be therefore interesting to define small, rectangular or diamond shaped junction areas. With the long side of the junctions oriented perpendicular to the microstrip line of the tuning circuit top electrode such geometry reduces this effect and thus the need for precise modeling. The smaller lateral dimensions involved with these geometries, though, demand an even higher lithographic resolution in order to achieve the same junction area reproducibility. The here presented e-beam lithography, etch mask deposition, lift-off and RIE processes demonstrate enough development potential to achieve this. Following will discuss a probable road map for future development.

6.1.1 E-beam lithography

Current e-beam fabrication uses a simple mono-layer PMMA scheme. Reduction of the PMMA thickness will improve lithography resolution and currently the minimal PMMA thicknesses required for a clean lift-off of the etch mask (Al or SiO_2) have not been determined yet. Some gain in resolution might be possible. But in the long-term a SIS fabrication compatible (resist baking temperatures) bilayer resist scheme seems worthwhile investigating as this will certainly circumvent any lift-off problems with the etch mask.

The KOSMA lithography system is currently being significantly upgraded with completely rewritten software by Karl Jacobs [35]. Mark recognition is implemented into the software so that an automated lithography process soon will be

possible for regular fabrication. It is expected that the automated mark recognition will yield more accurate and more reproducible alignment. It is expected that the relatively constant mark scan and recognition durations will yield a more constant local PMMA charging and consequently improved junction area reproducibility.

6.1.2 RIE

As discussed in Sec. 5.2.2 the junction area reproducibility is currently significantly limited by the RIE process. This is particularly evident for the embedded trilayer type devices (Band 2 mixer) due to the more complicated RIE process required. The baseline fabrication process for THz frequency junctions is of the same embedded trilayer type and the practice of defining larger than required junction areas for compensation of isotropic etch behavior will not succeed for these very small areas.

Thus the niobium RIE process has to be made significantly more anisotropic for definition of junction areas $< 0.5\,\mu\mathrm{m}^2$. During the final stages of this PhD the etch recipe has undergone several changes in order to improve the anisotropic behavior. The new SF_6+CHF_3 gas mixture based recipe, as used for the 490EBL devices, still needs more improving because it is unstable. In parallel, a SF_6+O_2 recipe is being developed and although not as anisotropic it seems more reproducible than the SF_6+CHF_3 recipe.

The biggest hopes lies in the new inductively-coupled plasma (ICP) reactive-ion etcher machine which will be purchased in the near future (funding has been cleared). The ICP RIE process can use significantly lower working pressures and thus promote anisotropic etch behavior. It allows independent control of the ion energy and the energy flux which is not possible with the simple parallel-plate etcher currently used. This should enable new processing options and yield a significantly more anisotropic RIE process.

The new ICP etcher will be equipped with an laser based end-point detection system (reflection measurement and interferometric) for more precise termination of the RIE process in order to minimize total etching time and generally increase RIE yield. It is planned to modify the existing RIE equipment with an self-built end-point system as well.

6.2 E-beam definition of tuning circuit top electrode

Process development for e-beam definition of the tuning circuit top electrode needs to be resumed. As the probable cause for the inferior RF mixer performance has been determined it should be possible to modify the already developed process to yield a functioning process with no contamination of the top electrode material. It is planned to use diluted AZ5214 resist in combination with a more thorough bake-out procedure together with the established e-beam parameters.

6.3 Enhancement of CMP

CMP planarization results also should be improved. As of autumn 2002 development has been halted for Herschel Band 2 mixer fabrication but will start again in summer 2003. Main focus will lie in using the new IBS polishing head with the latest wafer template design. The monolithic head has been favored for Herschel fabrication due to proven planarization result stability and safety (wafer breakage) even though the IBS head should improve planarization results. The variable back pressures possible with the IBS head will help to faster optimize processing conditions, presumably, with even lower back pressure values.

Stability of the wafer-to-wafer global planarization rate is addressed by several tasks which also should be beneficial to the within-wafer planarization uniformity:

1. The conditioning process can be improved. A new CVD diamond based conditioner will be used (model KINIK from Rodel) and the benefit of in-situ conditioning, i. e. parallel to wafer polishing, will be evaluated as the new IBS polisher is equipped with two polishing stations.

2. It is not known whether the shelf-life of the non-colloidal ILD1200 slurry is the cause for the MRR variations. A new colloidal slurry with a specified longer shelf-life will be introduced to the CMP process. Both Klebosol™ (Rodel) and Levasil™ (Bayer) types will be evaluated. The colloidal slurry also has the advantage that the agglomeration behavior is inhibited.

3. The slurry delivery system will be improved. A tandem diaphragm recirculation pump will be connected to the undiluted slurry holding tank and will feed the existing pump with point-of-use slurry dilution.

4. A new type of polishing pad will be evaluated.

At some time it will be interesting to enhance junction fabrication by using larger wafer diameters. For example integrated receiver designs require much larger devices and demand the use of larger substrates for economic fabrication. Principally this should not be a problem for the CMP process but actually be beneficial for the planarization characteristics. 2" wafer diameters would be directly compatible to existing fabrication hardware.

6.4 Submillimeter SIS mixer devices

In the near future SIS mixer design for groundbased observatories will focus on more complicated device design with more than one or two junctions. These integrated receiver circuits can incorporate sideband separation and balancing schemes and require up to 4 junctions [42, 43, 84]. Of course an e-beam based fabrication scheme is in advantage over conventional UV photolithography and

ensures that all junction areas are defined closely to the design values and that the microstrip lines are precisely aligned with regard to the junctions.

For very wide-band lower frequency applications ($< 700\,\mathrm{GHz}$) junction array devices seem interesting. These arrays use up to five junctions and can, additionally, require different sized junction areas, hence stressing the need for very reproducible junction definition [68, 75, 69, 74].

6.5 THz SIS mixer device development

The e-beam / CMP process lays a sound foundation for THz mixer device fabrication. In addition to the already discussed definition accuracy aspects new processing is required. Most importantly, AlN barrier technology needs to be developed. AlN to date is the best barrier material for the very high current density junctions required for THz SIS mixer design and is compatible to NbTiN junction electrode material. The technology is available to several groups and state of the art published results show that excellent R_{sg}/R_N ratios are achievable for very high current densities $J_c = 20$–$50\,\mathrm{kA/cm^2}$ [39, 47, 11]. For this reason initial fabrication development for AlN also has been initiated at KOSMA [73].

Furthermore the appropriate processing conditions for NbTiN as junction electrode material have to be established at KOSMA.

A

Process data

A.1 Fabrication recipe for 490EBL mask

batch 490EBL- **wafer**	SMART 460-492 GHz devices for KOSMA and HIFI Band 1 mixer backup devices for LERMA
	e-beam mask: junction definition: version date: 150 / 8 / (200 +30) nm trilayer 20 nm Al + 20 nm Au junction RIE mask 200 nm final SiO_2 thickness desired for tuning PMMA AR669.04 (600k, 4%) for junction definition (with 10 nm Al layer)
substrate: t = 268 µm ∅ = 25 mm fused quartz (INFRASIL 1)	process start: process end:

process step		target	comment
1.	wafer clean	IPA rinse, spin(4000, N_2) microscopic inspection: choose smaller diameter side as top measure thickness check substrate surface for scratches, edge for cracks dip in TCE used H_2O rinse **2:00** H_2O 1 (always ultra pure / deionized) H_2O rinse **2:00** H_2O 2 (p) IPA rinse **2:00** ACE 1 (p) IPA rinse **2:00** IPA (p) spin(4000, IPA rinse, IPA / N_2 blow x5)	**abbreviations** **IPA** = Isopropanol **TCE** = Trichlorethylene **ACE** = Acetone **p** = "process beaker" **if not explicitly stated, all times are ultrasonic agitation durations in min.:sec.** Marangoni: standard clean
2.	inspection of wafer cleaning (microscope)	wafer clean? else 1:00 H_2O 1:00 IPA IPA rinse spin(4000, IPA rinse, IPA / N_2) (swab + IPA +spin, only if necessary)	
3.	deposition of AlN etch stop layer blanket layer DC-sputtering in new sputtering machine 20 nm reactive-sputtered AlN	**position pallet in load-lock** **transfer of pallet into RIE chamber** **3:00** O_2 clean (10 Pa, 20 W, 220 V,10 sccm) transfer into main chamber evacuate to < $1 \cdot 10^{-7}$ mbar **5:00** Al pre-sputter (300 W, 300 V, 100 sccm, N_2, 0.4 Pa) **1:28** AlN sputter (300 W, 300 V, 100 sccm, N_2, 0.4 Pa)	

4.	deposition of trilayer (junction and tuning base electrode layers) blanket layer DC-sputtering O_2 clean Nb sputtering parameters **r(Nb, 300W) = 1.59 nm/s** [8.11.2002] Nb1 (base) = 150 nm Al = 8 nm Nb2 (top) = 230 nm 200 nm for tuning with SiO_2 as dielectric desired + 30 nm for CMP top electrode erosion during wiring sputter clean Al sputtering parameters r(Al,150W) = 0.89 nm/s r(Al,75W) = 0.59 nm/s	de-gas load lock (LL): 3h with quartz lamp $p \leq 4 \cdot 10^{-8}$mbar else 3:00 NbTi getter-sputter, wait ≥ 2 h (or overnight) turn on cooling for sputter station and cathodes: water, pump and Peltier (4 A) **10:00** Ar sputter-clean “490EBL trilayer” aperture of pallet, 100 W, 3 Pa **1:30 150°C** HP pre bake place substrate with some APIEZON on heated (90°C HP) sputter pallet, fix **diam. 22 aperture** (“490EBL trilayer”) onto pallet place pallet into LL evacuate to $1 \cdot 10^{-1}$mbar, then N_2 inlet through VK valve cooling LL RF cathode, **stays on** **1:00** wait evacuate to < $9 \cdot 10^{-6}$ mbar (≈ 1:00) **3:00** O_2 clean (10 Pa, **220 V**, ≈ 10 W, 25 sccm) reduce to 2.5 sccm for oxidation at end evacuate to < $4 \cdot 10^{-6}$ mbar (≈ 1:00) transfer into sputter chamber (SC) **2:00 wait to pre-sputter**, vacuum gauge stays off move aperture to pos. **3** switch power-supply to **DC-Sputter**, **Nb cathode** **3:00** Nb pre-sputter (**300** W, **250** sccm, Ar, **1.44** Pa) **1:34** Nb1 sputter (150 nm): move aperture to pos. **1** (300 W, 250 sccm, Ar, **1.45** Pa) let Ar in to 2.5E-1 mbar, then HK valve shut, cryo throttle shut, stop flow with HK valve **5:00 wait to pre-sputter**, vacuum gauge stays off, open cryo pump throttle prior Al pre-sputter move sputter plate to pos. **2** (1 1/3 clockwise) move aperture to pos. **4** switch power-supply to **Al cathode** **3:00** Al pre-sputter (**150** W, **250*** sccm, **1.88** Pa) **0:20** Al sputter (12 nm): move aperture to pos. **2** (**75** W, 250 sccm, **2.00** Pa) Ar off, cryo throttle full open move sputter plate back to pos. **1** pallet transfer into LL Al oxidation (**1.0** sccm O_2 – stop with VK valve - decrease flow very slowly to 1.5 sccm, then close turbo throttle, water cooling on) (j_c = 14 kA/cm^2 required by design): **9:00 - 9:30 @ 1.60** Pa **2:00** evacuate (**no** vacuum gauge), cooling LL off, leave VK valve open for 1:00 turn water cooling LL off transfer into SC **1:00 wait to pre-sputter**, vacuum gauge stays off move aperture to pos. **3**	reduce to 10 W for process at end and check O2 clean process impedance match **impedance match?** **temperature of substrate cooling =** (reading @ “Vorlauf”) for thermal contact prior Al sputtering (sputter cooling) **temperature of substrate cooling =** **oxidation parameters vary with substrate material and thickness!!** **static pressure during oxidation** **take time at half pressure values**

		switch power-supply to **Nb cathode** **3:00** Nb pre-sputter (**300** W, **250** sccm, Ar, **1.44** Pa) **2:25** Nb2 sputter (230 nm): move aperture to pos. **1** (300 W, 250 sccm, Ar, **1.45** Pa) Ar off, cryo throttle full open move sputter plate back to pos. **1** pallet transfer back to LL ventilate LL reduce Peltier current to 0A, switch off sputter station cooling pump	
5.	wafer cleaning step	heat up sputter pallet short on 90°C HP dip wafer in TCE used (p) / new (p) IPA rinse **0:30** IPA (p), rinse spin(4000, N2 + IPA, 5x)	
6.	definition of RF-chokes (AZ 5214 + AZ 726) **IMAGE REVERSAL**	*** PR in syringe must be new *, need HP at 120°C** clean mask if necessary: H_2O, ACE, IPA N_2 blow dry of center, swab with ACE / IPA for more persistent marks **1:30** 90°C HP pre bake **1:00** HMDS, wafer on spinner, no vacuum **0:40** spin(4000, thorough N_2 blow) AZ 5214 coat: spin(**0:40**, 4000 rpm) **1:30** 90°C HP soft bake (SB) **2:30** UV400 exp. edge bead removal (EBR), soft contact, diam. 21 mask **1:00** develop in AZ 726, H_2O rinse **0:40** spin(4000, N_2) **0:30** UV300 exp. “TRILAYER” **1:30** 120°C HP RB (reversal bake) **1:42** (**1.7 min**) UV300 flood exposure, no mask, wafer on Si subwafer, soft contact, O-ring on top **1:00** develop in AZ 726 thorough, but gentle H_2O rinse **0:40** spin(4000, **little** N_2 on wafer center)	
7.	inspection of RF-choke litho (microscope check)	definition O.K.? any residue left?	
8.	RIE of RF-chokes (trilayer etch) SF6 / CHF3 for Nb, Ar sputter-etch for Al2O3 / Al visual end-point determination through port hole in RIE chamber process is completely in-situ	turn on RIE PC for correct voltage reading **5:00** evacuate process gas lines for Ch.4 if NF3 used during last etch: max. flow on Ch.4, 5:00, gas=on: let flow decreases to zero place **VA template** in etcher pre-condition etcher: (switch Penning off) **30:00** Ar, 10 µbar, 6 sccm, 70/1 W @ **adjust to SF6 / CHF3 process:** 3/2 sccm, 10 µbar, **275V** (16/1 W): **impedance match!** use as little time as possible, else chamber contamination influences etch behavior!!! **2:00 before end of pre-conditioning:** **1:30** 90°C HP wafer bake place wafer on spinner, short N_2-blow	(recipe still under evaluation)

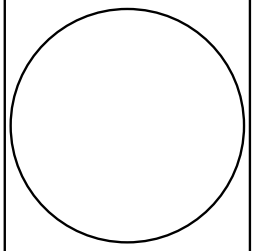
		place wafer in etcher and pump down LL $p_{vac} \leq 3 \cdot 10^{-2}$ mbar: transfer into main chamber $p_{vac} \leq 3 \cdot 10^{-5}$ mbar: start etching process **RIE Nb2 (230 nm):** (SF6 / CHF3, 3 / 2 sccm, 10µbar, **275V** (16/1 W), manual control **1:45 etch (clear-up + 20 s)** **sputter-etch Al2O3 / Al barrier** use first etching cycle for impedance match: Ar, 10 µbar, 6 sccm, 540V, 50 W, remote (PC) **17x 1:00** etch / 1:00 break, 10 µbar, 50 W, ~ 550V, **RIE Nb1 (150 nm):** (SF6 / CHF3, 3 / 2 sccm, 10µbar, **275V**, 17/2 W, manual): don't change matching increase P to yield 275 V **1:25 etch (clear-up + 20 s)**	
9.	inspection of trilayer RIE (microscope)	cleared? e-beam alignment crosses O.K?	
10.	PR removal	**1:00** soak Ace5 (p) **0:30** Ace 5 (p) **0:30** IPA (p) IPA rinse **0:40** spin(4000, IPA / N_2 x5)	
11.	inspection of PR removal (microscope)	wafer clean? spin-coat with PMMA	
12.	preparation for junction definition through e-beam lithography PMMA AR669.04 (600k, 4 %) + 10 nm Al for charge dissipation r(Al,75W) = 0.59 nm/s	let PMMA bottle heat up to room temperature **1:00** 90°C HP pre bake PMMA coat: **150 µl with micro pipette**, **no** filtering, **no** HMDS spin(**0:40**, 4000 rpm) **1:00 wait on spinner, no vacuum (PMMA re-flow)** **3:00** 120°C HP bake, **no vacuum** check: is PMMA layer clean and bubble free? put wafer on sputter pallet with very little APIEZON **see 3. for sputter procedures** (**no** plasma clean, diam. 22 "490EBL Al/Au" aperture) sputter **0:17** Al for 10 nm remove APIEZON with swab and little TCE spin(4000, little N_2) heat up wafer **0:30** on 90°C HP prior to loading into SEM load into SEM (scratches with metal tweezers for "definition" of large areas for later mask and RIE thickness	**replace PMMA in small bottle if older than 1 month** 220 nm thickness pre-sputter **3:00** when following reactive sputtering, else pre-sputter **1:30**

		measurements: on large rectangular areas next to UV alignment)	
13.	e-beam lithography of junctions	**follow procedures in SEM manual** e-beam dose to area variation: **see accompanying Excel spreadsheet:** **490EBL**……**.xls** (dose variation per device) **lithography (ACAD-)mask used:** **490EBL**……..**.dwg (AutoCAD 12 formatted)** 14.0 pA beam current and 20 kV acceleration voltage	
14.	PMMA development (MIBK AR600-**56**, stopper AR600-60)	**check wafer appearance prior to Al etch (substrate is "light gray" = thin Al layer): CCD system** **1:50** etch in Al etch solution (diluted **1:3** H_2O): use pipettes, move wafer from top to bottom of beaker to stir liquid, only slow movements else bubbles occur thorough rinse with H_2O **0:40** spin blow dry (4000, N_2) **check wafer appearance after Al etch (substrate should be "black" not grayish = Al gone)** **4:00** develop in AR600-**56** **0:30** stop in AR600-60 (or IPA) IPA rinse **0:40** spin blow dry (4000, N_2)	solution not too old? clear-up + 30 sec. **else etch longer, mix new etch solution for next wafer**
15.	e-beam area analysis (best image contrast)	**check and measure junction sizes, register results per device species into spreadsheet:** **490EBL**…….**_pmma_def.xls** in case discrepancies visible: **new e-beam process** clean for new PMMA coating: **2:00** Remover soak **0:15** Remover **0:30** ACE 5 (p) **0:30** IPA IPA rinse **0:40** spin(4000, IPA / N_2 x5) **go back to 10.**	

16.	definition of junction etch mask DC-sputter 20 nm Al +20 nm Au (passivation against isolation etch mask development) r(Al, 75W) = 0.59 nm/s r(Au, 25W) = 0.33 nm/s	**1:30** 90°C HP bake, switch on sputter station cooling (Peltier current = 4A) place wafer on pallet with little APIEZON, use diam. 22 “490EBL Al/Au” aperture **see 3. for sputter procedures** **plasma de-scum** **1:00** Ar, 3 Pa, **6 W**, 225 V, 33 sccm **transfer into main chamber, turn LL cooling off** **layer sputtering** **3:00** pre-sputter Al **0:34** Al, 75 W for 20 nm **0:30** pre-sputter Au **1:00** Au, 25 W for 20 nm	 “soft clean” temperature (“Vorlauf”) of sputter station =
17.	etch mask lift-off	heat up carrier on 90°C HP dip wafer in TCE used (p) / new (p) IPA rinse **20:00** soak wafer in **AR300-70** (p) remover, after 10:00: **10x** UA pulse swab wafer surface (on glove) **1:00** AR300-70 (p) UA IPA rinse **0:30** ACE lift-off 5 (p) IPA rinse **0:30** IPA 1 (p) IPA rinse **0:40** spin(4000, IPA / N_2 x5)	use minimum amount of UA!
18.	microscopic measurement of etch mask areas (difficult) and layer thickness metrology	wafer clean? lift-off of etch mask? **measure trilayer (several points) and etch mask thickness** (adjust sputtering rates?) calculate new Nb (300W) sputtering rate r*(Nb, 300W) =	 trilayer = nm (target = 392) etch mask = nm (target = 40)
19.	post metrology clean	IPA rinse **0:30** IPA (p) IPA rinse **0:40** spin(4000, IPA / N_2 x5) then resist coat, next step	
20.	definition of junction isolation (secondary etch mask) UV contact lithography AZ MIR701 + AZ 726	clean mask if necessary **1:30** 90°C HP pre bake **1:00** HMDS coat: wafer on spinner, no vacuum **0:40** spin(4000, thorough N_2 blow) AZ 7212 coat: spin(**0:40**, 4000 rpm) **1:00** 90°C HP SB **2:30** UV400 exp. EBR, soft, “diam. 21” **1:00** develop in AZ 726, H_2O rinse **0:40** spin(4000, N_2) **0:36** UV300 exp. “ISOLATION” **1:00 110°C PEB** **1:00** develop in AZ 726, H_2O rinse **0:40** spin(4000, N_2)	

		(**1:30** 90°C HP when process break) **RIE should follow**	
21.	Nb reflectivity measurement, pt.1	**measure reflectivity of Nb** (12bit gray, 1000x, 30x30 µm^2 area, histogram function, standard setting in OPTIMAS software, camera gain =+8 dB) keep microscope settings int(taper C24) = int(etch monitor middle) = int(etch monitor left top) = int(etch monitor right bottom) =	set microscope lighting to yield a value of roughly **2500**
22.	RIE of Nb2 layer (junction top electrode) with SF6 / CHF3 etch with visual end-point determination through port hole, check with reflectivity measurement	turn on RIE PC for correct voltage reading **5:00** evacuate process gas lines for Ch.4 if NF3 used during last etch: max. flow on Ch.4, 5:00, gas=on: let flow decreases to zero place **VA template** in etcher pre-condition etcher: (switch Penning off) **30:00** Ar, 10 µbar, 6 sccm, 70/1 W @ **adjust to SF6 / CHF3 process:** 3/2 sccm, 10 µbar, **275V** (16/1 W, manual control): **impedance match!** **use as little time as possible, else chamber contamination influences etch behavior!!!** **2:00 before end of pre-conditioning:** **1:30** 90°C HP wafer bake place wafer on spinner, short N_2-blow place wafer in etcher and pump down LL $p_{vac} \leq 3 \cdot 10^{-2}$ mbar: transfer into main chamber $p_{vac} \leq 3 \cdot 10^{-5}$ mbar: start etching process **RIE Nb2 (230 nm):** (SF6 / CHF3, 3 / 2 sccm, 10µbar, **275V**, 16/1 W, manual) **etch 4 : 00 (clear-up + 20 s)**	*reduce voltage!!!!* (recipe under evaluation) approx., final value tbd.
23.	measurement of reflectivity, pt. 2	**same settings as pt. 2, target delta=400-500** int(taper C24) = int(etch monitor middle) = int(etch monitor left top) = int(etch monitor right bottom) =	
24.	PR removal	**2:00** soak in ACE lift-off 2 (p) **0:30** ACE lift-off 2 (p) ACE rinse **1:00** ACE lift-off 3 (p) IPA rinse **1:00** IPA 1 (p) IPA rinse **0:40** spin(4000, IPA / N_2 x5)	
25.	inspection of junction RIE (microscope)	wafer clean? **measure exemplary junction areas for**	

		490EBL……._**RIE_def.xls** **and shoot some images for documentation purposes** additional clean: IPA rinse spin(4000, IPA / N_2 x5)	
26.	definition of CMP monitor and bond pad contact areas (for lift-off defined SiO2 holes) AZ 5214 + AZ 726 **IMAGE REVERSAL**	*** PR in syringe must be new *, need HP at 120°C,** clean mask with H_2O, ACE, IPA N_2 blow dry of center, paintbrush with ACE / IPA for more persistent marks) **1:30** 90°C HP pre bake **1:00** HMDS, wafer on spinner, no vacuum **0:40** spin(4000, thorough N_2 blow) AZ 5214 coat: spin(**0:40**, 4000 rpm) **1:30** 90°C HP SB **2:30** UV400 exp. EBR, soft, diam. 21 mask **1:00** develop in AZ 726, H_2O rinse **0:40** spin(4000, N_2) **0:30** UV300 exp. "SiO2 HOLES", hard contact **1:30** 120°C HP RB **1:42** (**1.7 min**) UV300 flood exposure, no mask, wafer on Si subwafer, soft contact **1:00** develop in AZ 726 thorough, but gentle H_2O rinse **0:40** spin(4000, **little** N_2 on wafer center)	
27.	inspection of litho (microscope)	use yellow filter on microscope place into rf sputterer	
28.	rf sputter deposition of tuning dielectric **600 nm SiO_2** (needed for planarization) dep. rate r (SiO2, 200 W) = 32.9 nm/min [11.2002] **200 W** (net P) p = 1.0 Pa, d = 50 mm target dist. 1.5x metalization layer thickness required for planarization *(sputter less, e.g. only 550 nm?)*	**1:30** 90°C HP bake place wafer on substrate carrier with APIEZON screw carrier onto station, center over rf cathode, check if shutter fits **cooling water changed to rf cathode?** **rf generator, match box cooling on** pump (turbo full power, turn Penning on), $p \leq 2 \cdot 10^{-5}$ mbar: plasma clean (Penning off) throttle turbo, open shutter, open needle valve **3:00** 4E-2 mbar (air via Ar gas line) re-connect Ar gas line, switch substrate cooling on, turbo full power, close shutter wait until $p \leq 1.5 \cdot 10^{-5}$ mbar: leave Ar valve open **5:00** evacuate gas line **5:00** Ar flow @ $1 \cdot 10^{-4}$ mbar, shut valve before opening Ar gas cylinder) set zero point Baratron, throttle turbo let Ar in to 180 mV for plasma ignition, switch rf generator routing to match box **1:00** pre-sputter, reduce Ar flow to **38 mV** (**1.0 Pa**), increase to 200 W net power (typically 203/3 W), impedance match? **5:00** Sputter 1 (200 W net) **5:00** cooling break 1 (reduce to 5 W, **shutter open**) **5:00** Sputter 2 **5:00** cooling break 2 **5:00** Sputter 3 **5:00** cooling break 3	approx. 2 h (temporary)

		3:14 Sputter 4 turn off rf generator, reduce P setting, switch routing back to sputter LL, stop Ar flow, close RIE valve and Ar cylinder **5:00** cool down phase, with rf cathode and substrate chamber vent	
29.	SiO_2 lift-off	heat up carrier on 90°C HP dip wafer in Tri used (p) / new (p) IPA rinse **20:00** soak in ACE lift-off (p) **1:00** ACE lift-off (p) ACE rinse **1:00** ACE lift-off 2 (p) IPA rinse **1:00** IPA (p) IPA rinse **0:40** spin(4000, IPA / N_2 x5) swab with Ace on spinner (stopped) if necessary	sputtered SiO_2 lift-off very difficult! try water, AZ remover (CMP should enhance lift-off)
30.	SiO_2 metrology	wafer clean, all PR removed? **measure SiO_2 distribution and calculate mean thickness** extra swabbing possible (IPA/ACE) mean SiO_2 thickness = nm final clean (backside of wafer must be clean for CMP) IPA rinse **0:30** IPA **0:40** spin(4000, IPA / N_2 x5)	
31.	preparation of substrate / subwafer combination for CMP 2” Si subwafer (290 µm) thin film wax bonding (LOGITECH OCON-195)	use wet bench in new litho lab **clean CMP subwafer** **1:00** TCE CMP beaker (if necessary) **1:00** H_2O CMP beaker **1:00** IPA CMP beaker IPA rinse **0:40** spin(new spinner, 4000, IPA / N_2 x5) **heat up CMP subwafer on HP (flow box) at 100°C** place drop of thin film wax on center of subwafer, distribute when molten **place substrate onto CMP subwafer** let wax draw under wafer move wafer to edge of subwafer and slowly back to the center (removes air bubbles) **place CMP weight centrally onto substrate / subwafer combination** move combo a little in circular motion (take care for wax spillovers) turn off HP, let combo cool down (≈ 10 min) take off weight very carefully (if stuck to combo heat up combination from cap side) **visual and microscopic check** wax film must be clean and completely bubble-free, else remove wafer and try again **combo clean** **1:00** soak in TCE CMP beaker **0:30** TCE CMP beaker **0:30** IPA CMP beaker	CMP weight (500 g, diam. 23, 1.2 N/cm2) with Teflon cap achieved wax thickness =

		IPA rinse **0:40** spin(new spinner, 4000, IPA / N_2 x5) **measure wax bonding layer thickness (digital gauge)** if thickness / planarity insufficient heat up combo, move combo with CMP weight to spread out wax layer **final clean for CMP** IPA rinse **0:30** IPA CMP beaker IPA rinse **0:40** spin(new spinner, 4000, IPA / N_2 x5) **cure thin film wax bonding layer** **0:15** 100°C sputter HP (flow box) or wait until wax film re-flows to substrate edge	achieved film planarity = target thickness < 5 µm planarity < ± 4 µm for all wafer points
32.	CMP startup polishing head: PA6,6 Template #1 with VA back recess depth = 1.27±0.01 mm with DF200 + subwafer = 185±5 µm approx. 100 µm wafer extension	fill up polishing slurry container with 750 ml turn on magnetic stirrer > 30 min in advance remove lid on IC-1000 polishing pad thoroughly flood pad with H_2O spin off H_2O **0:30** turn on slurry pump to purge slurry line (aim next to pad surface, maximum flow setting) rinse diamond conditioner with H_2O, place it onto pad initial pad pre-condition (dry pad / new process) **2x 5:00 H_2O** (80 / 80 rpm) first at 1/3 radius position, then at 2/3 radius position rinse conditioner and pad (spin off) with H_2O	standard polishing parameters: D_1 = pad speed = 20 rpm = 0.64 m/s D_2 = head speed = 24 rpm ≅ “100” in display U_2 ILD1200 slurry diluted to **3 wt. % silica conc.:** 160 ml slurry, fill to 750 ml with H_2O
33.	**CMP sequence** **step 1**	**5:00 pre-condition 20 rpm / 24 rpm (“100”)** continuous H_2O flow (250 ml) rinse head thoroughly with H_2O: rub backing film in wafer with glove (remove old slurry residue) place head onto pad **1:00 pad charging with slurry 20 rpm / 24 rpm** rinse polishing head with H_2O place CMP wafer/chip combo onto backing film carefully place polishing head onto polishing plate **3:00 polish 20 / 24 (“100”) rpm** **1:00 slurry removal / cleaning step** **20 rpm / 24 rpm** stop slurry feed continuously pour H_2O onto pad (250 ml) lift wafer / subwafer combo from head recess thorough H_2O rinse	**slurry flow 6ml/min** 110 bpm, 10% stroke start with 3:00 intervals, reduce to 0:30 or 0:15 duration for last CMP steps reduce to 0:30 for last CMP steps

		place combination in transport box filled with H_2O keep combo wet keep pad wet **intermediate clean of combo** H_2O rinse **0:30** H_2O CMP beaker **0:30** IPA CMP beaker **0:40** spin(new spinner, 4000, IPA / N_2 x5) **analysis** measure (field-)SiO_2 thickness measure junction isolation topography planarization state: field thickness: nm – nm ISO thickness: nm – nm remaining field oxide left ⇒ calculate approximate next polishing duration **cure thin film wax bonding layer** **0:15** 100°C sputter HP (flow box) or wait until wax film re-flows to substrate edge	metalization height = initial SiO_2 thickness =
34.	CMP step 2	pre-condition 5:00 polish : slurry removal / cleaning step **1:00** stop slurry feed, continuously pour H_2O onto pad (250 ml)	
35.	intermediate CMP clean 2	as above	
36.	CMP analysis 2	field thickness: nm – nm ISO thickness: nm – nm	
37.	following CMP steps (3-6)	as above	
38.	final CMP clean NH_4OH, 2% PVA sponge	Keep wafer wet H_2O rinse Scrub wafer combo with PVA sponge and NH_4OH (2%) solution H_2O rinse **0:30** H_2O CMP beaker **0:30** IPA CMP beaker **0:40** spin(new spinner, 4000, IPA / N_2 x5)	
39.	**CMP planarization analysis**	field thickness: nm – nm ISO thickness: nm – nm note colors of dielectric windows visual confirmation that top electrodes are dielectric free? topography measurements ⇒ calculate 2d dielectric thickness values record CMP data into **cmpdata.xls**	200 nm+ (wiring sputter clean) final dielectric thickness needed

40.	wafer removal & cleaning	clean wafer/subwafer combination 0:40 spin(4000, H2O + swab, IPA rinse, N_2) heat up wafer / subwafer on HP (flowbox) slide wafer off subwafer with tweezers clean wafer 1:00 TCE used dip TCE used (p) dip TCE (p) IPA rinse 1:00 H2O (p) IPA rinse 1:00 ACE 2 (p) IPA rinse 1:00 IPA 1 (p) IPA rinse 0:40 spin(4000, IPA rinse, N_2) clean subwafer 1:00 TCE 1:00 IPA spin(4000, IPA, N2)	
	definition of tuning top electrode ("wiring"), bond pad reinforcement, dicing alignment marks AZ 7212 + AZ 726	*** PR in syringe should not be older than 1 day *** **1:30** 90°C HP pre bake **1:00** HMDS coat: wafer on spinner, no vacuum **0:40** spin(4000, thorough N_2 blow) AZ 7212 coat: spin(**0:40**, 4000 rpm) **1:30** 90°C HP SB **3:00** UV400 exposure, soft **0:30** develop in AZ 726, H_2O rinse **0:40** spin(4000, N_2) **0:25** UV300, hard + vac exposure **0:45** 110°C HP PEB **1:00** develop in AZ 726, H_2O rinse **0:40** spin(4000, N_2)	note: MIR701 not yet evaluated for wiring litho / lift-off
41.	deposition of tuning top electrode, bond pad and dicing mark layers DC-sputter 350 nm Nb +30 nm Au low power Ar clean r(Nb, 300W) = 1.59nm/s p = 1.45 Pa r(Au, 25 W) =0.33 nm/s p = 1.75 Pa	clean "490EBL wiring" aperture of pallet use I/KI solution, H2O rinse, UA?, bake then **10:00** Ar sputter-clean, 100 W, 3 Pa (cover substrate position with aluminum foil) turn on cooling for sputter station and cathodes: water, pump and Peltier (4 A) **1:30** 90°C HP pre bake place substrate with some APIEZON on heated (90°C HP) sputter pallet place pallet into LL cooling LL RF cathode on evacuate to < $9 \cdot 10^{-6}$mbar **3:00** Ar clean (3.0 Pa, 405 V, **25 W**, 25 sccm) cooling LL RF cathode off evacuate to < $4 \cdot 10^{-6}$mbar (≈ 1:00) transfer into sputter chamber (SC) **2:00 wait to pre-sputter**, vacuum gauge stays off move aperture to pos. **3** switch power-supply to **DC-Sputter**, **Nb cathode** **3:00** Nb pre-sputter (**300** W, **250** sccm, Ar, **1.52** Pa) **2:00** Nb1 sputter: move aperture to pos. **1** (300 W, 250 sccm, Ar, **1.45** Pa) 1:00 cooling break: move aperture to pos. **3**,	

		plasma and gas on, 1.44 Pa **1:40** Nb2 sputter: move aperture to pos. **1** (300 W, 250 sccm, Ar, **1.45** Pa) gas off, open cryo move sputter plate to pos. (2 2/3 clockwise) move aperture to pos. **1** switch power-supply to **Au cathode** **0:30** Au pre-sputter (**25** W, **250** sccm, **1.75** Pa) **1:30** Au sputter (30 nm): move aperture to pos. **3** (**25** W, 250 sccm, 1.75 Pa) Ar off, cryo throttle full open move sputter plate back to pos. **1** pallet transfer into LL ventilate LL reduce Peltier current to 0A, switch glycol pump off	
42.	wiring lift-off	heat up carrier on 90°C HP dip wafer in Tri used (p) / new (p) IPA rinse **20:00** soak in ACE lift-off (p) **1:00** ACE lift-off (p) IPA rinse swab with Ace on spinner (stopped) **1:00** ACE lift-off 1 (p) **1:00** ACE lift-off 5 (p) IPA rinse **0:30** IPA (p) IPA rinse **0:40** spin(4000, IPA / N_2 x5)	
43.	wiring layer metrology	measure total thickness of wiring layer (SiO_2 removal approx. 15 nm through Ar sputter clean)	thickness =
44.	protection layer for dipstick dicing	coat with PR for protection **1:30** 90°C HP pre-bake **1:00** HMDS coat: wafer on spinner, no vacuum **0:40** spin(4000, thorough N_2 blow) AZ 5214 coat: spin(**0:40**, 4000 rpm) **1:30** 90°C HP SB	

A.2 Metal wet-etch solutions

Al wet-etch

85 vol%	H_3PO_4
5 vol%	HNO_3
5 vol%	CH_3COOH
5 vol%	H_2O
usage	1:3 diluted with H_2O

Cu wet-etch

20 weight%	$Fe(III)Cl_3$ (solid)
80 weight%	H_2O
usage	10 drops diluted with 40 ml H_2O

A.3 SiO_2 thickness color chart

Thickness [nm]	Color
50	tan
70	brown
100	dark - red violet
120	royal blue
150	light - metallic blue
170	metallic - very light yellow green
200	light gold or yellow slightly metallic
220	gold with slight yellow orange
250	orange - melon
270	red violet
300	blue - violet blue
310	blue
320	blue - blue green
340	light green
350	green - yellow green
360	yellow green
370	yellow
390	light orange
410	carnation pink
420	violet red
440	red violet
460	violet
470	blue violet

Thickness [nm]	Color
490	blue
500	blue green
520	green
540	yellow green
560	green yellow
570	yellow - “yellowish” (light gray - metallic)
580	light orange - yellow - pink
600	carnation pink
630	violet red
680	“bluish” (violet red, blue green, grayish)
720	blue green - green
770	“yellowish”
800	orange
820	salmon
850	dull, light red violet
860	violet
870	blue violet
890	blue
920	blue green
950	dull yellow green
970	yellow - “yellowish”
990	orange
1000	carnation pink

B

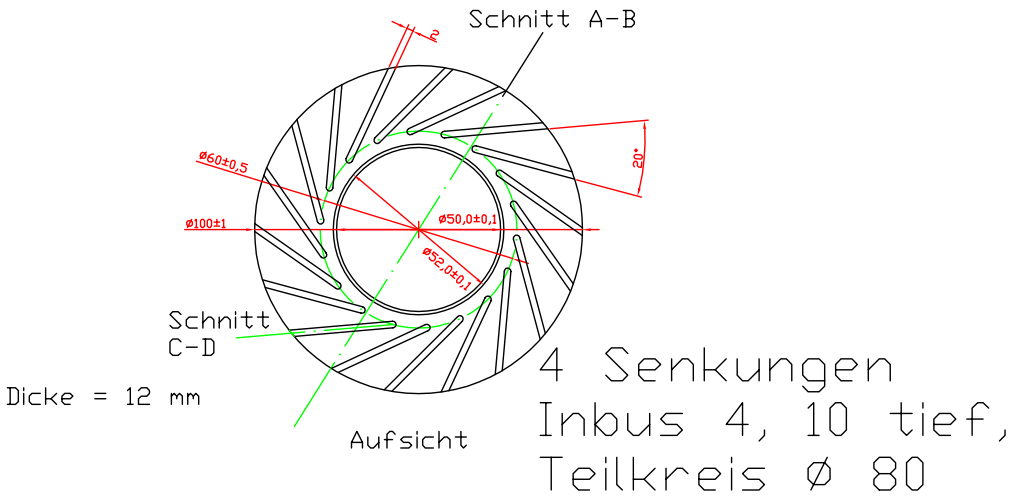
Tuning circuit parameters of 475 GHz SMART devices

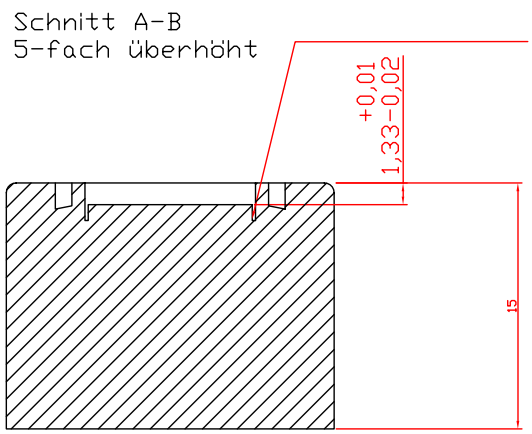
ID	choke	tuning	A_J	σ_n	w_1	l_1	w_2	l_2	w_3	l_3	P(460)	P(490)	comment
490ebl_ap_bs200_A081_sn_18	asymm.	trafo	0.81	1.8	2.5	7.9	27	73	4.1	59	0.969	0.965	centered on 460 and 490 GHz
490ebl_ap_bs200_A081_sn_19	asymm.	trafo	0.81	1.9	3	9.5	24	71	3.6	60	0.967	0.965	centered on 460 and 490 GHz
490ebl_ap_bs200_A081_sn_19_+20_mod	asymm.	trafo	0.81	1.9	2.5	5.3	28	77	3.5	47	0.686	0.964	+ 20 GHz
490ebl_ap_bs200_A081_sn_19_-20	asymm.	trafo	0.81	1.9	2.5	15.4	13	52	3.5	86	0.937	0.588	- 20 GHz, nur max. 94%
490ebl_ap_bs200_A064_sn_18	asymm.	trafo	0.64	1.8	2.5	9.5	25	80	3.9	58	0.967	0.964	centered on 460 and 490 GHz
490ebl_ap_bs200_A064_sn_19	asymm.	trafo	0.64	1.9	3	13.1	20	67	3.5	62	0.964	0.965	centered on 460 and 490 GHz
490ebl_ap_bs200_A064_sn_19_+20_mod	asymm.	trafo	0.64	1.9	2.5	7.8	25	75	3.5	47	0.706	0.967	+ 20 GHz
490ebl_ap_bs200_A064_sn_19_-20	asymm.	trafo	0.64	1.9	2.5	19.8	14	45	3.8	84	0.93	0.656	- 20 GHz, only max. 94%
490ebl_sp_bs200_A081_sn_18	symm.	trafo	0.81	1.8	2.5	9.5	31	56	3.5	60	0.967	0.959	centered on 460 and 490 GHz
490ebl_sp_bs200_A081_sn_19	symm.	trafo	0.81	1.9	3	11.1	35	58	4	60	0.965	0.958	centered on 460 and 490 GHz
490ebl_sp_bs200_A081_sn_19_+20	symm.	trafo	0.81	1.9	2.5	8.5	34	58	3.6	57	0.914	0.954	+ 20 GHz, wideband: 485-515> 95%
490ebl_sp_bs200_A081_sn_19_-20	symm.	trafo	0.81	1.9	2.5	12	25	53	3.5	67	0.951	0.875	- 20 GHz, wideband: 440-480 > 95%
490ebl_sp_bs200_A064_sn_18_mod	symm.	trafo	0.64	1.8	2.5	12	28	56	3.5	60	0.966	0.958	centered on 460 and 490 GHz
490ebl_sp_bs200_A064_sn_19_mod	symm.	trafo	0.64	1.9	3	14.5	29	53	3.5	61	0.966	0.96	centered on 460 and 490 GHz
490ebl_sp_bs200_A064_sn_19_+20_mod	symm.	trafo	0.64	1.9	2.5	10.8	32	55	3.6	56	0.844	0.959	+ 20 GHz
490ebl_sp_bs200_A064_sn_19_-20_mod	symm.	trafo	0.64	1.9	2.5	15.8	27	44	3.8	68	0.953	0.856	- 20 GHz
490ebl_test450_bs200_A064_sn_19	symm.	jctest	0.64	1.9	7.9	95					0.96	0.338	centered on 450 GHz
490ebl_test450_bs200_A081_sn_19	symm.	jctest	0.81	1.9	8.2	90.5					0.96	0.35	centered on 450 GHz
490ebl_test450_bs200_A196_sn_19	symm.	jctest	1.96	1.9	11.7	80.5					0.952	0.263	centered on 450 GHz
490ebl_test450_bs200_A256_sn_19	symm.	jctest	2.56	1.9	13	78					0.95	0.238	centered on 450 GHz
490ebl_test450_bs200_A289_sn_19	symm.	jctest	2.89	1.9	13.3	76.5					0.95	0.238	centered on 450 GHz
490ebl_test490_bs200_A064_sn_19	symm.	jctest	0.64	1.9	6.2	81					0.568	0.955	centered on 490 GHz
490ebl_test490_bs200_A081_sn_19	symm.	jctest	0.81	1.9	6.9	78.5					0.551	0.952	centered on 490 GHz
490ebl_test490_bs200_A196_sn_19	symm.	jctest	1.96	1.9	9.9	70.5					0.463	0.942	centered on 490 GHz
490ebl_test490_bs200_A256_sn_19	symm.	jctest	2.56	1.9	11	68.5					0.419	0.939	centered on 490 GHz
490ebl_test490_bs200_A289_sn_19	symm.	jctest	2.89	1.9	11.8	68					0.403	0.936	centered on 490 GHz

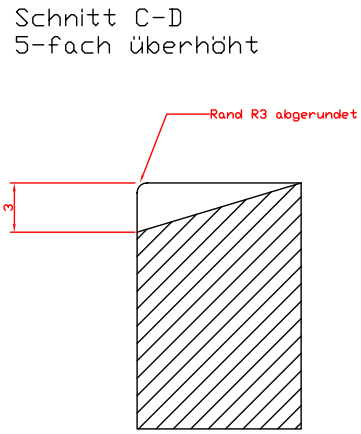
Table B.1: Summary of the integrated tuning circuit design on mask 490EBL (475 GHz SMART devices). l_J is the junction sidelength, σ_n the normal conductivity of niobium in $10^7\,\Omega^{-1}\mathrm{m}^{-1}$ and the w_i and l_i are the widths and lengths of the microstrip segments as explained in Fig. 2.12, respectively. P(460) and P(490) denote the power coupling to the junction as calculated with the ABCD matrices formalism for the frequencies 460 GHz and 490 GHz, respectively.

C

CAD drawing of wafer carrier and polishing head







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Erklärung

Ich versichere, dass ich die von mir vorgelegte Dissertation selbständig angefertigt, die benutzten Quellen und Hilfsmittel vollständig angegeben und die Stellen der Arbeit—einschließlich Tabellen, Karten und Abbildungen—, die anderen Werken im Wortlaut oder dem Sinn nach entnommen sind, in jedem Einzelfall als Entlehnung kenntlich gemacht habe; dass diese Dissertation noch keiner anderen Fakultät oder Universität zur Prüfung vorgelegen hat; dass sie—abgesehen von unten angegebenen Teilpublikationen—noch nicht veröffentlicht worden ist sowie, dass ich eine solche Veröffentlichung vor Abschluss des Promotionsverfahrens nicht vornehmen werde. Die Bestimmungen dieser Promotionsordnung sind mir bekannt. Die von mir vorgelegte Dissertation ist von Prof. Dr. J. Stutzki betreut worden.

Teilpublikationen

[1] P. Pütz and K. Jacobs. E-Beam SIS Junction Fabrication using CMP and E-Beam Defined Wiring Layer. In T. W. Crowe and R. M. Weikle, editors, *Proc. 10th Int. Symp. on Space Terahertz Technology*, pages 118–129, Charlottesville, VA, March 1999. University of Virginia.

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Kurzfassung

Diese Doktorarbeit beschreibt die Entwicklung eines verbesserten Fabrikationsverfahrens zur Herstellung von Supraleiter-Isolator-Supraleiter (SIS) Mischer-Elementen für den Einsatz in radioastronomischen Heterodynempfängern. Dafür wurde die Definition der Submikrometer großen Tunnelelement-Fläche und der integrierten Anpassstruktur auf ein elektronenstrahllithographisches Verfahren umgestellt, um so den höheren Anforderung moderner und zukünftiger Mischerelemente-Designs nach größerer Präzision dieser Strukturen gerecht zu werden. Zusätzlich ist ein Planarisierungs-Verfahren, basierend auf chemisch-mechanischem Polieren (CMP) für die Fertigung bei KOSMA neu entwickelt worden, um die Elektronenstrahllithographie bei der Tunnelelement-Definition in die Fabrikation integrieren zu können.

Es wird anhand von Messergebnissen gezeigt, dass sich das Elektronenstrahllithographie-CMP-Verfahren zur Fertigung der neuen Generation von Mischerelementen qualifiziert und darüber hinaus ausreichend Entwicklungspotenzial für zukünftige Mischer-Entwicklungen im THz-Frequenzbereich bietet. Die Fertigung der HIFI Band 2 Mischerelemente für das Herschel Satellitenteleskop profitiert maßgeblich von dem neuen Herstellungsverfahren, da die Implementierung von CMP eine deutliche Verbesserung der Strom-Spannungs-Charakteristika der Mischerelemente bewirkt.

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