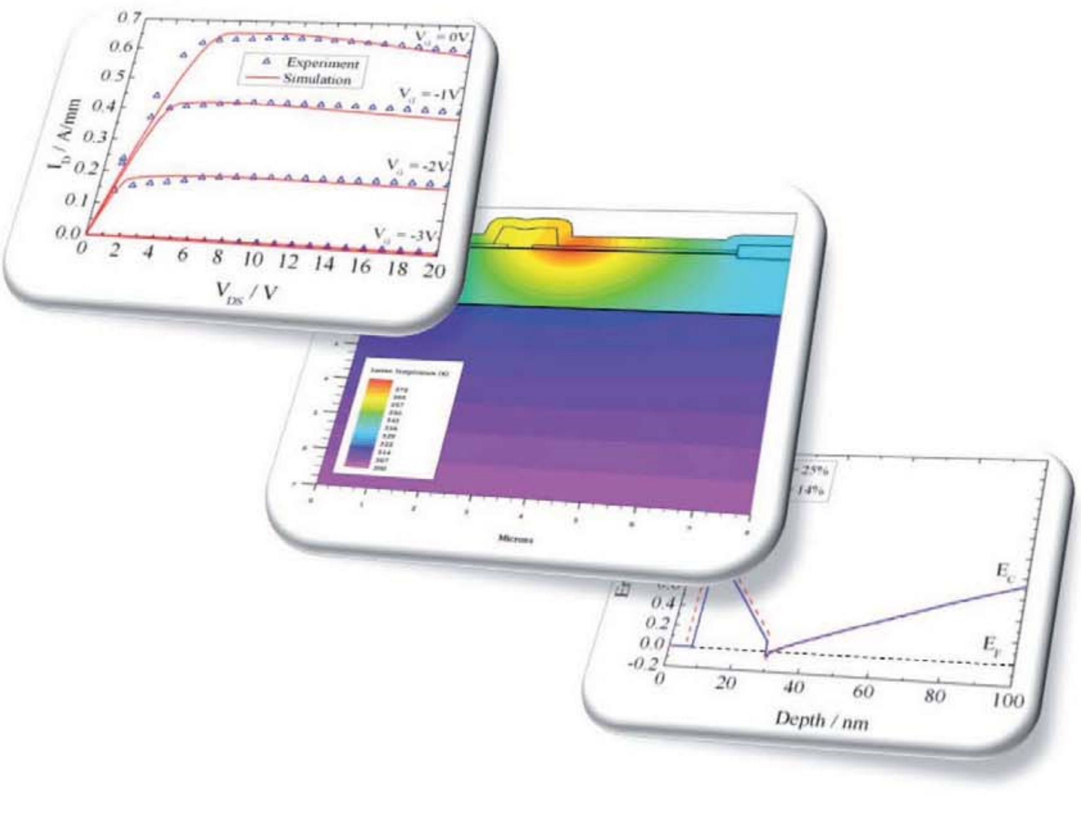
Michael Hosch

Analysis and Optimization of AlGaN/GaN High Electron Mobility Transistors for Microwave Applications



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to my family

"The grand aim of all science is to cover the greatest number of empirical facts by logical deduction from the smallest number of hypotheses or axioms."

- Albert Einstein

"When you know a thing, to hold that you know it; and when you do not know a thing, to allow that you do not know it - this is knowledge."

- Confucius

"Never fear big long words. Big long words mean little things. All big things have little names, such as life and death, peace and war, or dawn, day, night, hope, love, home. Learn to use little words in a big way. It is hard to do, but they say what you mean. When you don't know what you mean, use big words. That often fools little people."

- Arthur Kudner (... to his son)

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Contents

Chapter 1

Introduction

THE High Electron Mobility Transistor (HEMT) or Modulation Doped Field Effect Transistor (MODFET) principle has been published in 1980 by Mimura [1] and Delagebeaudeuf [2] independently as a result of research efforts to improve the microwave behavior of Field Effect Transistors (FET). Since that time researchers all over the world have been working to improve these transistors to achieve higher and higher performance in monolithic microwave integrated circuits (MMIC). Today the HEMT is, besides the Heterojunction Bipolar Transistor (HBT), the state-of-the-art device for microwave ($1 \ldots 30\,\mathrm{GHz}$) and millimeter wave ($> 30\,\mathrm{GHz}$) MMIC applications. To reach such high frequency regimes a device with improved carrier mobility and an adequate noise level is needed. Therefore the formerly used Metal Semiconductor Field Effect Transistor (MESFET) was modified such that heterostructures were introduced to separate mobile charge carriers from fixed ionized impurities to increase their mobility.

HEMTs are meanwhile available in every commercial III-V material system. Although today Silicon-Germanium (SiGe) HBT circuits achieve operation frequencies in the high millimeter wave regime [3] up to 79 GHz [4], for higher frequencies, lower noise level or higher power, compound semiconductors such as Gallium Arsenide (GaAs) and Indium Phosphide (InP) are the dominant materials for HEMT devices in the microwave and millimeter wave regime.

Under current research and development for high power microwave applications, however, Gallium Nitride (GaN) has become the predominant material system among all III-V technologies since it combines the capabilities to operate at high power and high frequency. A comparison with other material systems is shown in Fig. 1.1. GaN-based devices handle very high signal level and bias points due to three terminal breakdown voltages of several hundreds of volts, allowing power densities even twenty times higher compared to GaAs-based devices [27]. Very high power densities then result in power added efficiencies (PAE) close to the theoretical maxi-

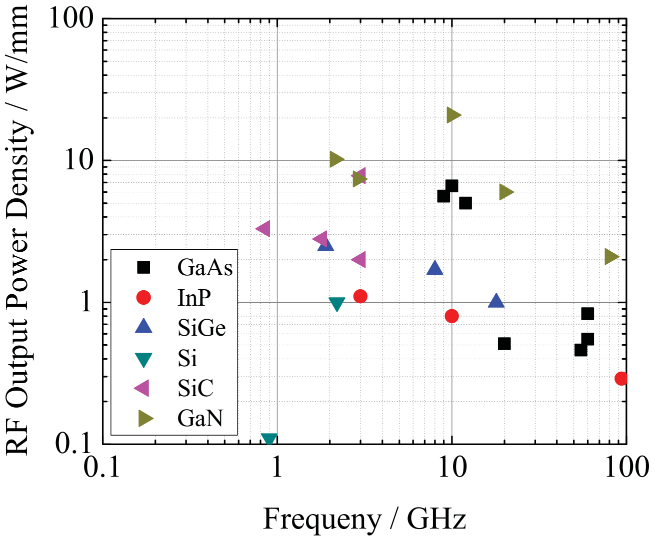


Figure 1.1: Comparison of power vs. frequency capability of Si- and SiC-based [5–13], GaAs- and InP-based [14–22] and GaN-based [23–27] technologies.

mum for each amplifier class. Especially in base station [28] and radar applications high power added efficiency over a very large bandwidth is desired. Since there are applications requiring a bandwidth of more than 100 % of the center frequency [29,30] an intrinsic power added efficiency as high as possible must be provided by the power devices in order to guarantee a high PAE over the whole bandwidth for those wide-band applications.

However, the microwave characteristics of such devices are limited due to non-idealities. Very often the non-ideal behavior is related to trapping effects, but also leakage currents and thermal management play an important role. To reduce or even avoid these non-idealities in order to overcome the limitation in microwave capability of those devices, it is essential to understand the nature and the origin of these effects. To assess non-ideal behavior of devices by electrical and thermal characterization requires various characterization techniques like DC, pulsed IV, small-signal RF, large-signal RF as well as LF and RF noise characterization for the electrical part and micro-Raman thermography as a thermal characterization technique. To investigate the origin of phenomena seen in those kinds of electrical and thermal characterization, physical device simulation is necessary to obtain an insight into the device physics. This kind of investigation of non-idealities in AlGaN/GaN devices for high-power microwave applications is the core intention of this work. It covers all aspects which are of importance to understand the non-ideal behavior of AlGaN/GaN HEMTs in microwave applications. The thesis starts with a brief overview of important material properties of group-III-nitrides in chapter 2. In comparison to other semiconductors it will become clear why GaN is promising for high-power microwave applications. An introduction of the basic operation principle of GaN-based high electron mobility transistor and the physical modelling follows in chapter 3. In chapter 4 then the non-ideal behavior of AlGaN/GaN HEMTs under DC and microwave operation is investigated and discussed in detail. Here, several different characterization techniques are utilized to assess the non-idealities in the devices and device simulations are performed to understand their physical origin. More general aspects for the improvement of the microwave performance of AlGaN/GaN HEMTs will be covered in chapter 5, where the impact of the layout and epitaxial layer sequence on the microwave performance is discussed. In this chapter it will be pointed out that the layout of the devices and the design of the epitaxial layers are as important as the processing in the design and development process of a GaN technology. Finally the thesis will be summarized and conclusions will be drawn in chapter 6.

Chapter 2

Group-III-Nitrides and their Heterostructures

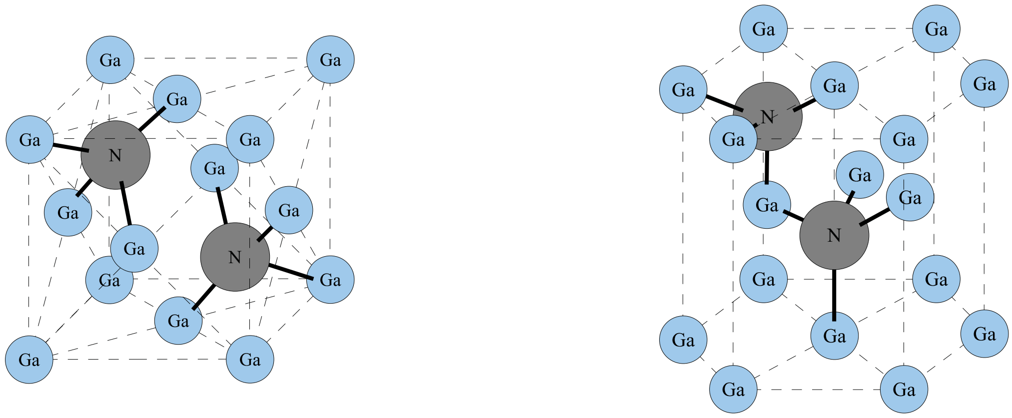
GROUP-III-NITRIDES have been under investigation for approximately 20 years and are therefore relatively young. Many properties are not fully understood, so that research into these materials remains a hot topic. In this chapter the general properties of group-III-nitrides will be discussed. Starting with a detailed overview of the basic material properties of GaN, the advantages of group-III-nitrides in microwave applications will become clear by comparison of GaN with well established materials like Si or GaAs. In the end the properties of AlGaN/GaN heterostructures will be discussed for a fundamental understanding of GaN-based HEMTs.

2.1 Gallium Nitride

To investigate material parameters of GaN was far beyond the scope of this work. However, knowing about the material properties is essential to understand device behavior. Therefore, the data presented in this section is a summary of state-of-the-art material parameters compiled various research groups working on the basic material properties of group-III-nitride materials.

2.1.1 Lattice Properties

Basically, GaN is available in the three different lattice configurations Wurtzite, Zinc Blende and Rock Salt, but the Rock Salt configuration is not important for electronic devices [31,32]. The Zinc Blende configuration on the other hand could be in principle used for electronic applications but suffers from two major drawbacks with respect to electronic devices.



(a) Face centered cubic unity cell of GaN in Zinc Blende phase.

(b) Simple hexagonal unity cell of GaN in Wurtzite phase.

Figure 2.1: Unity cells of GaN related to different lattice configurations.

The first important drawback is due to the fact that the Zinc Blende structure is not thermodynamically stable at room temperature. Thus, it is very hard to grow epitaxial layers with reasonably good lattice quality because this instability add additional effort to force the molecules into crystalline order by a proper substrate and adequate growth conditions which are not easy to handle. As the substrate is of importance for the Zinc Blende configuration since the unity cell of the Zinc Blende lattice is face centered cubic (FCC), as depicted in Fig. 2.1(a). This means that also a substrate with an FCC unity cell is needed to force GaN to grow in Zinc Blende configuration. One option for this is GaAs [33], but due to its poor thermal characteristics GaAs is not suitable as a substrate for high power devices like AlGaN/GaN HEMTs. The second major drawback of GaN in Zinc Blende phase is again related to its FCC unity cell. GaN in Zinc Blende phase is totally free of polarization. Ga-atoms and N-atoms form a dipole due to the high electronegativity of Nitrogen resulting in a larger ion radius as depicted in Fig. 2.2. Due to the symmetry of the FCC unity cell of the Zinc Blende phase the vectors of the polarization field $\vec{E}_{\mathrm{pol}}$ cancel out. This results in a GaN material that is free of any polarization field so that the big advantage for GaN-based heterostructures, providing high sheet charge densities just due to the polarization without any applied doping is gone. This will be discussed in more detail in section 2.3.

Due to the exclusion of the Rock Salt and Zinc Blende configurations the only phase of GaN remaining reasonable for electronic devices is the Wurtzite phase which is the thermodynamically stable phase of GaN at room temperature and therefore the easiest to growth among all available phase configurations. Its unity cell is simple hexagonal, as shown in Fig. 2.1(b), and therefore provides a high spontaneous and piezoelectric polarization at the same time along the c-axis due

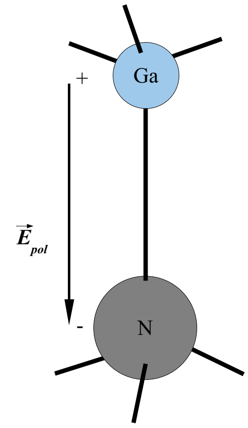


Figure 2.2: GaN dipole as a result of high electronegativity of Nitrogen.

to its low symmetry. The most common substrates for GaN to be grown on are Sapphire (Al_2O_3), Silicon (Si) and Silicon Carbide (SiC). Other advanced materials like diamond [34,35] or native GaN substrates [36] are currently the object of research. They may further reduce the defect density of epitaxial layers grown on but offering a thermal management of GaN-based power devices comparable to those fabricated on Si substrates. Native GaN substrates are currently of most interest for optoelectronics applications like solid-state lasers. The most important lattice and band structure parameters of GaN are summarized in table 2.1.

2.1.2 Electrical and Thermal Material Properties

Electrical and thermal properties are most important for electronic devices. Hence, a short summary of all relevant electrical and thermal properties of GaN shall be given in this subsection. The big advantage of GaN among all semiconductors used for RF and microwave technologies is the high electric breakdown field strength due to the large band gap in combination with a reasonably high electron mobility. This makes GaN suitable for operation at high power densities and high frequencies at the same time. A detailed comparison to other semiconductors will be given in section 2.2. On the other hand, high power operation gives rise to the need for enhanced thermal management. The thermal conductivity of GaN is very comparable to Si, however, since GaN is grown on hybrid substrates, mostly SiC is used to enhance the thermal management since its thermal conductivity is approximately three times higher than Si and even eight times higher than GaAs. Because GaN is grown on 4H-SiC the latter's thermal properties are very important and therefore also considered in this summary. All relevant electrical and thermal parameters are summarized in table 2.2.

Parameter	**Value**
Band gap E_G	$3.39\,\mathrm{eV}$
Electron affinity χ	$4.1\,\mathrm{eV}$
Number of atoms in $1\,\mathrm{cm}^3$	$8.9 \cdot 10^{22}$
Density	$6.15\,\mathrm{g/cm}^3$
Effective electron mass	$0.2 \cdot m_0$
Effective hole mass (heavy)	$1.4 \cdot m_0$
Effective hole mass (light)	$0.3 \cdot m_0$
Effective hole mass (split-off band)	$0.6 \cdot m_0$
Lattice constant a	$3.189\,\mathrm{Å}$
Lattice constant c	$5.186\,\mathrm{Å}$
Effective conduction band density of states N_C	$2.3 \cdot 10^{18}\,\mathrm{cm}^{-3}$
Effective valence band density of states N_V	$4.6 \cdot 10^{19}\,\mathrm{cm}^{-3}$

Table 2.1: Lattice and band structure parameters of GaN in Wurtzite phase at $T = 300\,\mathrm{K}$ [31].

Parameter	**Value**
Electric breakdown field E_B	$5 \cdot 10^6\,\mathrm{V/cm}$
Electron drift saturation velocity $v_\mathrm{sat,n}$	$2.6 \cdot 10^5\,\mathrm{m/s}$
Hole drift saturation velocity $v_\mathrm{sat,p}$	$9.4 \cdot 10^4\,\mathrm{m/s}$
Electron low-field mobility μ_n	$1000\,\mathrm{cm}^2/\mathrm{Vs}$
Hole low-field mobility μ_n	$200\,\mathrm{cm}^2/\mathrm{Vs}$
Permittivity ε (static)	8.9
Permittivity ε (high frequency)	5.35
Thermal conductivity σ_th	$1.3\,\mathrm{W/cmK}$
Permittivity (4H-SiC) ε (static)	9.66
Permittivity (4H-SiC) ε (high frequency)	6.52
Thermal conductivity (4H-SiC) σ_th	$4.2\,\mathrm{W/cmK}$

Table 2.2: Electrical and thermal parameters of GaN in Wurtzite phase at $T = 300\,\mathrm{K}$ [31].

2.2 Gallium Nitride for Microwave Applications

Several figures of merit assess the suitability of semiconductor materials for RF and microwave applications. *Johnson's Figure of Merit* (JFOM) judges the suitability of a semiconductor material using its electric breakdown field strength E_B and drift saturation velocity v_sat of the minority carriers as parameters as shown in equation (2.1) [37].

$$\mathrm{JFOM} = \frac{E_\mathrm{B} \cdot v_\mathrm{sat}}{2\pi} \tag{2.1}$$

JFOM provides an upper limit to the product of breakdown voltage and transit frequency, but does not take thermal aspects into account. Therefore, very often in addition to the JFOM *Keyes's Figure of Merit* (KFOM) is given which is a measure for the thermal limitation of the switching behavior of transistors used in integrated circuits. It is given by equation (2.2) [38]. Here, σ_th is the thermal conductivity, v_sat the drift saturation velocity of the majority carriers, c is the speed of light and ε the dielectric constant of the used material.

$$\mathrm{KFOM} = \sigma_\mathrm{th} \cdot \sqrt{\frac{c \cdot v_\mathrm{sat}}{4\pi \cdot \varepsilon}} \tag{2.2}$$

The third commonly used figure of merit is *Baliga's Figure of Merit* (BFOM) which judges the material by its conduction losses in a field effect transistor. The BFOM is given by equation (2.3) and uses the dielectric constant ε, the low-field mobility μ and the band gap E_G as parameters [39].

$$\mathrm{BFOM} = \varepsilon \cdot \mu \cdot E_\mathrm{G}^3 \tag{2.3}$$

To better assess high power high frequency semiconductor devices, according to [40] this figure of merit was further elaborated and *Baliga's High Frequency Figure of Merit* (BHFFOM) was derived as shown in equation (2.4). Here E_B is the electric breakdown field strength, μ the low-field mobility, V_G the applied gate voltage and V_B the breakdown voltage of the device.

$$\mathrm{BHFFOM} = \mu \cdot E_\mathrm{B}^2 \cdot \frac{\sqrt{V_\mathrm{G}}}{2 \cdot V_\mathrm{B}^{1.5}} \tag{2.4}$$

However, the BHFFOM is just mentioned for completeness and not used for the comparison of different semiconductor materials since it takes the operational condition of the device into account which leads to an unfair comparison. A comparison of the well established semiconductors by means of the three discussed figures of merit is summarized in table 2.3. It can be seen that

Figure of Merit	**Si**	**$Si_{0.7}Ge_{0.3}$**	**GaAs**	**4H-SiC**	**GaN**
JFOM	1.0	1.0	1.5	12.1	9.5
KFOM	1.0	0.5	0.6	3.2	1.2
BFOM	1.0	0.1	14.5	13.9	16.5

Table 2.3: Comparison of different bulk semiconductor materials by figures of merit normalized to Silicon.

GaN is by a factor of 9.5 better suited for high power high frequency application compared to Si according to JFOM. Furthermore, KFOM says that from a thermal point of view GaN is by a factor of 1.2 slightly better than Si. But one has to notice that this is just true for homogeneous GaN material. In real applications GaN is mostly grown on 4H-SiC, as already mentioned, which further enhances the thermal management as one would also expect from KFOM of 4H-SiC which is higher by a factor of 3.2 compared to Si. In terms of conduction losses BFOM indicates that GaN is by a factor of 16.5 better suited compared to Si. Overall, it can be seen that GaN is strongly dominating all well established semiconductors in RF and microwave applications. The only semiconductor which seems to be better suited than GaN for high power operation seems to be 4H-SiC with a JFOM = 12.1. However, this is only because of the higher electric breakdown field strength E_B of SiC compared to GaN. Thus, the better high power operation capability of SiC compared to GaN is only true for moderate operation frequencies due to the lower carrier mobility and drift saturation velocity.

2.3 Properties of AlGaN/GaN Heterostructures

The origin of high polarization in GaN was already introduced in section 2.1. This property of all group-III-nitrides is the most important one which is exploited in the utilization of GaN-based heterostructures. The basis for the realization of heterostructures, however, is the ability of band gap engineering which is provided in GaN by the formation of GaN alloys with Aluminum or Indium. Although ternary alloys with In, like AlInN and InGaN are currently under research and partly already in the industrialization phase, in this work we will only focus on the AlN/GaN material system and its ternary alloys. Figure 2.3 shows a map of band gap versus the respective lattice constant of all group-III-nitrides. For the AlN/GaN material system the band gap can be varied over almost 3 eV. However, it turns out that AlGaN alloys are never lattice matched to GaN resulting in a pseudomorphic strain in AlGaN layers grown on GaN. This strain induces a piezoelectric polarization on top of the spontaneous polarization in the layer. The dependence of

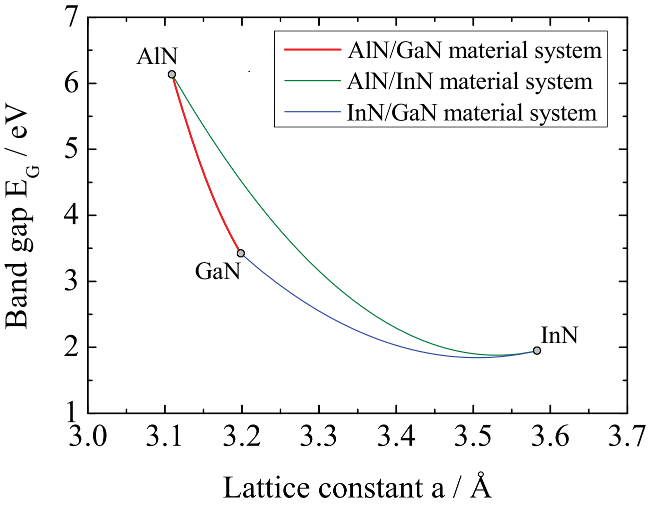


Figure 2.3: Relation between band gap and lattice constant of group-III-nitrides and their ternary alloys.

the polarization charge in an AlGaN layer on the Aluminum fraction x_{Al} is depicted in Fig. 2.4. In heterostructures formed by AlGaN and GaN this high polarization is exploited to form HEMT structures with remarkably high sheet carrier densities without utilizing any kind of doping. This sheet charge is a result of the polarization charge distribution in AlGaN/GaN heterostructures which is schematically depicted in Fig. 2.5. According to Dingle et al. [42] the electron mobility enhancement in GaAs-based HEMTs is due to the separation of free electrons from their parent donors, however, since AlGaN/GaN heterostructures also work without any applied doping but show still mobility improvement compared to the bulk semiconductor, today it is known that also the separation from unintentionally incorporated dopants and defects yield a mobility enhancement. Furthermore, according to Mimura et al. [1] as well as Delagebeaudeuf et al. [2] the operation principle of a HEMT device is mainly based on the control of confined electrons at the heterostructure interface. The net charge at the AlGaN/GaN hetero-interface leads to a confinement of free electrons provided by states at the surface of the epitaxy [43] in the formed quantum well. These confined electrons act as a 2-dimensional electron gas (2DEG). Since all characteristics of a HEMT structure are fulfilled for AlGaN/GaN heterostructures, devices based on such epitaxial structures will be called AlGaN/GaN HEMTs as it is also commonly accepted. A schematic viewgraph of the band diagram of a Schottky diode using an AlGaN/GaN heterostructure is depicted in Fig. 2.6. Since the polarization of AlGaN depends on the Aluminum fraction, the net polarization charge and therefore the sheet carrier density n_{S} can be varied by varying

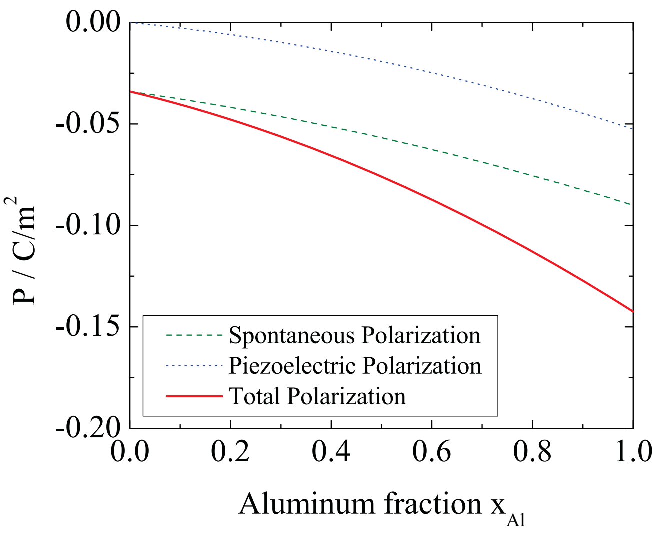


Figure 2.4: Polarization charge in an AlGaN layers [41].

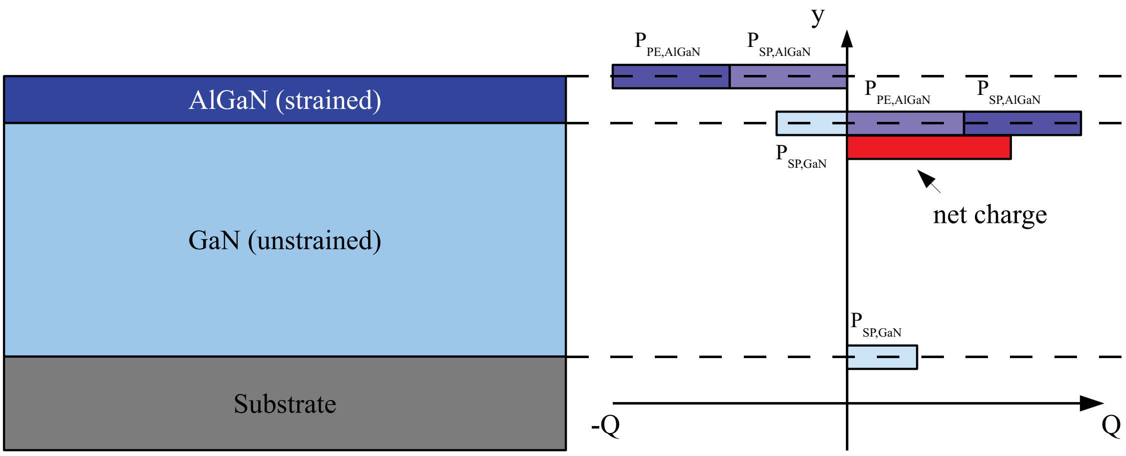


Figure 2.5: Polarization charge distribution in an AlGaN/GaN heterostructure.

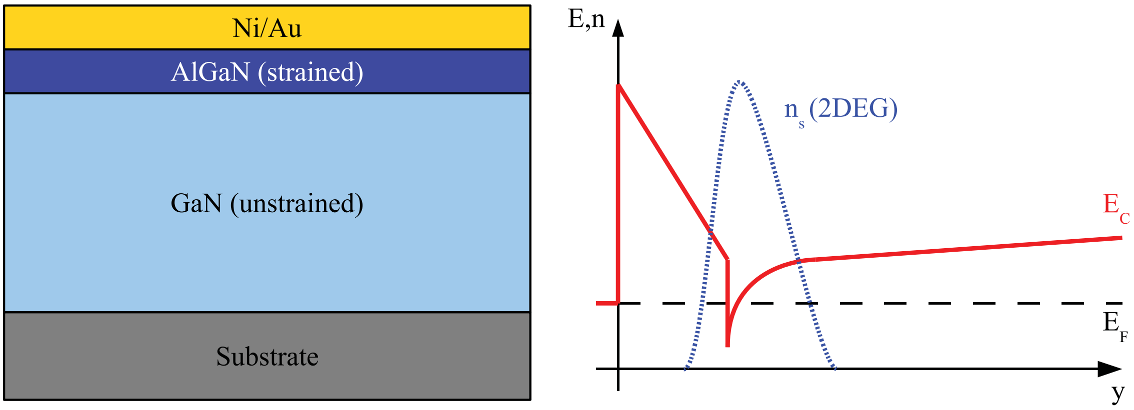


Figure 2.6: Cross section and band diagram of an AlGaN/GaN Schottky contact.

the Aluminum fraction in the AlGaN layer of a AlGaN/GaN heterostructure. On the other hand, the n_S is also dependent on the layer thickness of the AlGaN layers. However, in layers with a thickness $>$ 15 nm the sheet carrier density becomes almost independent of the layer thickness. The effect of Aluminum fraction and layer thickness on n_S was studied by Ambacher et al. [41] and is depicted for an AlGaN layer thickness above 15 nm in Fig. 2.7.

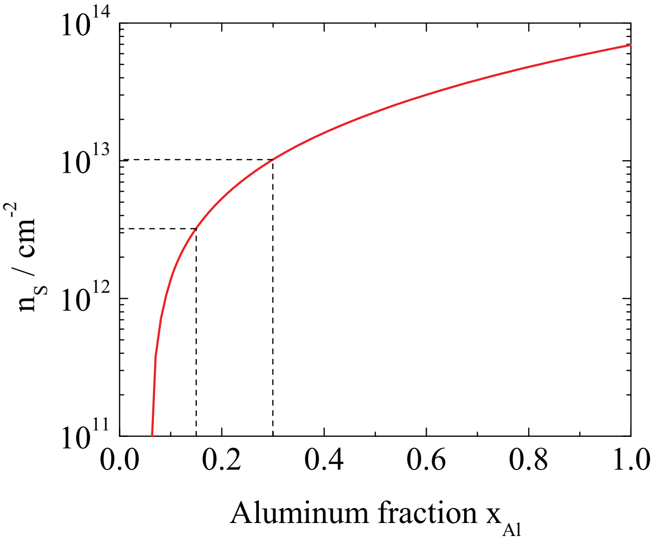


Figure 2.7: Dependence of n_S on the Aluminum fraction for an AlGaN layer thickness $> 15\,\text{nm}$ [41].

Chapter 3

Basic Physics and Modelling of AlGaN/GaN HEMTs

In this chapter, the operation principle of AlGaN/GaN HEMTs shall be explained. First, some basic current-voltage calculations on the ideal device operation will assist in understanding how non-ideal effects impact device behavior. Based on this, a physical modelling approach will be elaborated using the commercial TCAD tool Silvaco ATLAS [44]. For this, it is necessary to have a physical model which combines electrical and thermal models linked to each other. In the end, three different models will be developed capable to determine the on-state DC and thermal characteristics (electro-thermal model), the sub-threshold behavior (sub-threshold model) and the small-signal RF characteristics (small-signal RF model).

3.1 Fundamental Current-Voltage Characteristics

At first glance, an AlGaN/GaN HEMT is nothing but a classical HEMT using a pseudomorphic HEMT structure formed by AlGaN and GaN. This HEMT structure forms a channel at the AlGaN/GaN hetero-interface in a triangular-shaped quantum well in which the electrons are confined acting as a 2DEG. This confinement of the electrons leads to an improvement of the carrier mobility from $\mu_\mathrm{n} = 1000\,\frac{\mathrm{cm}^2}{\mathrm{Vs}}$ in bulk GaN (cf. table 2.2) up to $\mu_\mathrm{n} = 1500\ldots1700\,\frac{\mathrm{cm}^2}{\mathrm{Vs}}$ for state-of-the-art AlGaN/GaN heterostructures due to a reduction of scattering. This is achieved by the separation of mobile charge carriers from defects or traps.

3.1.1 Pinch-off Voltage

The first parameter to be calculated is the pinch-off voltage V_p and its dependence on the epitaxy configuration. The pinch-off voltage V_p of an ideal classical HEMT is given by equation (3.1)

$$V_\mathrm{p} = \frac{\phi_\mathrm{b} - \Delta E_\mathrm{C}(x_\mathrm{Al})}{q} - \frac{q \cdot N_\mathrm{D} \cdot d_\mathrm{d}^2}{2\varepsilon} \tag{3.1}$$

with the Schottky barrier hight ϕ_b, the conduction band discontinuity ΔE_C, the doping concentration N_D in the barrier layer and its doped layer thickness d_d [45]. However, in GaN-based devices the main part of the free electrons is induced by the polarization rather than any applied doping. Therefore, the expression for the pinch-off voltage V_p must be extended by the polarization induced sheet charge density [46]. The full expression for V_p is given in equation (3.2).

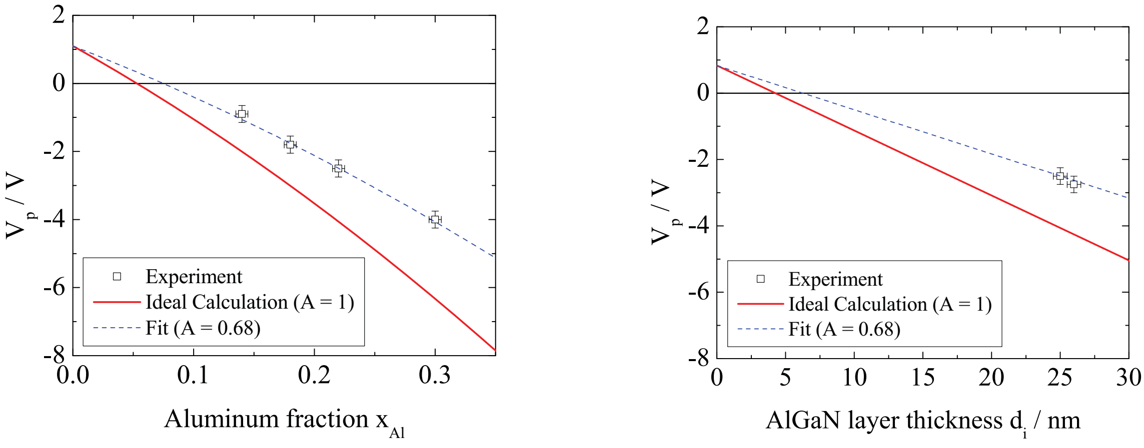
$$V_\mathrm{p} = \overbrace{\frac{\phi_\mathrm{b} - \Delta E_\mathrm{C}(x_\mathrm{Al})}{q} - \frac{q \cdot N_\mathrm{D} \cdot d_\mathrm{d}^2}{2\varepsilon}}^{\text{classical HEMT expression}} - \underbrace{\frac{A \cdot \sigma(x_\mathrm{Al})}{\varepsilon} \cdot (d_\mathrm{d} + d_\mathrm{i})}_{\text{polarization induced sheet charge}} \tag{3.2}$$

Here σ is the polarization induced sheet charge density, d_i is the thickness of the intrinsic part of the barrier layer and A is an empirical scaling factor which will be explained later on in this section. In this expression, there are three parameters which depend on the epitaxy. These are the total Schottky barrier layer thickness $(d_\mathrm{d} + d_\mathrm{i})$, the conduction band discontinuity ΔE_C and the polarization induced sheet charge density σ. ΔE_C and σ are both dependent on the Aluminum concentration x_Al in the AlGaN layer. The empirical expressions for ΔE_C and σ for AlGaN/GaN heterostructures are derived from [41] and given in equations (3.3) and (3.4).

$$\Delta E_\mathrm{C}(x_\mathrm{Al}) = 0.63 \cdot x_\mathrm{Al}^2 + 1.0773 \cdot x_\mathrm{Al} \qquad [\mathrm{eV}] \tag{3.3}$$

$$\sigma(x_\mathrm{Al}) = 0.0492 \cdot x_\mathrm{Al}^2 + 0.0593 \cdot x_\mathrm{Al} \qquad \left[\frac{\mathrm{C}}{\mathrm{m}^2}\right] \tag{3.4}$$

The dependence of the pinch-off voltage on the Aluminum fraction is plotted in Fig. 3.1(a) for a barrier layer thickness of 25 nm. In Fig. 3.1(b) V_p is plotted versus the barrier layer thickness for an Aluminum fraction of $x_\mathrm{Al} = 0.22$. Both plots show the ideal calculation directly from the derived equations. However, when comparing the calculated with experimental values of V_p from fully processed devices with a gate length of $L_\mathrm{G} = 500\,\mathrm{nm}$ it turns out that the ideal calculation overestimates the value for V_p. If then the empirical scaling factor A for the polarization induced sheet charge density is used to fit the calculation in both cases to experimental data, we get



(a) Pinch-off voltage versus Aluminum fraction for an 25 nm thick undoped Schottky barrier layer.

(b) Pinch-off voltage versus barrier layer thickness for an Aluminum fraction of 0.22 in the undoped Schottky barrier layer.

Figure 3.1: Pinch-off voltage dependence on epitaxy configuration.

consistently the same value of $A = 0.68$. This shows that there is a systematic discrepancy between measurement and calculation. This discrepancy can be explained by the presence of Iron (Fe) doping in the buffer for improvement of the buffer isolation which leads to a reduction of n_S impacting the pinch-off voltage of a device. Another reason which might contribute to part of the deviation is the fact that for practical reasons the pinch-off voltage in a real device was defined as the gate voltage at a drain current density of $I_D = 1\,\mathrm{mA/mm}$. Bringing now both dependencies together with the scaling factor determined to be $A = 0.68$ results is a 3D plot for the pinch-off voltage V_p as depicted in Fig. 3.2. The basis of all calculation was the assumption of a Nickel (Ni) based Schottky contact with a workfunction of 5.1 eV as also used in real devices. In combination with an AlGaN barrier layer this results in a Schottky barrier height of $\phi_b = 1.1\,\mathrm{eV}$. Another observation which can be made from plot 3.1 is that for both, the Aluminum fraction and the AlGaN layer thickness, there is a value where the device turns from a normally-on to a normally-off device. For the ideal calculation, these values are $x_{Al} = 0.053$ for the Aluminum fraction with a barrier layer thickness of 25 nm (cf. Fig. 3.1(a)) or $d_i = 4.25\,\mathrm{nm}$ for the barrier layer thickness with an Aluminum fraction of 0.22 (cf. Fig. 3.1(b)). However, in real devices both values cannot be realized since on the one hand, it turns out that there is no channel formed for Aluminum fractions $x_{Al} < 0.1$ and on the other hand, AlGaN layer thicknesses below $d_i < 15\,\mathrm{nm}$ are very hard to realize in reasonably good quality. This is one big reason why, especially for normally-off devices, InAlN/GaN heterostructures are currently under

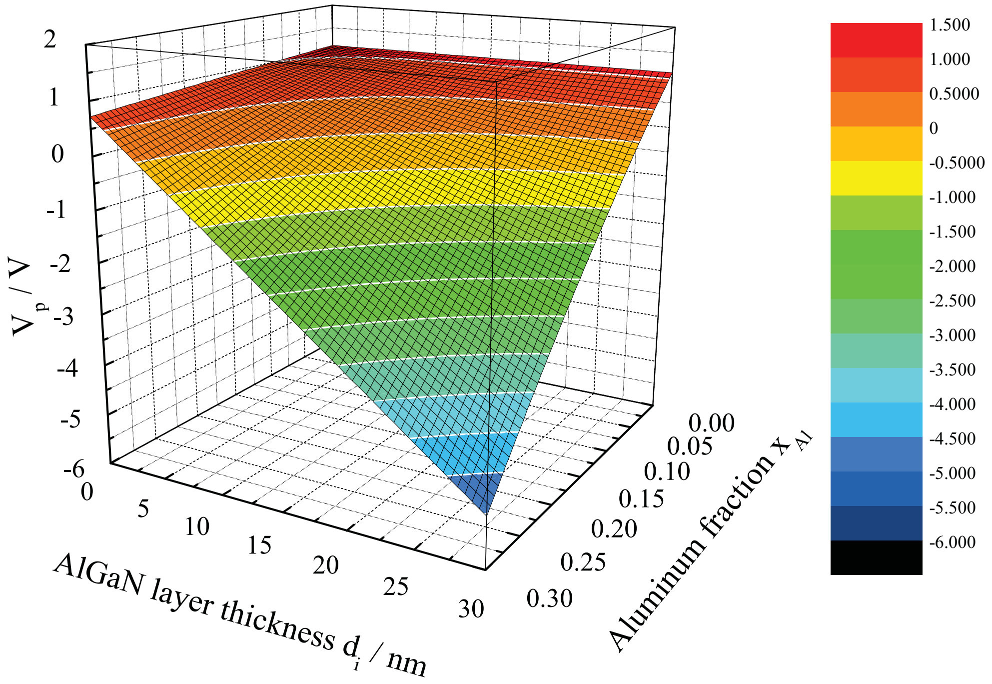


Figure 3.2: Pinch-off voltage dependence on barrier layer thickness and Aluminum fraction for an undoped epitaxy with experimental correction.

research and development in which very thin barrier layers of few nanometer thickness can be easily realized [47–49].

3.1.2 Drain Channel Current

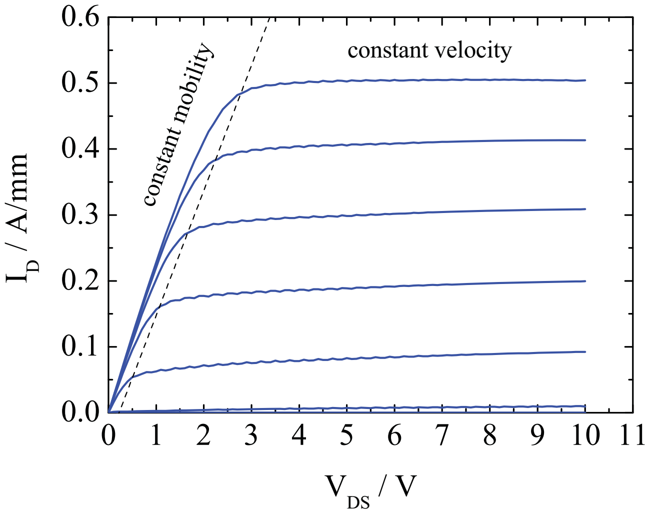
For the calculation of the I-V characteristics of an AlGaN/GaN HEMT we apply a two-region model. In the linear region of the output characteristic of a HEMT the condition for constant carrier mobility is fulfilled. In this region the device operates as a voltage-controlled resistor. For the condition of constant carrier velocity we need to operate the device in the saturation region of the output characteristics where the device acts as a voltage-controlled current source. The two regions are indicated in Fig. 3.3(a) and its relation to the carrier mobility in Fig. 3.3(b). For the condition of constant mobility, drain current can be expressed as shown in equation (3.5) [45]. This equation describes for $V_{\mathrm{DS}} << 2 \cdot \left(V_{\mathrm{GS}} - V_{\mathrm{p}}\right)$ a voltage-controlled resistor.

$$I_{\mathrm{D}} = \frac{\varepsilon_1 \mu_{\mathrm{n}} W_{\mathrm{G}}}{\left(d_{\mathrm{d}} + d_{\mathrm{i}} + \Delta d\right) L_{\mathrm{G}}} \cdot \left[\left(V_{\mathrm{GS}} - V_{\mathrm{p}}\right) V_{\mathrm{DS}} - \frac{V_{\mathrm{DS}}^2}{2}\right] \tag{3.5}$$

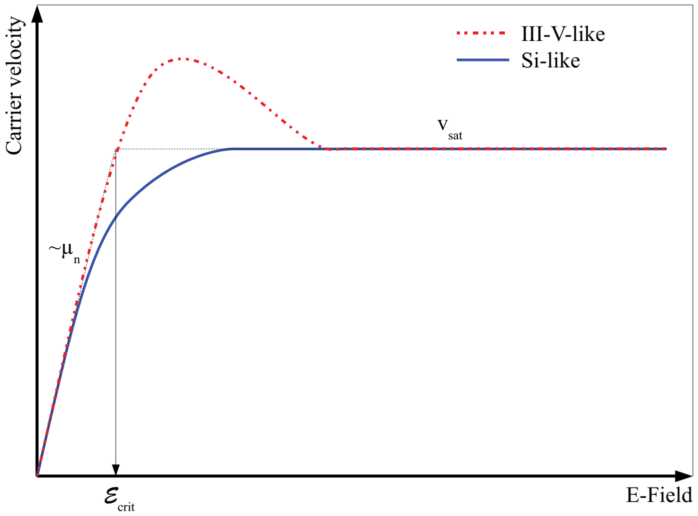
In this equation ε_1 is the dielectric constant of the AlGaN barrier layer below the Schottky contact and Δd is the *virtual increase of the Schottky barrier layer thickness* given by equation (3.6)

$$\Delta d = \frac{\varepsilon_2 a}{q} \tag{3.6}$$

with the dielectric constant ε_2 of the buffer layer and its material parameter a. This parameter is well known for GaAs with $a_{\mathrm{GaAs}} = 0.125 \cdot 10^{-12}\,\mathrm{Vcm}^2$. However, to calculate the drain current for a GaN-based HEMT, we need to know this material parameter a for GaN. To determine a_{GaN} we measure the on-state transfer characteristic of an AlGaN/GaN HEMT at $V_{\mathrm{DS}} << 2 \cdot \left(V_{\mathrm{GS}} - V_{\mathrm{p}}\right)$ an use equation (3.5) to calculate Δd in the linear region of the transfer characteristic. From this we can then derive a_{GaN} using equation (3.6). It is very important that for the determination of a_{GaN} the measurements are taken from a so called FATFET structure with very large gate length to make sure that the field below the gate is small enough to keep the charge carriers in the constant mobility region. Therefore, a FATFET structure with a gate length of $L_{\mathrm{G}} = 75\,\mu\mathrm{m}$ and a gate width of $W_{\mathrm{G}} = 130\,\mu\mathrm{m}$ was used. The layout of the device is depicted in Fig. 3.4(a). The transfer characteristics for several drain voltages $V_{\mathrm{DS}} << 2 \cdot \left(V_{\mathrm{GS}} - V_{\mathrm{p}}\right)$ was measured on this device. The measurement results are shown in Fig. 3.4(b). For the calculation the drain current must linearly follow the gate voltage. This condition is fulfilled in the measurement result in the range $V_{\mathrm{G}} = -2\,\mathrm{V} \ldots -1\,\mathrm{V}$. In this range we extract the virtual increase of the

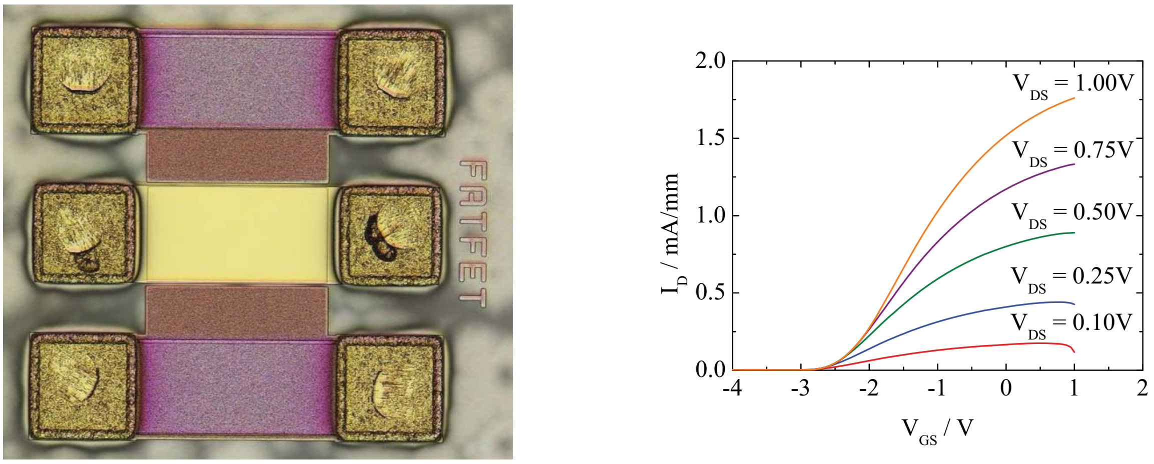


(a) Two-region model indicated in the output characteristic of an AlGaN/GaN HEMT.



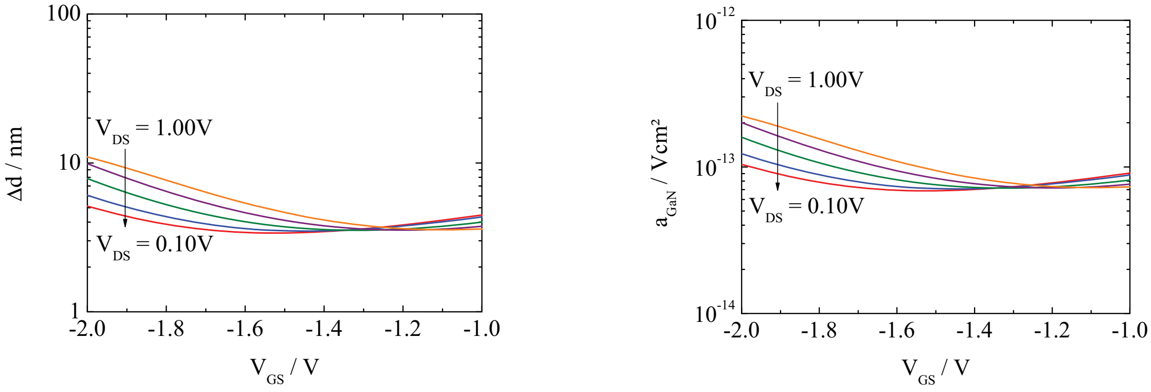
(b) Schematic velocity versus electric field plot of a Silicon-like and III-V-like relation.

Figure 3.3: Definition of low-field mobility and drift saturation region of electrons under transitor operation.



(a) FATFET structure used for the determination of a_{GaN}.

(b) Transfer characteristic for $V_{DS} << 2 \cdot \left(V_{GS} - V_p\right)$ measured on a FATFET.



(c) Δd extracted from experimental data.

(d) a_{GaN} extracted from experimental data.

Figure 3.4: Experimental results of measurements on a FATFET structure.

AlGaN barrier layer thickness Δd and we find the values plotted in Fig. 3.4(c). Interestingly, we find the parameter a_{GaN} to be dependent on the drain bias voltage. This is not unusual since the extraction of a_{GaN} itself is based on a model which relies on constant parameters and a perfect linear dependence of I_{DS} on V_{GS}. This assumption in reality is not necessarily true and is a simplification of the model as the transfer characteristics in Fig. 3.4 show. However, the best fit in the region around $V_{\mathrm{GS}} = -1\,\mathrm{V}$ where the transfer characteristics show a good linear dependence of I_{DS} on V_{GS} we determine $a_{\mathrm{GaN}} = 0.1 \cdot 10^{-12}\,\mathrm{Vcm}^2$. How the bias dependence of the parameter a_{GaN} is treated for further drain current calculations will be described in the following paragraph.
Now, we want to calculate the drain current in the region of constant velocity. In this region I_{D} is given by equation (3.7). This equation describes a voltage-controlled current source [45] with $V_0 = \mathscr{E}_{\mathrm{crit}} L_{\mathrm{G}}$.

$$I_{\mathrm{D}} = \frac{\varepsilon_1 \mu_{\mathrm{n}} W_{\mathrm{G}}}{(d_{\mathrm{d}} + d_{\mathrm{i}} + \Delta d)\, L_{\mathrm{G}}} \cdot V_0^2 \cdot \left[\sqrt{1 + \left(\frac{V_{\mathrm{GS}} - V_{\mathrm{p}}}{V_0} \right)^2} - 1 \right] \tag{3.7}$$

Under the assumption that the carrier velocity is a continuous function of the electric field, $\mathscr{E}_{\mathrm{crit}}$ is the electric field strength were the transition from constant mobility to drift saturation of the charge carriers occurs. This relation is schematically depicted in Fig. 3.3(b). With this definition of $\mathscr{E}_{\mathrm{crit}}$, a mobility of $\mu_{\mathrm{n}} = 1500\,\frac{\mathrm{cm}^2}{\mathrm{Vs}}$ and a drift saturation velocity of $v_{\mathrm{sat}} = 1.5 \cdot 10^7\,\frac{\mathrm{cm}}{\mathrm{s}}$ we end up with $\mathscr{E}_{\mathrm{crit}} = 10\,\mathrm{kVcm}^{-1}$. Knowing all these parameters, we now use equation (3.7) to fit experimental data measured on a $1\,\mathrm{x}\,100\,\mu\mathrm{m}$ device with $L_{\mathrm{G}} = 500\,\mathrm{nm}$. Due to this short gate length and the very high electric field below the gate associated with that, the charge carriers are also for low V_{DS} always in drift saturation. Measured transfer characteristics and calculated drain current are plotted on top of each other in Fig. 3.5 for different V_{DS}. When we compare experimental data with calculation we find for three different drain voltages a significant deviation. Using the range of parameter a_{GaN} which was determined experimentally in the paragraph before and the pinch-off voltage V_{p} as fitting parameters, we find a_{GaN} and V_{p} to be drain voltage dependent where a_{GaN} decreases and V_{p} increases with increasing V_{DS} in the constant velocity region as also shown in Fig. 3.5. The deviation between measurement and fitting for high V_{GS} is due to saturation effects, e.g. self-heating or limited control of the channel current due to too low V_{DS}, which are not taken into account in this theoretical calculation. The fitting parameters are summarized in table 3.1.

The most interesting goal of all these calculations in the end is to be able to calculate the dependence of the drain saturation current I_{DSS} on the Aluminum fraction and AlGaN barrier layer thickness. To do so, we take the parameters determined for $V_{\mathrm{DS}} = 7\,\mathrm{V}$, insert equation (3.2) into equation (3.7) and calculate the drain current at $V_{\mathrm{GS}} = 0\,\mathrm{V}$. This leads to the results plotted in

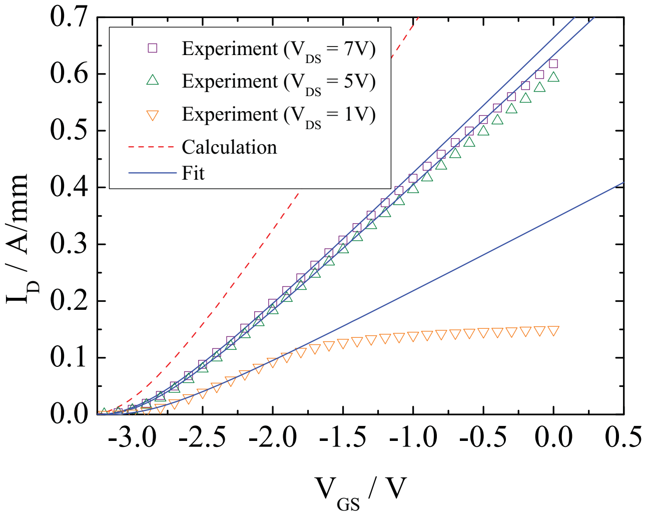


Figure 3.5: Experimental results and drain current calculation of a 1 x 100 μm AlGaN/GaN device.

Fitting Parameter	**V_{DS} = 1 V**	**V_{DS} = 5 V**	**V_{DS} = 7 V**
a_{GaN}	$1.30 \cdot 10^{-12}\,\mathrm{Vcm}^2$	$0.49 \cdot 10^{-12}\,\mathrm{Vcm}^2$	$0.45 \cdot 10^{-12}\,\mathrm{Vcm}^2$
V_{p}	3.16 V	3.22 V	3.24 V

Table 3.1: Fitting parameter for calculation of drain current.

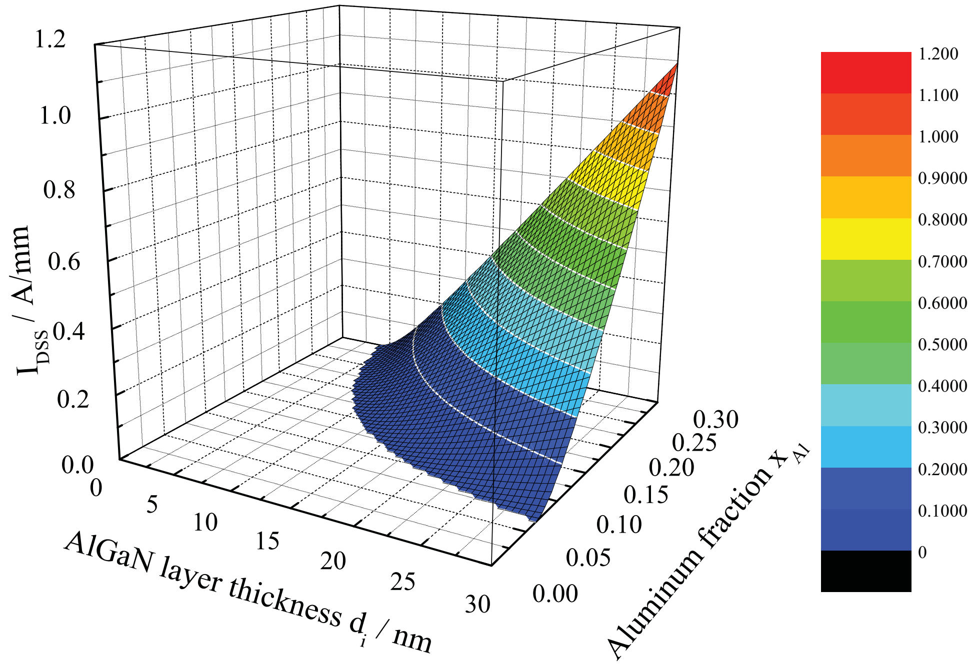


Figure 3.6: Drain saturation current dependence on barrier layer thickness and Aluminum fraction for an undoped epitaxy with experimental correction for a gate length of $L_G = 500\,\text{nm}$.

Fig. 3.6 for all $V_p < 0\,\text{V}$ which means normally-on mode.

3.2 Physical Device Modelling

3.2.1 Electro-Thermal DC Model

This electro-thermal model is based on the drift-diffusion transport equations for free charge carriers given in equations (3.8) and (3.9).

$$\vec{J}_\text{n} = qn\mu_\text{n}\vec{E}_\text{n} + qD_\text{n}\nabla n \tag{3.8}$$

$$\vec{J}_\text{p} = qp\mu_\text{p}\vec{E}_\text{p} - qD_\text{p}\nabla p \tag{3.9}$$

The mobility model used is a concentration and temperature dependent low-field mobility model based on the work of Farahmand et al. [50] in combination with a Silicon-like high-field mobility which does not consider the velocity overshoot commonly encountered in III-V materials. The low field mobility in GaN was adjusted to $\mu_\text{n} = 1500\,\frac{\text{cm}^2}{\text{Vs}}$ according to literature [31] and measurement data. The saturation velocity of electrons in GaN was set to $v_\text{sat} = 2.0 \cdot 10^7\,\frac{\text{cm}}{\text{s}}$ simply as a compromise between the theoretical value of $v_\text{sat} = 2.5 \cdot 10^7\,\frac{\text{cm}}{\text{s}}$ [31] and data from Monte-Carlo simulations [50,51] which claim a value of $v_\text{sat} = 1.5 \cdot 10^7\,\frac{\text{cm}}{\text{s}}$ in real state-of-the-art matter. The chosen value also leads to the best fit of the drain current to experiment as will be shown further down. Finally, for the recombination behavior of the carriers a concentration dependent model following the work of Shockley, Read and Hall [52,53] was applied. For more detailed information about these models, the author would like to refer to [54]. The crucial parts of the whole modeling approach, however, will be discussed in detail as follows.

Polarization

There are build-in models available within ATLAS to model the polarization in the device for a high number of materials, including GaN. However, using these models, which are mainly based on [41], leads to high computational effort and inflexibility and therefore bears the risk of convergence problems and bad fitting of the simulation to experimental data as we have already seen in subsection 3.1.1. To add an additional degree of freedom in modelling, the total polarization charge of each layer in the epitaxial layer sequence was calculated manually by the empirical formulas (3.10), (3.11) and (3.12) according to [41]. Associated with this methodology also the computational effort is reduced leading to a better convergence of the simulation. These formulas are given for the AlN/GaN material system.

$$P^\text{SP}_\text{AlGaN}(x_\text{Al}) = -0.090x_\text{Al} - 0.034(1-x_\text{Al}) + 0.021x_\text{Al}(1-x_\text{Al}) \qquad \left[\frac{\text{C}}{\text{m}^2}\right] \tag{3.10}$$

$$P^\text{PE}_\text{AlGaN/GaN}(x_\text{Al}) = -0.0525x_\text{Al} + 0.0282x_\text{Al}(1-x_\text{Al}) \qquad \left[\frac{\text{C}}{\text{m}^2}\right] \tag{3.11}$$

$$P_\text{AlGaN}(x_\text{Al}) = P^\text{SP}_\text{AlGaN}(x_\text{Al}) + P^\text{PE}_\text{AlGaN/GaN}(x_\text{Al}) \tag{3.12}$$

Using the resulting polarization charge, we calculate the corresponding sheet charge density Q at the interfaces of the layer resulting from equation (3.13).

$$Q_\text{AlGaN}(x_\text{Al}) = A \cdot \frac{P_\text{AlGaN}(x_\text{Al})}{q} \qquad \left[\frac{1}{\text{m}^2}\right] \tag{3.13}$$

Here q is the elementary charge and A an empirical scaling factor. Due to the orientation of the polarization the corresponding sheet charge at the top interface of the layer is considered to

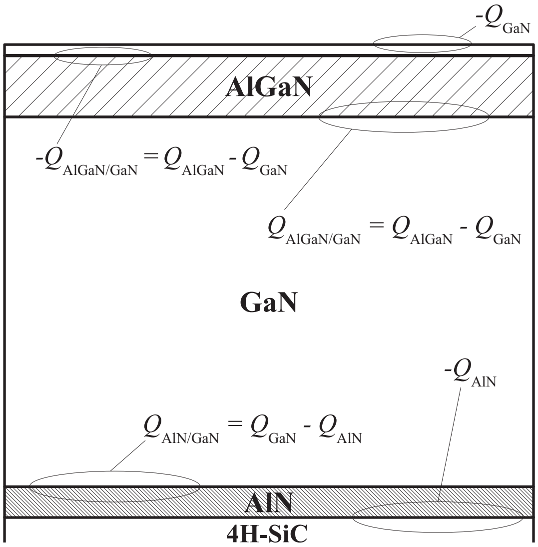


Figure 3.7: Fixed charges at the interfaces of all epitaxial layers are used to model the polarization.

be positive and at the bottom interface to be negative. When the corresponding interface sheet charge has been calculated, the difference in interface sheet charge of both layers is then placed at their interface using fixed charges as schematically depicted in Fig. 3.7. The calculation of the polarization induced sheet charge at the AlGaN/GaN hetero-interface at this point is equivalent to equation (3.4). Thus, the empirical scaling factor A in equation (3.13) is identical to that discussed before in subsection 3.1.1 and it turned out that the best fit to measurement data was achieved with $A = 0.75$ which was used in all performed simulations. Fixed charge means charge with a fixed polarity that cannot be changed in any case.

Surface States

The previous subsection already indicated that the interfaces between different layers in the device are the most critical locations and therefore need to be modeled very carefully.

All semiconductor surfaces have a high density of active surface states acting as donor-like traps with various energy levels and time constants originating from non-ideal atomic layers or dangling bonds at the surface. To control these active surface states, the devices are passivated with a dielectric layer like SiN in this case. The interface between this SiN layer and the semiconductor, however, is still not ideal and offers a certain amount of active donor-like states. The location of these donor-like surface states is indicated in Fig. 3.8. For clarity, a simplified structure was used in this drawing. The active surface states are modeled using donor-like interface traps with an

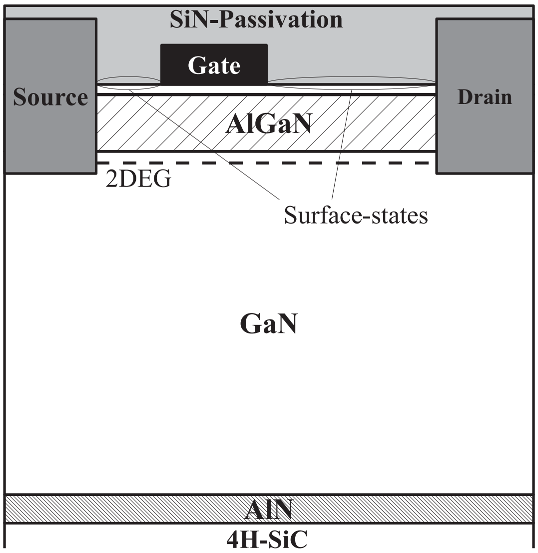


Figure 3.8: Interface traps are placed at the semiconductor/passivation interface to model the surface states.

energetic trap level of $E_C - E_T = 0.6\,\mathrm{eV}$ which is in agreement with [55,56]. The time constant τ_n of these traps varies in a wide range from 10^{-3} s to 10^{-6} s strongly dependent on the processing. However, these time constants are only of interest when performing transient DC simulations, which is beyond the scope of this quasi-static electro-thermal model and therefore not discussed here. The density of active surface traps n_{st} has a strong impact on n_s and the electric field distribution. DLTS measurements [57] for example on passivated epitaxial structures but also the work from various other groups [58,59] indicate that the density of the active surface trap density is in the order of magnitude of $10^{12}\,\mathrm{cm}^{-2}$, which is used as a starting value.

Self-Heating

To model the self-heating effect in the device, two models are used. One models the heating of the lattice and the other one takes heating and cooling effects by generation and recombination processes into account. The main material parameter one needs to know is the thermal conductivity σ_{th} for all materials in the epitaxial layer sequence. Especially, an accurate value of σ_{th} for the 4H-SiC substrate is important, as this layer forms the major part of the whole layer structure. The thermal dependence of σ_{th} for GaN, AlGaN, AlN and 4H-SiC was modeled according to [60]. Their temperature dependence is based on equation (3.14). As can be seen, the thermal

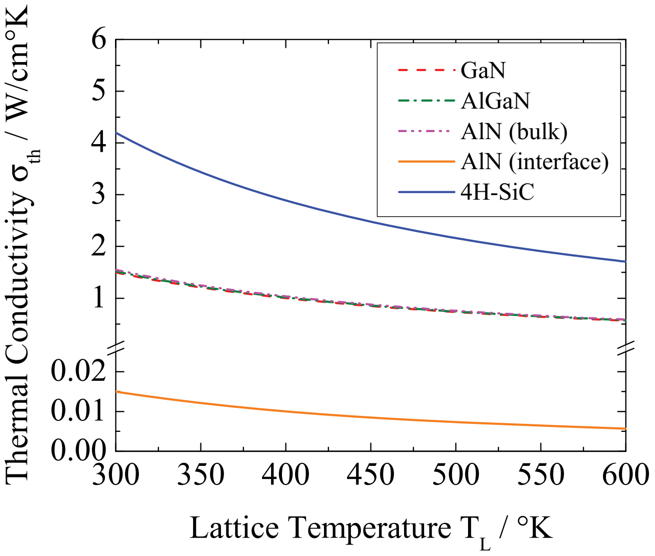


Figure 3.9: Temperature dependence of the thermal conductivity σ_{th} for all materials used.

conductivity of bulk GaN and AlN is nearly identical and so it is for their AlGaN alloys.

$$\sigma_{\mathrm{th}}\left(T_{\mathrm{L}}\right) = \sigma_{\mathrm{th},0} \cdot \left(\frac{T_{\mathrm{L}}}{300\,\mathrm{K}}\right)^{-\eta} \tag{3.14}$$

To model the non-ideal thermal behavior of the interface between AlN and GaN, which can lead to a contribution of 30 % to the thermal resistance of an AlGaN/GaN device [60,61] due to a reflection of phonons back into the GaN buffer layer, we decreased the thermal conductivity of the whole AlN nucleation layer by a factor of 100. This is reasonable because the layer thickness is of the order of nanometers. In Fig. 3.9 the thermal conductivity σ_{th} is plotted versus lattice temperature for all used materials. To get a reasonable temperature profile in the device, the boundary conditions need to be set properly. In order to simulate the operation under on-wafer conditions, a heat sink is placed over the whole substrate area of the structure. According to [60,62], under on-wafer operation only 10 μm of the 4H-SiC substrate below the AlN nucleation layer are affected by a significant temperature rise. Therefore, the heat sink in the simulation is placed in a way that this condition is fulfilled.

(a) Layout of a 1 x 100 μm device. (b) Layout of a 2 x 43 μm device.

Figure 3.10: Structures used for model verification.

Material	**Parameter**					
	E_G	μ_n	v_{sat}	$\sigma_{th,0}$	η	ε_r
$Al_{0.26}Ga_{0.74}N$	3.89 eV	285 cm^2/Vs	$1.12 \cdot 10^7$ m/s	1.52 W/cmK	1.4	8.8
GaN	3.43 eV	1500 cm^2/Vs	$2.0 \cdot 10^7$ m/s	1.5 W/cmK	1.4	8.9
AlN	6.14 eV	680 cm^2/Vs	$2.17 \cdot 10^7$ m/s	0.015 W/cmK	1.4	8.5
4H-SiC	3.26 eV	460 cm^2/Vs	$2.2 \cdot 10^7$ m/s	4.2 W/cmK	1.3	9.7

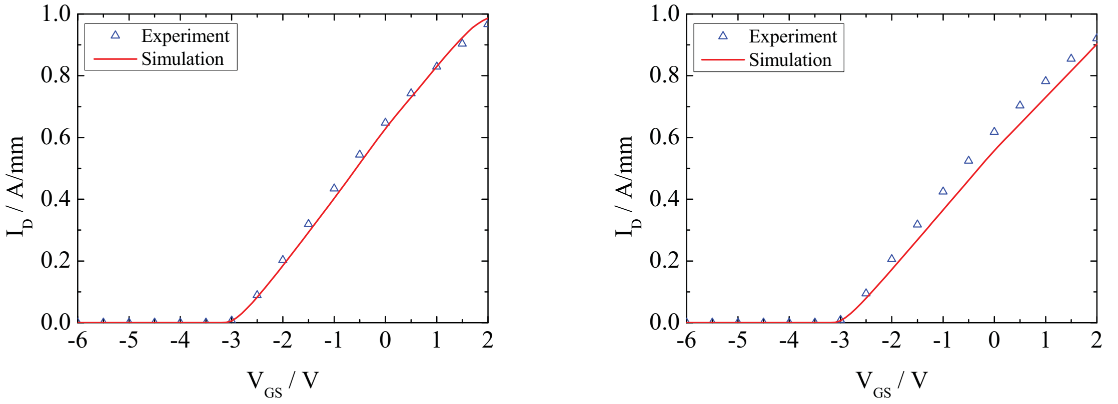
Table 3.2: Material parameters used for simulation to verify the electro-thermal model.

Electro-Thermal DC Model Verification

For the verification of the developed electro-thermal model a 1 x 100 μm device was characterized by DC measurements and a 2 x 43 μm device was characterized by micro-Raman thermography. The layout of the structures is depicted in fig 3.10. The characterized AlGaN/GaN HEMTs were fabricated by MOCVD on SiC substrate. The simulation structure was designed using the layout and epitaxial layer parameters from the fabricated devices. In this case the epitaxy utilized a AlGaN Schottky layer with an Aluminum mole fraction of $x = 0.26$. All electrical and thermal material parameters used for this model verification are summarized in table 3.2. The layout parameter of the characterized devices will be described in the respective section as they vary depending on the characterization technique.

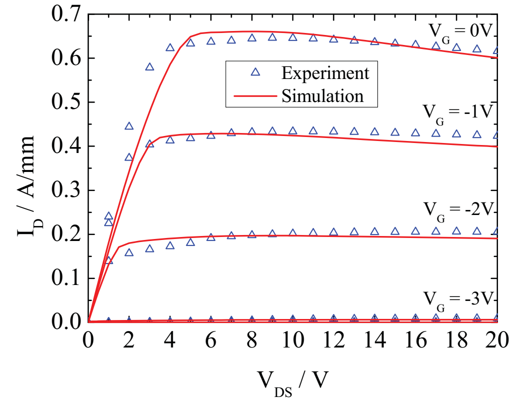
DC Characterization was performed using a Hewlett-Packard HP 4145B semiconductor parameter analyzer and tungsten needles for probing. The output characteristics and the transfer characteristics for several drain voltages V_{DS} were measured and compared to the simulation results. After adjusting the polarization interface charges mainly with respect to the threshold voltage V_{th} and adjusting n_{st} with respect to I_{DSS} and the transconductance g_{m}, we ended up with a donor-like $n_{\mathrm{st}} = 3.25 \cdot 10^{12}\,\mathrm{cm}^{-2}$ and a sheet charge density in the channel of $n_{\mathrm{s}} = 6.15 \cdot 10^{12}\,\mathrm{cm}^{-2}$ which is in good agreement with Hall measurements. Fig. 3.11 shows the good agreement between simulation and measurement of the transfer characteristics at $V_{\mathrm{DS}} = 10\,\mathrm{V}$ and $V_{\mathrm{DS}} = 20\,\mathrm{V}$ reached with the given parameters. Also the simulated linear region and the knee-voltage of the output characteristics are in good agreement with experimental data as depicted in Fig. 3.11(c). It can be seen in the graphs especially at higher drain voltages that the impact of temperature on the current density is slightly overestimated by the model.

Micro-Raman Thermography measurements have been performed on AlGaN/GaN devices with $L_{\mathrm{G}} = 500\,\mathrm{nm}$ using a Renishaw InVia micro-Raman system with the 488-nm-line of an Ar laser as excitation source. The laser was focused to a spot size of $0.5 - 0.7\,\mu\mathrm{m}$ on the device surface. Since the area of the spot size corresponds to the integration area of the Raman signal, the spot size gives also the spacial resolution of the measurements. The device temperatures were extracted from the difference between the GaN E_2(high) and A_1(Longitudinal optical) phonon frequency for various dissipated power densities of the device by varying the drain current density at a given drain voltage. For a more detailed description of the micro-Raman thermography method the author would like to refer to [63–65]. The overall measurement accuracy of the setup has been determined to be better than $\pm 5\,^{\circ}\mathrm{C}$. As already mentioned, the Raman signal is integrated over the whole area of the laser spot and the whole depth the laser is penetrating into the device under test. Therefore, the measured temperature typically corresponds to the temperature in the center point of the GaN layer. For better comparison of the experimental results with simulations in addition the SiC substrate temperatures were also determined by shifting the focal plane of the laser spot from the surface down into the SiC substrate exploiting the transparency of the material for this wave length of the laser. A simulated 2-dimensional temperature profile under operation at a dissipated power density of $P_{\mathrm{diss}} = 11.8\,\mathrm{W/mm}$ at $V_{\mathrm{DS}} = 50\,\mathrm{V}$ is depicted in Fig. 3.12(a) using the parameters from table 3.2. The measurements were taken at $V_{\mathrm{DS}} = 50\,\mathrm{V}$ and the dissipated power density was varied along the respective transfer characteristic by varying the gate voltage. A comparison between measured and simulated GaN and SiC temperatures versus dissipated power density is plotted in Fig. 3.12(b). The prediction of the SiC temper-



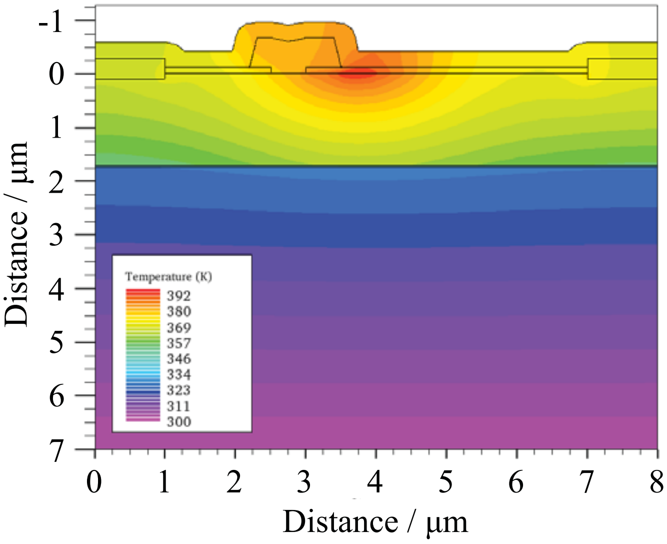
(a) Simulated and measured drain current at $V_{DS} = 10\,V$.

(b) Simulated and measured drain current at $V_{DS} = 20\,V$.

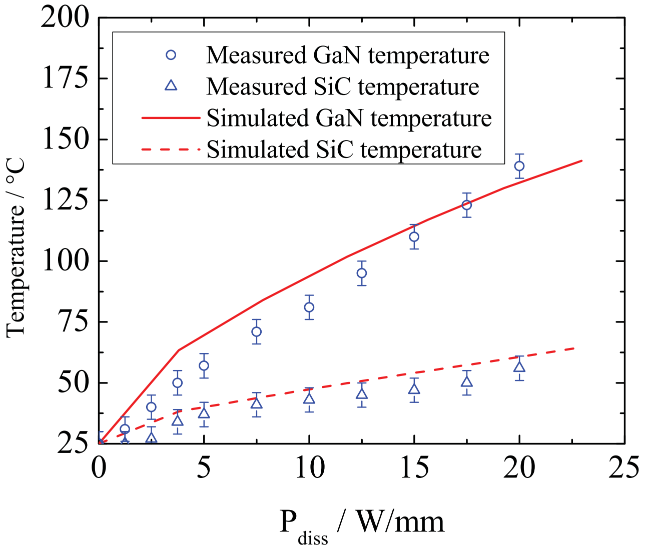


(c) Simulated and measured output characteristics.

Figure 3.11: Comparison of simulated and measured DC characteristics of a 1 x 100 μm device.



(a) Simulated temperature profile for a dissipated power density of $P_{\text{diss}} = 11.8\,\text{W/mm}$ at $V_{\text{DS}} = 50\,\text{V}$.



(b) Comparison of simulated and measured device temperatures versus dissipated power.

Figure 3.12: Electro-thermal simulation results.

ature is very good whereas the deviation between measured and simulated GaN temperature is larger but still within reasonable values. The deviation is a results of the point of data extraction in the device. As already mentioned the Raman temperature is averaged through the GaN layer thickness and corresponds therefore nearly to the temperature in the middle of the GaN buffer layer. However, since this assumption is not very accurate, the discrepancy obtained when comparing the simulated temperature in the middle of the GaN layer with measured Raman temperatures is acceptable since the local temperature resolution of the simulation is far higher than the measurement. Thus, the calibration of the electro-thermal model is very good.

3.2.2 Sub-Threshold DC Model

The sub-threshold DC model describes the device operation at gate voltages $V_{\mathrm{GS}} < V_{\mathrm{p}}$. It is the operation regime where leakage currents become dominating. In this subsection, it is assumed that the physical mechanism of these leakage currents is thermionic Schottky tunneling. It is a combination of a simple Schottky tunneling mechanism and thermionic emission. The assumption was made as it best reproduces experimental effects discussed further down in section 4.2. The electro-thermal model, already introduced, provides the foundation for this model. It is modified in the way that models for self-heating are switched off to increase convergence of the simulation and the model for thermionic Schottky tunneling based on [66,67] is added. It is described mathematically by equation (3.15) [54].

$$J_{\mathrm{T}} = \frac{A^{*}T_{\mathrm{L}}}{k} \int_{E}^{\infty} \Gamma(E)\, ln \left[\frac{1+f_{\mathrm{s}}(E)}{1+f_{\mathrm{m}}(E)} \right] dE \tag{3.15}$$

Here J_{T} is the tunneling current density, A^{*} the effective Richardson's coefficient, T_{L} the lattice temperature, $\Gamma(E)$ is the tunneling probability, f_{s} and f_{m} are the Maxwell-Boltzmann distribution functions in the semiconductor and metal of the Schottky contact and E is the carrier energy. Associated with the tunneling current density we get the localized tunneling rate G_{T} in equation (3.16).

$$G_{\mathrm{T}} = \frac{1}{q} \cdot \nabla J_{\mathrm{T}} \tag{3.16}$$

The thermionic tunneling model is schematically depicted in Fig. 3.13. What we get is a tunneling current density which depends on the local electric field, the lattice temperature and finally the shape of the band diagram of the Schottky contact. In Fig. 3.14 some simulation results are shown. A detailed comparison to measurement data will not be done since it turns out that each

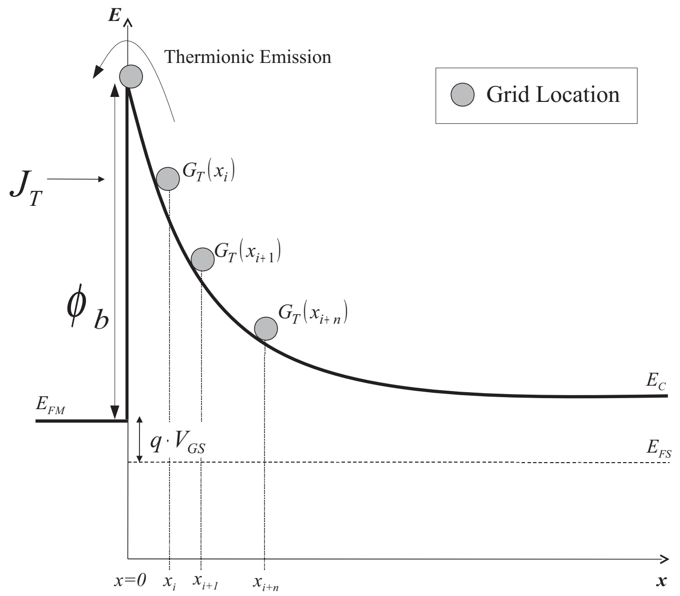


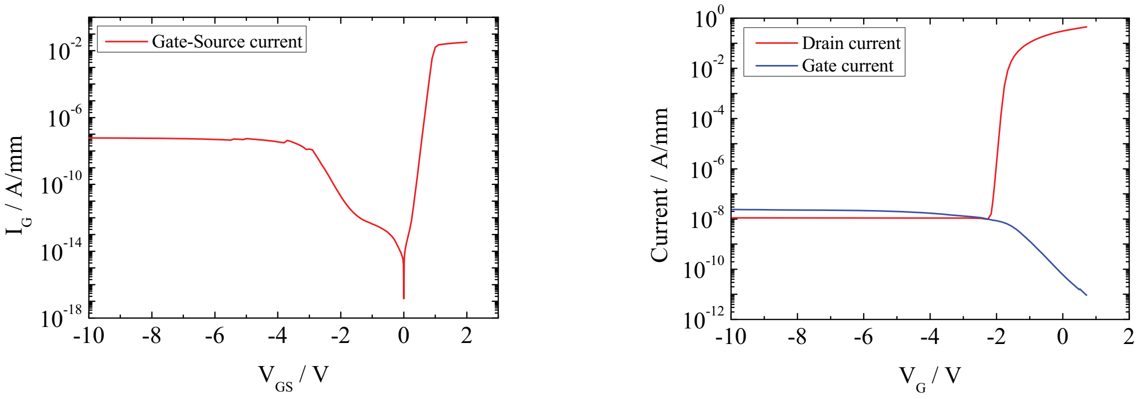
Figure 3.13: Schematic concept of the thermionic tunneling model [54].

single process variation needs its own fitting due to different dominating effects as will become clear in section 4.2. Here the leakage was realized by introducing a donor-like trap density of $N_{\mathrm{DT}} = 1 \cdot 10^{17}\,\mathrm{cm}^{-3}$ below the Schottky contact.

3.2.3 Small-Signal RF Model

The RF model was also derived from the already developed electro-thermal model. The basic modelling philosophy is based upon the assumption that a good fit in the DC parameters results directly a good fit in RF parameters. This is not a trivial assumption since it hold just for ideal non-dispersive devices, but although GaN-based HEMTs are highly dispersive in this particular case it turns out to be valid. This is due to the fact that traps located in the bulk semiconductor material or at the surface are deep enough in their energy level, e.g. Fe with an trap energy level of $E_{\mathrm{C}} - E_{\mathrm{T}} = 1.7\,\mathrm{eV}$ or surface states with an $E_{\mathrm{C}} - E_{\mathrm{T}} = 0.6\,\mathrm{eV}$, to have no impact on the small-signal performance due to very long time constants related to the deep energy levels. This can also be seen in the load-pull data of a highly dispersive device shown later on in chapter 4 where the linear gain equivalent to the small-signal gain is not dependent on the dispersion.

In this small-signal model the self-heating is neglected since it is not expected to impact the RF parameters because of comparably long thermal time constants and furthermore leads an improved convergency of the simulations. However, this leads to a slight overestimation of the



(a) Simulated 2-terminal leakage current of the gate-source diode.

(b) Simulated 3-terminal leakage current at $V_{\mathrm{DS}} = 50\,\mathrm{V}$.

Figure 3.14: Simulation results using a thermionic tunneling model with an AlGaN/GaN device with $L_{\mathrm{G}} = 500\,\mathrm{nm}$.

DC drain current and therefore the RF gain. It is not useful to compare measured and simulated S-parameters in order to verify the RF model since the simulation tool allows only to simulate single-finger devices in a 2-dimensional manner. Real RF devices are multi-finger device in either coplanar or microstrip configuration. This leads to a strong dependence of the small-signal parameters shown in Fig. 3.15 on the device layout. Therefore, the current gain $|H_{21}|$ is used as a parameter for the model verification. This is useful since the current gain considers an ideal current source at the input and is defined at a short circuit at the output of the SSEC.

$$H_{21} = \frac{i_2}{i_1}|_{v_2=0} \tag{3.17}$$

This eliminates some of the layout and gate width dependent small-signal parameters, e.g. parasitic output pad capacitances, as depicted in Fig. 3.16. Since inductances and resistances from the embedding network are very small in III-V technologies due to the utilization of Gold for the metallization, the remaining output branch in Fig. 3.16 drastically reduces the effect of C_{ds} and R_{ds}. This leads in total to a better comparison of small devices with different layout in terms of current gain $|H_{21}|$. In Fig. 3.17 a comparison between the simulated and measured current gain up to 50 GHz is shown. One has to notice that the simulation considers just the intrinsic part plus part of the drain and source resistances R_{d} and R_{s} of the device since the ohmic contact resistance is taken into account. The measurement taken from a 2x50 μm device with $L_{\mathrm{G}} = 250\,\mathrm{nm}$, however, shows the embedded data including additional series inductances and resistances from

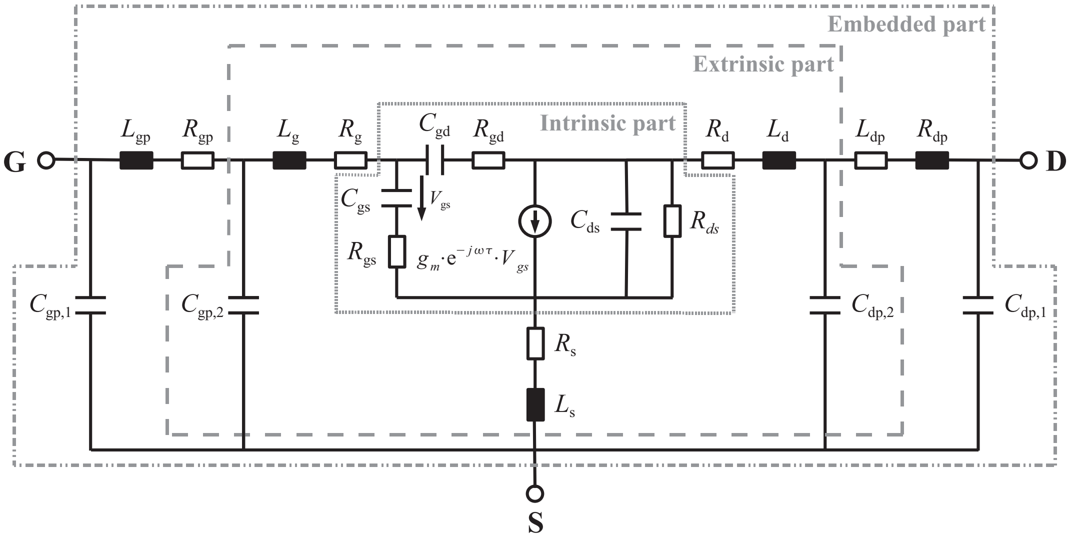


Figure 3.15: Small-signal equivalent circuit of a FET [68].

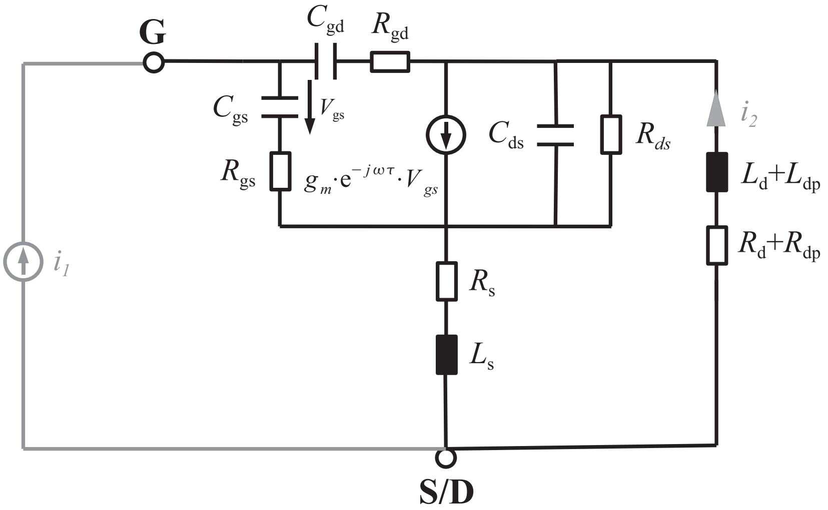


Figure 3.16: Small-signal equivalent circuit of a FET under current gain $|H_{21}|$ condition with short-circuited output.

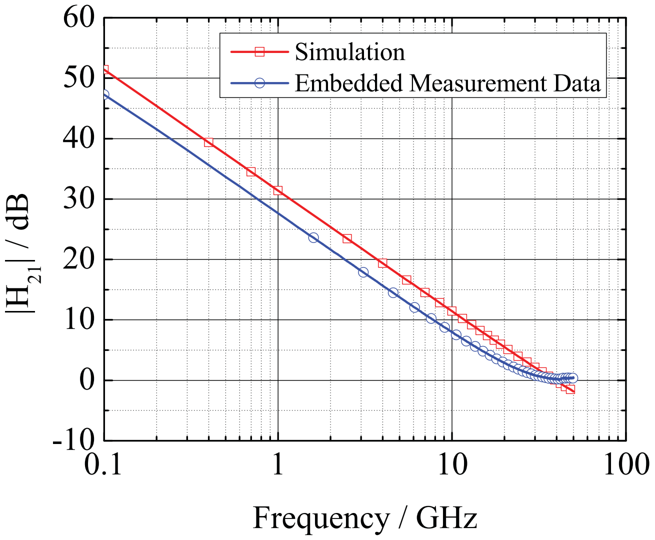


Figure 3.17: Comparison of the simulated and measured current gain for bias conditions at maximum g_m at $V_\mathrm{DS} = 30\,\mathrm{V}$.

the surrounding network which contribute according to Fig. 3.16. For more details about the extraction of the small-signal parameters the author would like to refer to [69].

Chapter 4

Impact of Non-Idealities on Device Performance

NON-IDEAL effects in AlGaN/GaN HEMTs are very striking since they are responsible for the limitation of the device performance in microwave applications. This chapter is dedicated to the discussion of three major effects in AlGaN/GaN HEMT and their root cause which will be investigated mainly by means of physical device simulations using the models discussed in the previous chapter.

4.1 Trapping Effects and Dispersion

In this section the so called current collapse will be discussed, which is a dispersion effect studied by various research groups using different techniques depending on the application. However, all electrical techniques such as transient DC measurements, pulsed I-V measurements or even advanced RF techniques using RF waveform engineering [70] just allow the investigation of the effect of dispersion rather than its root cause. In this work, we want to study dispersion and its effect on the performance of AlGaN/GaN devices using simple standard characterization techniques like low-frequency S-parameter measurements as well as two-tone measurements to study the effect of dispersion on linearity represented by the third-order intermodulation distance (IMD3). Using these results, the main root cause of dispersion in AlGaN/GaN devices will be discussed supported by device simulations.

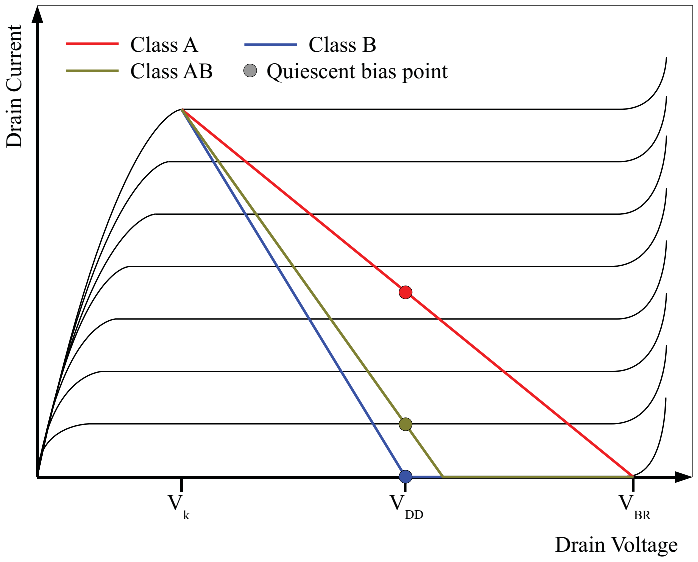


Figure 4.1: Schematic plot of the load-lines for operation classes A, AB and B.

4.1.1 Influence of Dispersion on RF Power Performance

To understand the influence of dispersion on the RF power performance it is necessary to discuss the large-signal operation of a HEMT device under RF operation. Therefore, we need to consider the applied load-line which is defined by the quiescent bias point and the output characteristics of the operating device. A schematic example for the construction to the load-line in the output characteristics is depicted in Fig. 4.1. It can be seen from this figure that the output power and, thus, the efficiency of a device is determined by the maximum voltage swing indicated by the respective load line limited by the supply voltage V_{DD}, the knee-voltage V_{k}, the maximum drain current I_{D} and the breakdown voltage V_{BR}. For class A operation, the maximum output power under linear operation can be calculated using these parameters as shown in equation (4.1) and the drain efficiency η_{D} and power added efficiency η_{PAE} is given in equations (4.2) and (4.3) which are related to each other via the RF gain G of the device.

$$P_{\mathrm{max,lin}} = \frac{1}{8} \cdot (V_{\mathrm{BR}} - V_{\mathrm{k}}) \cdot \left(I_{\mathrm{D,max}} - I_{\mathrm{D,min}}\right) \tag{4.1}$$

$$\eta_{\mathrm{D}} = \frac{P_{\mathrm{RF,out}}}{P_{\mathrm{DC}}} \tag{4.2}$$

$$\eta_{\mathrm{PAE}} = \frac{P_{\mathrm{RF,out}} - P_{\mathrm{RF,in}}}{P_{\mathrm{DC}}} = \left(1 - \frac{1}{G}\right) \cdot \eta_{\mathrm{D}} \tag{4.3}$$

Bias	**Reference**	**Cold Pinch-Off**	**Hot Pinch-Off**
V_{GSq}	$0\,\mathrm{V}$	$-7\,\mathrm{V}$	$-7\,\mathrm{V}$
V_{DSq}	$0\,\mathrm{V}$	$0\,\mathrm{V}$	$50\,\mathrm{V}$

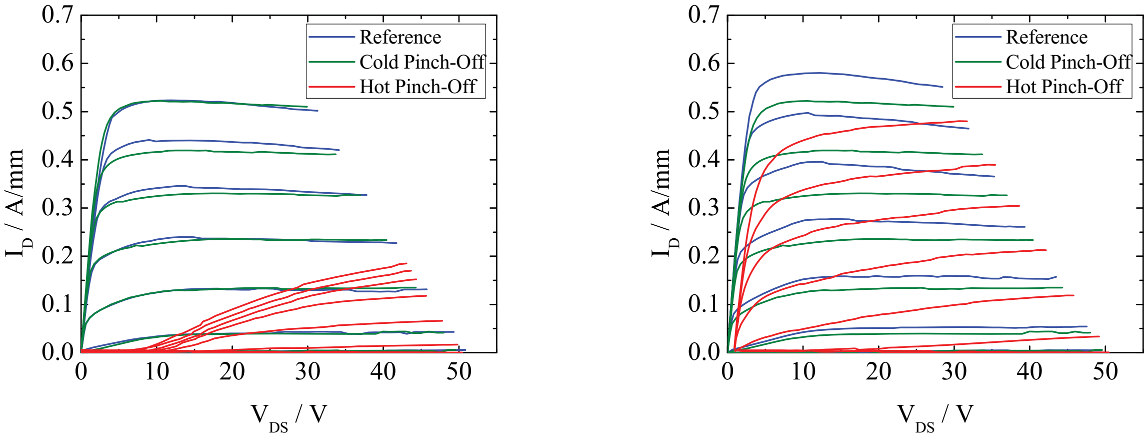
Table 4.1: Quiescent bias points of pulsed-IV measurements for the determination of current collapse.

To discuss the impact of dispersion on the RF power performance, we clearly need to define a parameter which quantifies the current collapse from pulsed-IV measurements. It should be noticed that a very common expression for that in the literature is *lagging*. However, using this expression for current collapse determined by pulsed-IV measurements is misleading since the early definition of drain and gate lagging was derived from transient current measurements and is therefore reserved for that. To avoid confusion, in this work we call the phenomena *drain-related current collapse* and *gate-related current collapse* and use the symbols CC_{D} and CC_{G}. The definition of CC is given in equation (4.4) at $V_{\mathrm{GS}} = +1\,\mathrm{V}$ and $V_{\mathrm{DS}} = 10\,\mathrm{V}$, which defines the power loss relative to the optimum operation due to the loss in drain current.

$$CC = \left| \frac{I_{\mathrm{D,ref}} - I_{\mathrm{D,dyn}}}{I_{\mathrm{D,ref}}} \right| \cdot 100\,\% \tag{4.4}$$

The distinction between drain-related and gate related current collapse is given by the quiescent bias point for the pulsed measurement of $I_{\mathrm{D,dyn}}$. These bias points for the three measured pulsed IV characteristics are summarized in Table 4.1. The quiescent bias point for the reference is called *Reference*, for the gate-related current collapse it is called *Cold Pinch-Off* and for the drain-related current collapse it is called *Hot Pinch-Off*. These quiescent bias points are the starting bias condition of each pulse applied during the measurement to drive the device in on-state.
In the cold pinch-off bias condition, the gate is biased with a gate-source voltage far below the pinch-off voltage (here $V_{\mathrm{GS}} = -7\,\mathrm{V}$) of the device under test and the drain as well as the source are at ground potential. This bias condition leads to charging effects close to the gate region of the device so that all effect associated with a current collapse during this measurement condition can be attributed to the gate area of the device.

The hot pinch-off bias condition extends the area affected by charging to the gate-drain region of the device. This is due to the high drain-source voltage applied (here $V_{\mathrm{DS}} = 50\,\mathrm{V}$) in addition to the gate-source voltage below pinch-off voltage as in the cold pinch-off condition. This fact allows to relate the current collapse obtained in this quiescent bias condition to effects in the gate-drain region taking the results from the cold pinch-off measurement into account. For



(a) Example of a device with strong drain-related current-collapse of $CC_D = 96.6\,\%$.

(b) Example of a device with reasonably weak drain-related current-collapse of $CC_D = 23.9\,\%$.

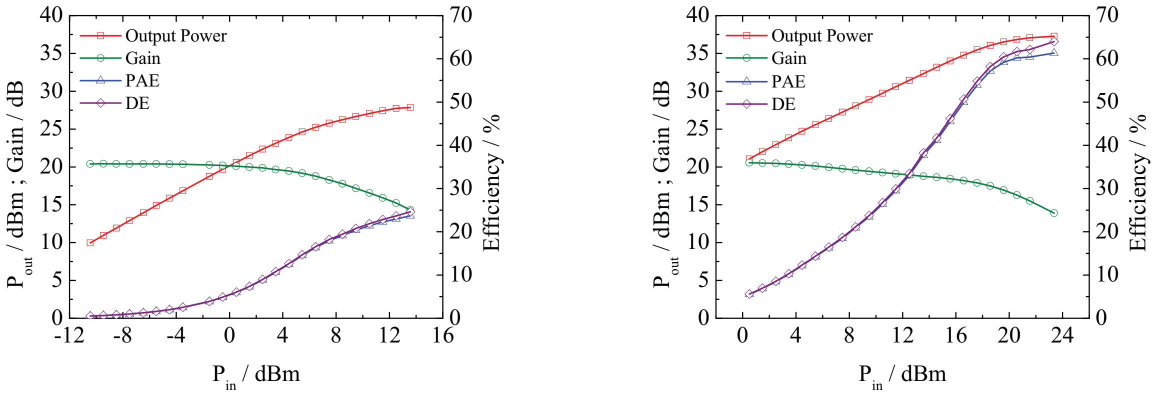
Figure 4.2: Pulsed IV measurements on devices with different passivation using a pulse width of $\tau_p = 1\,\mu$s and a duty cycle of $d_p = 0.001\,\%$.

the judgement of the RF power performance, CC_D is the main parameter of interest since it represents the real 3-terminal operation of the device and contains also the effect of gate-related current collapse. The main information gained from the gate-related current collapse is the estimation of the quantity of current collapse coming from the gate area. However, this is a valuable information for the technology development rather than for the RF circuit design in which the overall RF power performance is of interest.

If we now compare a device with very high drain-related current collapse depicted in Fig. 4.2(a) to a device with reasonably low drain-related current collapse, depicted in Fig. 4.2(b) we find the reduction in drain current and the strong increase of the knee-voltage causing the loss in RF power seen in Fig. 4.3 where the related load-pull data at $f = 2\,$GHz is shown. The reduced output power furthermore has direct impact on the efficiency of the device which is also drastically reduced.

4.1.2 Traps as the Root Cause of Dispersion

It is well known that traps are the root cause of current collapse [58,59]. The real challenge, however, is the localization of the region where dominant traps with respect to dispersion are located. For the localization of these traps, physical device simulations will be used in order to reproduce the current collapse. To this end, the electro-thermal model is used and acceptor-like



(a) Load-pull characteristics of a device with strong current-collapse of $CC_{\mathrm{D}} = 96.6\,\%$.

(b) Load-pull characteristics of a device with reasonably weak current-collapse of $CC_{\mathrm{D}} = 23.9\,\%$.

Figure 4.3: Load-pull measurements at $f = 2\,\mathrm{GHz}$ and a bias of $V_{\mathrm{DS}} = 50\,\mathrm{V}$ and $I_{\mathrm{D}} = 50\,\mathrm{mA/mm}$ on devices with different passivation.

traps are placed at the semiconductor-passivation interface. Finally, the static IV characteristics are calculated. As traps need to be charged to have an influence on the DC characteristics, it is very likely that traps located near the drain-side edge of the gate foot are responsible for the current collapse since we obtain the highest electric field in that region. Other driving effects for charging like externally applied or internally generated temperature or incident light are much lower level effects because of the deep trap energy level of these assumed acceptor-like traps of $E_{\mathrm{T}} - E_{\mathrm{V}} = 0.6\,\mathrm{eV}$. These traps act as a *virtual gate* and cause a depletion of the 2DEG in the gate-drain region. This results in an increase of the series resistance resulting in a reduction of the drain current. A simulated example of the virtual gate effect is depicted in Fig. 4.4. To quantify the density of traps n_{AT} and the gate length of the virtual gate $L_{\mathrm{G,virt}}$, a simulation study has been performed and one branch of the output characteristics has been simulated using different trap densities and different extensions of the affected region. The results of these simulations are plotted in Fig. 4.5. One can see that both parameters have a strong influence on the current collapse. It is quite hard especially for devices with high current collapse, cf. Fig. 4.2(a), to identify a single set of parameters in order to quantify the trap density and the related extension. However, for good current collapse behavior it turns out from the simulation study that for an epitaxy with an Aluminum fraction of $x_{\mathrm{Al}} = 0.18$ with a $n_{\mathrm{S}} \approx 3 \cdot 10^{12}\,\mathrm{cm}^{-2}$, the density of traps is in the range of the sheet charge density in the channel and the virtual gate length is in the range of $L_{\mathrm{G,virt}} \approx 300\,\mathrm{nm}$. This combination leads to a current collapse behavior depicted in Fig.

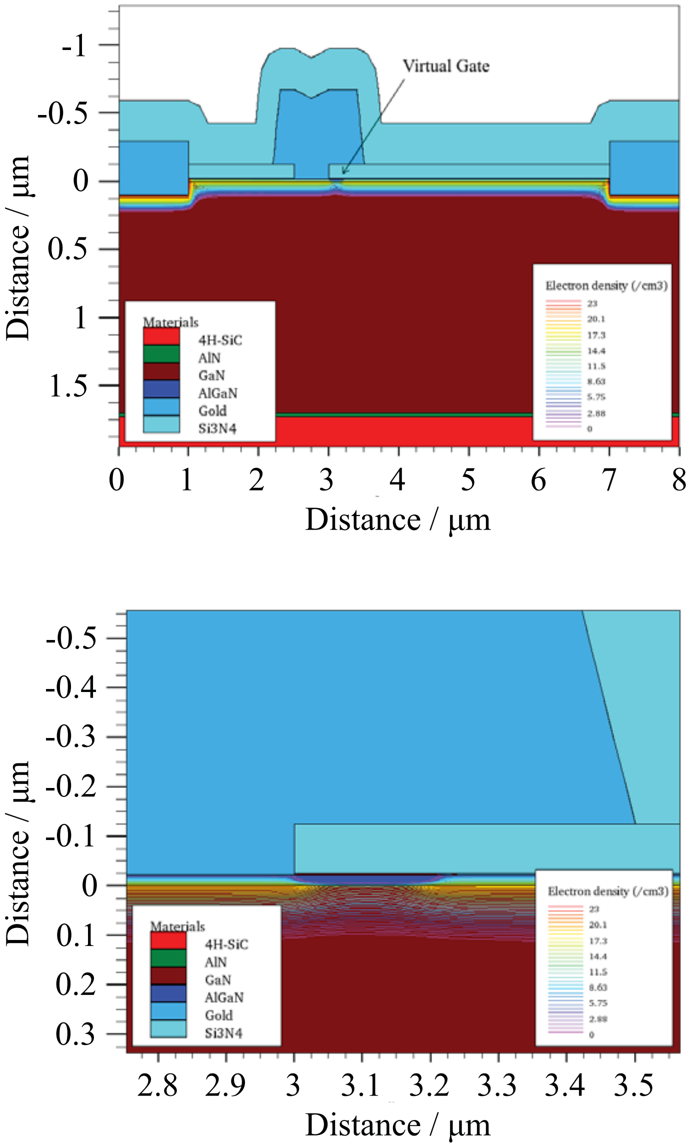
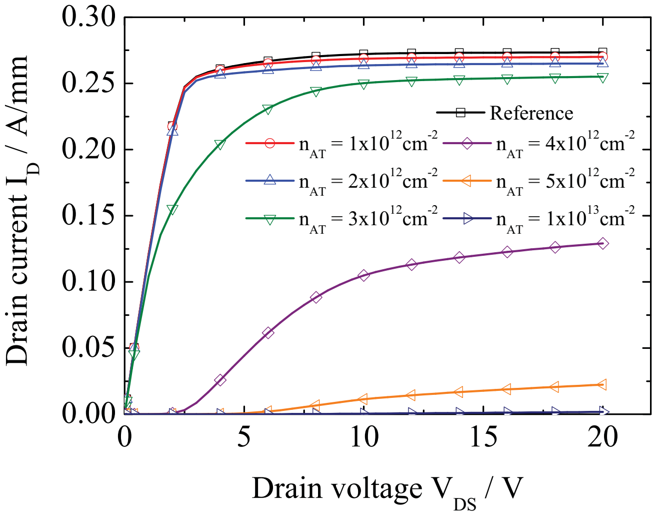
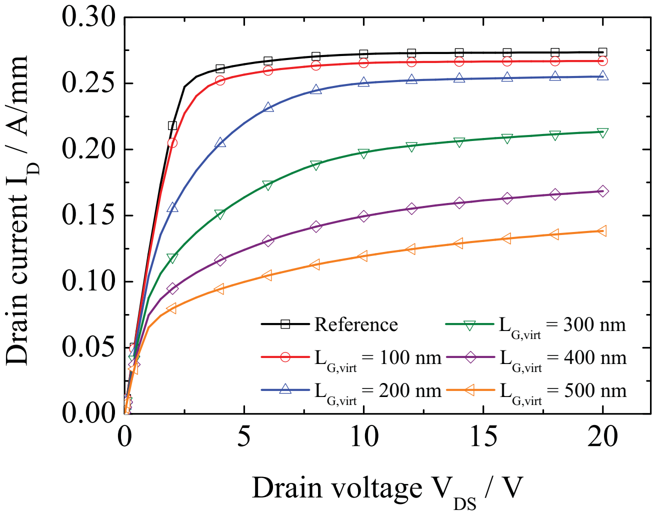


Figure 4.4: Simulated virtual gate effect at the drain-side edge of the gate with an acceptor-like trap density of $n_{\mathrm{AT}} = 5 \cdot 10^{12}\,\mathrm{cm}^{-2}$ and a gate length of the virtual gate of $L_{\mathrm{G,virt}} = 200\,\mathrm{nm}$.



(a) Simulation results of the output characteristic at $V_{GS} = 0\,\mathrm{V}$ affected by a virtual gate with a gate length of $L_{G,virt} = 200\,\mathrm{nm}$ and different trap densities.



(b) Simulation results of the output characteristic at $V_{GS} = 0\,\mathrm{V}$ affected by a virtual gate with a trap density of $n_{AT} = 3 \cdot 10^{12}\,\mathrm{cm}^{-2}$ and different virtual gate length.

Figure 4.5: Simulation study to quantify the trapping effect as root cause of current collapse.

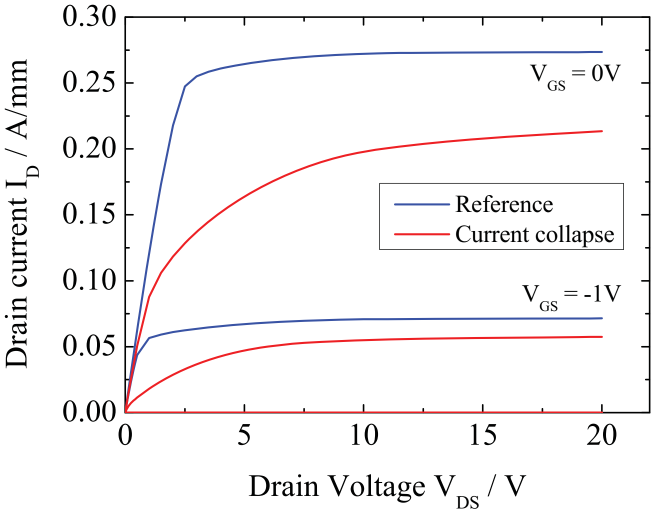


Figure 4.6: Reproduction of reasonably low current collapse assuming a $n_{\mathrm{AT}} = 3 \cdot 10^{12}\,\mathrm{cm}^{-2}$ and $L_{\mathrm{G,virt}} = 300\,\mathrm{nm}$.

4.6. It can be seen that the increase in the knee-voltage V_{k} and the reduction in drain current is nicely reproduced confirming the assumption of traps near the gate being the root cause of current collapse.

4.1.3 Transconductance Dispersion and its Impact on Linearity

It can be seen from Fig. 4.2 that with the output characteristics also the transfer characteristics and with that the related transconductance g_{m} is affected by the current collapse.

Small-Signal Transconductance

To characterize the g_{m}-dispersion, in this work we used low-frequency S-parameters measurements using a vector network analyzer described in [71]. This VNA is capable to measure S-parameters down to 1 kHz and it was used to characterized the dispersive behavior of the transconductance and the related time constant τ. The measurement setup is depicted in Fig. 4.7. The S-parameter have been measured at drain voltages of $V_{\mathrm{DS}} = 4.5\,\mathrm{V}$ and $V_{\mathrm{DS}} = 8.5\,\mathrm{V}$ with a drain current density of $I_{\mathrm{D}} = 100\,\mathrm{mA/mm}$ and $I_{\mathrm{D}} = 120\,\mathrm{mA/mm}$. These quite small drain voltages were chosen to be high enough to drive the device in the saturation region of its output characteristics and to be small enough to prevent the measurement results from being affected by

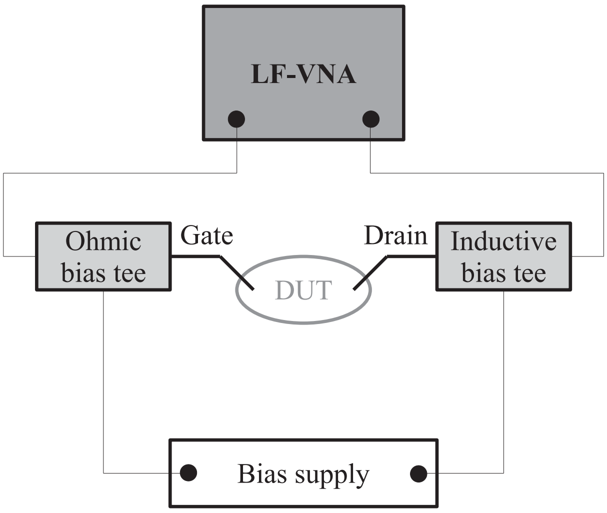


Figure 4.7: Measurement setup for low-frequency S-parameter measurements.

impact ionization which typically occurs at higher drain voltage [72,73]. The S-parameters were measured in a frequency range of $f = 100\,\text{kHz} \ldots 100\,\text{MHz}$. The lower limit in frequency is a consequence of the highpass characteristics of the utilized ohmic bias tee in which a high value ohmic resistor is used as DC feed. The transmission characteristics of the ohmic bias tee plotted in Fig. 4.8 show a 3 dB-cut-off frequency of $f_{3\,\text{dB}} = 23\,\text{kHz}$. The small-signal transconductance was extracted from the measured S-parameters using the small-signal parameter extraction procedure described in [69] and plotted versus frequency. In Fig. 4.9 the small-signal transconductance is plotted for several measurement conditions versus frequency. A clear frequency dependence of g_m is observed comparable to what has been published by Ladbrooke et al. for GaAs MESFET's [74]. From this plot, we find that the transconductance dispersion is independent of the drain current density and it makes no difference if the measurements are taken with illumination or in the dark. This means that the trap energy level is deeper in energy than the energy of visible light. On the other hand, a strong dependence on the drain voltage is observed which supports again the theory from subsection 4.1.2 that traps causing dispersion are charged by the externally applied electric field. If we take the 3 dB-cut-off frequency $f_\text{Disp} = 2\,\text{MHz}$ as a criterion for the determination of the dispersion time constant τ_Disp indicated by the dashed line in Fig. 4.9(a) we get the time constant calculated in equation (4.5).

$$\tau_\text{Disp} = \frac{1}{2\pi f_\text{Disp}} = 8 \cdot 10^{-8}\,\text{s} \tag{4.5}$$

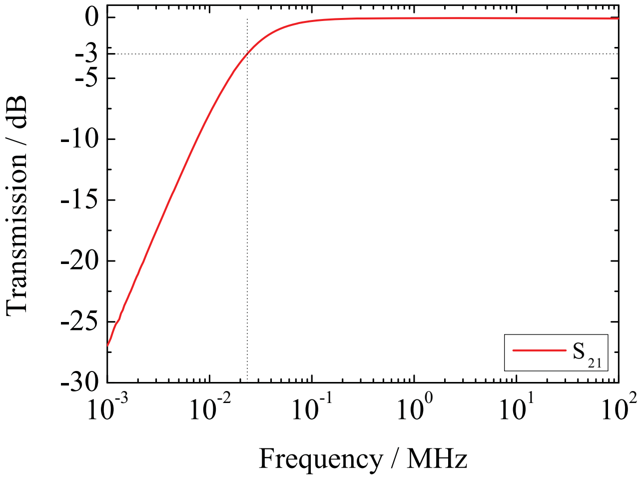


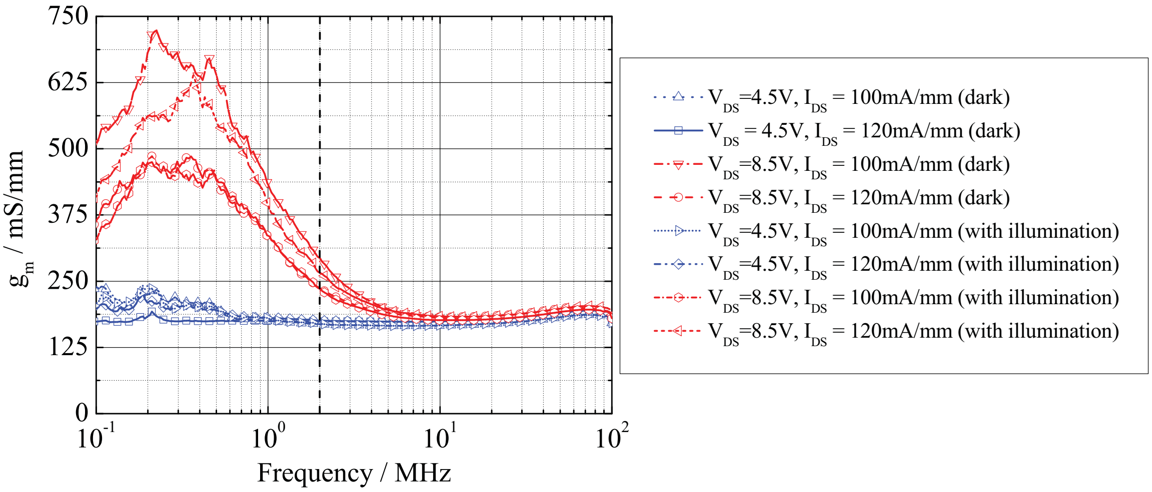
Figure 4.8: Measured transmission characteristics of the ohmic bias tee.

Due to the good agreement between theory and experiment we conclude that low-frequency S-parameter measurements are a powerful technique to characterize dispersive devices.

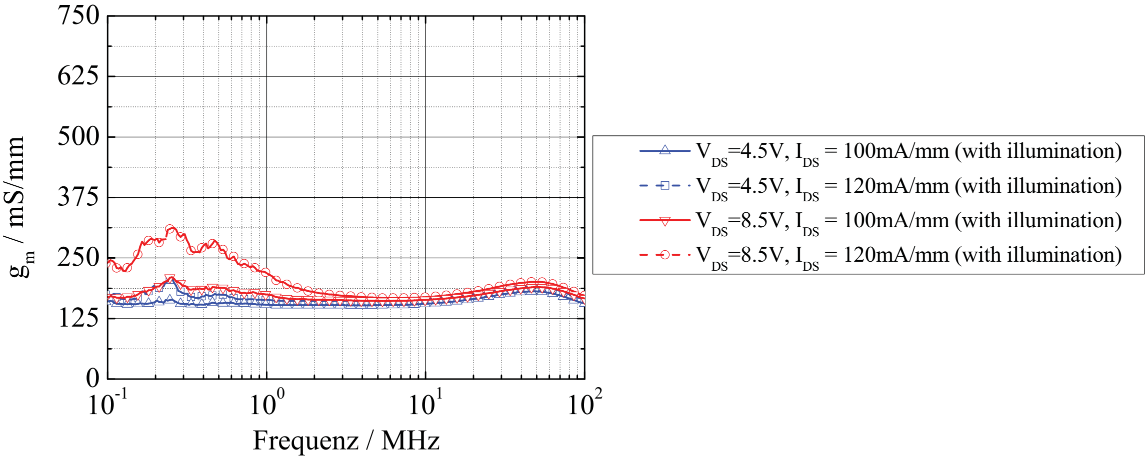
Linearity

Another characteristic which is closely linked to the transfer characteristics is the two-tone linearity measured by the third-order intermodulation distance IMD3. The output of a linear system under two-tone operation with two input tones $f_1 = A_1 \cdot cos(\omega_1 t)$ and $f_2 = A_2 \cdot cos(\omega_2 t)$ is given by $B \cdot (f_1 + f_2)$ with the transfer function B of the system (e.g. gain or attenuation). However, a non-linear system like a HEMT shows typically an output spectrum under two-tone operation with a tone-spacing Δf as depicted in Fig. 4.10. The third-order intermodulation distance IMD3 is given by the difference in amplitude of the fundamental tone and one of the third-order intermodulation products $2f_1 - f_2$ or $2f_2 - f_1$. For the mathematical description of IMD3 we start with a Taylor series expansion of the transconductance g_m in equation (4.6) as it is known to be the dominant parameter for the IMD3 linearity and we neglect terms higher than third order. Here, we assume $\Delta V_\mathrm{GS} << V_\mathrm{GS}$ and for all expressions in this subsection V_GS is used for visibility but is meant to be the reduced gate-sourse voltage $V_\mathrm{GS} - V_\mathrm{p}$.

$$g_\mathrm{m}(V_\mathrm{GS} + \Delta V_\mathrm{GS}) = g_\mathrm{m}(V_\mathrm{GS}) + \frac{\partial g_\mathrm{m}(V_\mathrm{GS})}{\partial V_\mathrm{GS}} \cdot V_\mathrm{GS} + \frac{1}{2!} \cdot \frac{\partial^2 g_\mathrm{m}(V_\mathrm{GS})}{\partial V_\mathrm{GS}^2} \cdot V_\mathrm{GS}^2 \ldots \quad (4.6)$$



(a) Small-signal transconductance of a transistor showing high dispersion.



(b) Small-signal transconductance of a transistor showing low dispersion.

Figure 4.9: Small-signal transconductance extracted from measured S-parameters.

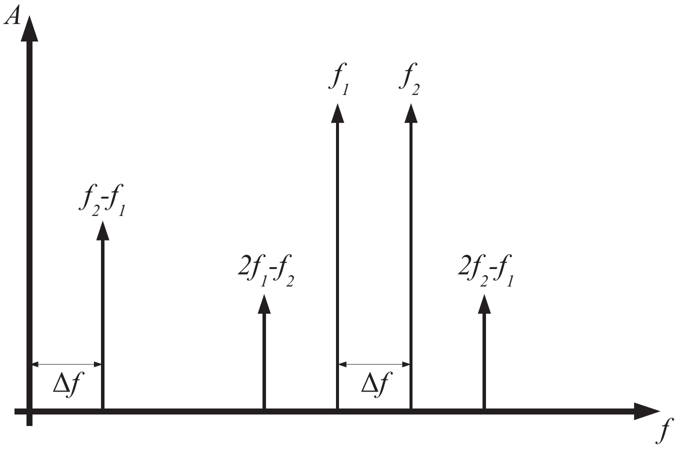


Figure 4.10: Theoretical output spectrum of a non-linear system under two-tone operation.

With the relations in equations (4.7) and (4.8) we get the expression for the output parameter of the transistor I_D in equation (4.9).

$$V_\mathrm{GS} = A_1 \cdot cos\left(\omega_1 t\right) + A_2 \cdot cos\left(\omega_2 t\right) \tag{4.7}$$

$$I_\mathrm{D} = g_\mathrm{m} \cdot V_\mathrm{GS} \tag{4.8}$$

$$I_\mathrm{D}\left(V_\mathrm{GS}, \Delta f\right) = g_\mathrm{m}\left(V_\mathrm{GS}, \Delta f\right) \cdot V_\mathrm{GS} + \frac{\partial g_\mathrm{m}\left(V_\mathrm{GS}, \Delta f\right)}{\partial V_\mathrm{GS}} \cdot V_\mathrm{GS}^2 + \frac{1}{2} \cdot \frac{\partial^2 g_\mathrm{m}\left(V_\mathrm{GS}, \Delta f\right)}{\partial V_\mathrm{GS}^2} \cdot V_\mathrm{GS}^3 \tag{4.9}$$

Here we introduced the beat frequency dependence of the transconductance $g_\mathrm{m}\left(V_\mathrm{GS}, \Delta f\right)$ and we see that the frequency dependence is directly transferred to the IMD3 behavior of a transistor. The schematic spectrum of the non-linear output of a device under two-tone operation in Fig. 4.10 shows a spectral component equal to the tone-spacing Δf which has a comparable large amplitude. This frequency is responsible for the modulation of the dispersive transconductance. To measure the dispersive characteristics of the two-tone linearity IMD3 we used the setup schematically depicted in Fig. 4.11. It has to be noticed that the device is measured in a $50\,\Omega$ environment which is not the ideal operation in terms of linearity because the device is not matched for optimum linearity to this impedance. In order to suppress the generation of higher harmonics in the spectrum which occur under operation in compression, we chose the input power to $P_\mathrm{in} = 0\,\mathrm{dBm}$ to ensure linear operation of the device. Since the beat frequency Δf is believed to be the driver for the dispersion in linearity, we measured the IMD3 at $f_1 = 2\,\mathrm{GHz}$ and $f_2 = 2\,\mathrm{GHz} + \Delta f$ versus the applied tone-spacing. An example of a measured frequency spectrum

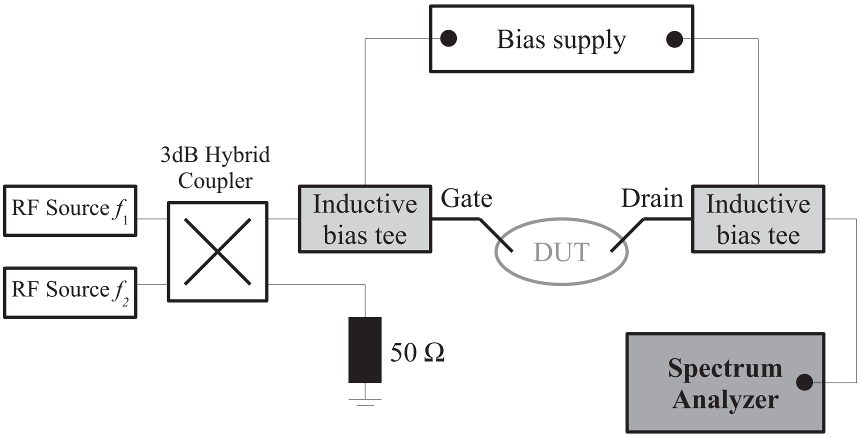


Figure 4.11: Measurement setup for two-tone IMD3 measurements.

is shown in Fig. 4.12. From the measured spectra the IMD3 distances have been extracted and plotted versus the applied tone-spacing. The results are plotted in Fig. 4.13. The measurement results show a decrease of the third-order intermodulation product with increasing tone-spacing. The 3 dB-cut-off frequency was determined to $f_{\mathrm{Disp}} = 5\,\mathrm{MHz}$ which is slightly higher compared to the value obtained from the transconductance dispersion but still close enough to conclude that the link between transconductance and linearity dispersion is proven. The simplest description of this behavior for compact modeling purposes like in [75] is to fit the data with an empirical exponential function such as equation (4.10).

$$\mathrm{IMD3}\left(\Delta f\right) = \mathrm{IMD3}_0 + C \cdot e^{-\frac{\Delta f}{f_0}} \tag{4.10}$$

The fitting is shown by the gray dashed line in Fig. 4.13. In the end, we can conclude that transconductance dispersion is directly affecting the linearity of a device. This fact is important especially in the design of wide-band RF amplifiers since the tone-spacing can vary within the frequency bandwidth of the respective application.

4.2 Leakage Currents

It has been always a challenge to investigate the root cause of leakage currents in semiconductor devices regardless whether they are active or passive since there is a high number of physical

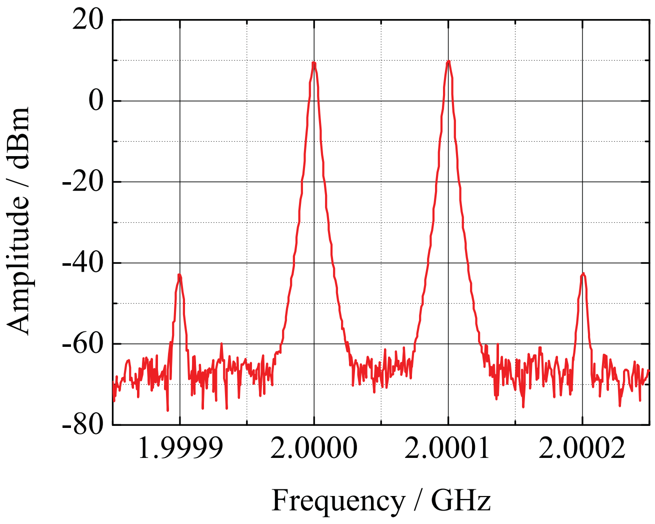


Figure 4.12: Measured frequency spectrum at a tone-spacing of $\Delta f = 100\,\mathrm{kHz}$.

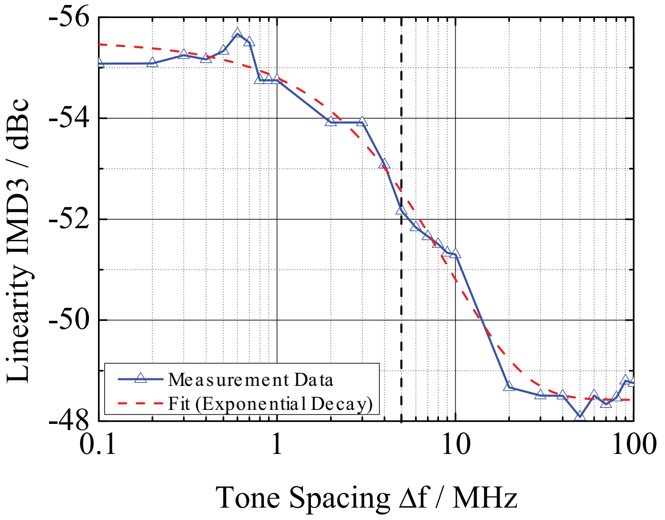


Figure 4.13: Measured third-order intermodulation distance IMD3 versus applied tone-spacing.

mechanisms depending on device type and material system that may cause or at least contribute to the leakage currents measured externally at the ports of the respective device. Semiconductor physics offers effects like thermionic emission, classical tunneling or even trap assisted tunneling which is a tunneling mechanism assisted by an hopping mechanism among traps in the respective energy barrier. These effects are the most important ones in III-V devices.

Avoiding excessive leakage currents in RF and microwave devices is important for two major reasons. According to [76] the gate leakage current strongly affects the minimum noise figure of a device. This is due to the increase in shot noise which is caused by the transition of free charge carriers over an energy barrier which must be due to thermionic emission. The Schottky energy barrier with more than 1 eV, however, is too high that the leakage current at room temperature can be caused by thermionic emission only. Thus, we assume that gate leakage in AlGaN/GaN devices is caused by a combination of tunneling and thermionic emission. The second effect of excessive leakage is seen very often in experiments but still not proven. It is believed that a high level of leakage current strongly affects the device reliability since it drastically reduces its lifetime. The investigation of the impact of leakage current on device reliability, however, is beyond the scope of this work. In this section we want to focus on the origin of leakage encountered right from the beginning of the device lifetime.

4.2.1 Schottky Diode Leakage

This subsection focuses on the pure Schottky diode leakage of a device. It is the leakage measured in the so called two-terminal configuration where either the source or the drain potential is floating. For simplicity, we just characterize and analyze the gate-source diode which means in this case a floating drain potential.

All the devices used for characterization had a gate length of $L_\mathrm{G} = 500\,\mathrm{nm}$ and were processed utilizing a dielectric assisted gate process. During processing the semiconductor surface on which the Schottky interface is formed is exposed to a fluorine-based plasma for the etching of the gate foot trench into the passivation. A high number of devices either processed differently or on different epitaxial layers were characterized and the leakage of the Gate-Source diode at $V_\mathrm{GS} = -6\,\mathrm{V}$ is plotted versus the sheet resistance of the respective epitaxial HEMT structure in Fig. 4.14. There are two major facts to be noticed from this plot. The first fact is the general observation that the device processing is capable to vary the level of leakage current over several orders of magnitude. The second observation indicates that a higher sheet resistance reduces the upper limit of the level of leakage and is therefore beneficial.

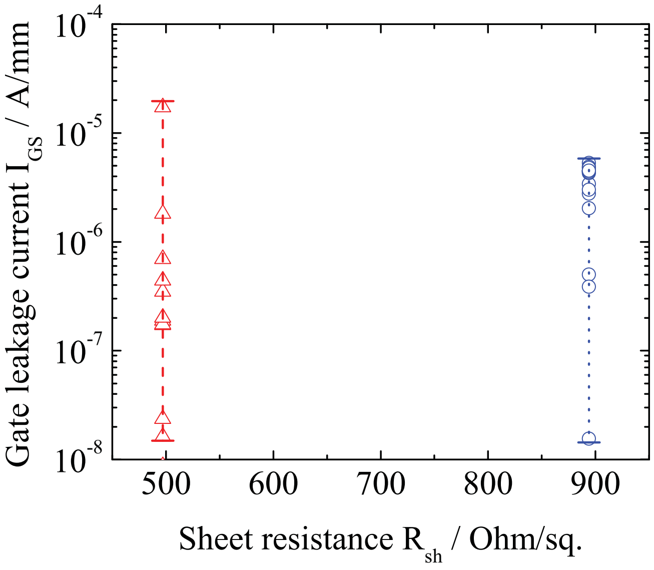
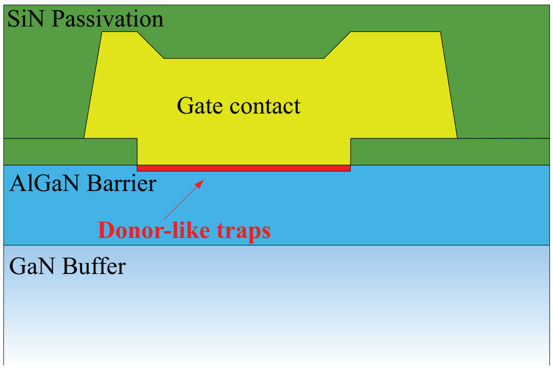
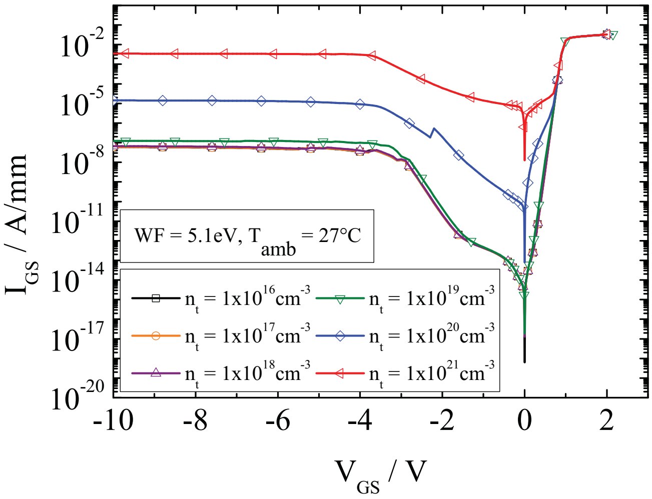


Figure 4.14: Gate-Source leakage current of several devices on epitaxial structures with two different sheet resistances at $V_{GS} = -6\,\mathrm{V}$ with floating Drain potential.

Due to the process sequence which is described in appendix B we assume that the Schottky diode leakage current is a consequence of plasma damage of the semiconductor. According to [77], plasma damage induces Nitrogen vacancies which act as donor-like traps. These traps are distributed in energy level over the whole band gap, however, we just want to account for the active fraction of those traps and we therefore assume the energy level to be $E_C - E_T = 0.2\,\mathrm{eV}$ which is the lowest level calculated by [78,79]. To check the feasibility of this assumption, we perform a simulation study using the model discussed in subsection 3.2.2. For the modelling of plasma damage donor-like traps were placed in a thin layer of 2 nm below the Schottky interface. The density of these traps was varied and the I-V characteristic of the Gate-Source diode was simulated. Fig. 4.15 shows schematically the location of traps along with simulation results.. For this simulation study the epitaxial structure contained an Aluminum fraction of $x_{Al} = 0.25$ in the AlGaN barrier layer. It can be seen from the simulation results in Fig. 4.15(b) that a trap density of $N_{DT} = 1 \cdot 10^{19}\,\mathrm{cm}^{-3} \ldots 1 \cdot 10^{20}\,\mathrm{cm}^{-3}$ is needed to reach the level of leakage where we find the most experimental values. This trap density corresponds to a sheet charge density of $n_{DT} = 2 \cdot 10^{12}\,\mathrm{cm}^{-2} \ldots 2 \cdot 10^{13}\,\mathrm{cm}^{-2}$ which is in the order of magnitude of the channel sheet charge density n_S. Another effect which needs to be reproduced by the simulation study in order to prove the assumed model is the beneficial effect of a higher sheet resistance of the epitaxial structure on the leakage current level. To this end, the same simulation study was performed



(a) Illustration of location of the traps to model plasma damage.



(b) Simulated I-V charactieristic of the Gate-Source diode for different trap densities.

Figure 4.15: Simulation of the Gate-Source leakage current induced by traps.

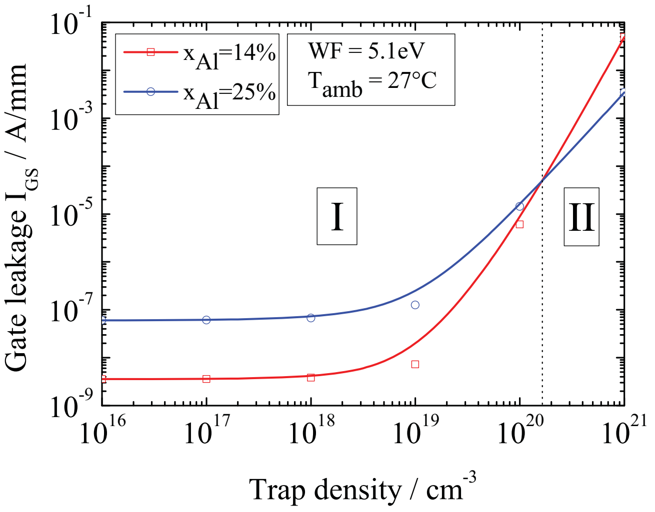


Figure 4.16: Simulated Gate-Source leakage current of epitaxial structures with two different Aluminum fractions in the Schottky barrier layer at $V_{GS} = -10\,V$.

utilizing a HEMT structure with an Aluminum faction of $x_{Al} = 0.14$ in order to reduce n_S. The simulation results at $V_{GS} = -10\,V$ versus the assumed trap density for both HEMT structures are compared in Fig. 4.16. The simulation study shows a systematic reduction of the Schottky diode leakage due to the decrease in Aluminum fraction for trap densities $N_{DT} < 1 \cdot 10^{20}\,cm^{-3}$ which is indicated in the plot as region I. We saw before that this is the region of leakage in which we statistically get the most experimental data. Thus, the study confirms the tendency of lower leakage at higher sheet resistance seen experimentally. However, when looking at region II in the plot we find for excessive trap densities the leakage for $x_{Al} = 0.14$ to be higher. Both observations indicate that we encounter two competing physical effects where each is dominating one of the two observed regions.

Region I is dominated by the lower Aluminum fraction in the AlGaN barrier. The effect of a reduced Aluminum fraction is an increased sheet resistance due to a lower polarization induced sheet charge according to equation (3.4). Under pinch-off condition, however, the dominating series resistance in the leakage path is not the source resistance, as depicted in Fig. 4.17, but the resistance induced by the depletion region below the Schottky contact $r_{DR} >> R_S$. This means that the higher sheet resistance of the epitaxy as a results of the reduced Aluminum fraction can not be the reason for a reduced level of leakage. Looking at equation (3.15), we find another parameter strongly affecting the leakage current which is also strongly modified by the

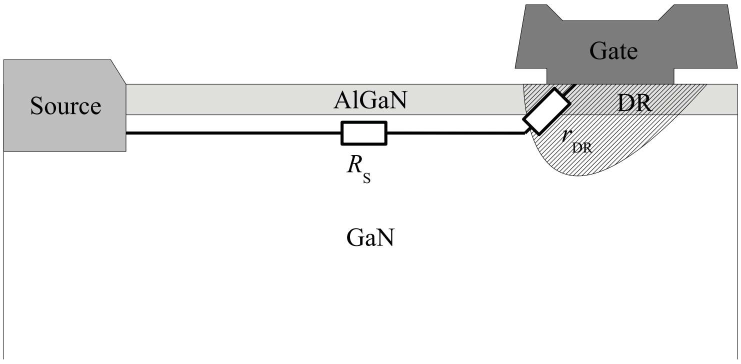
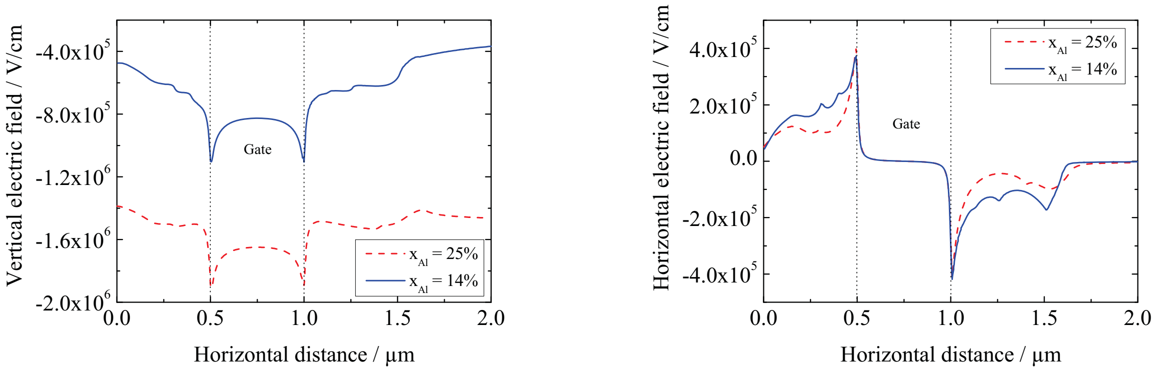


Figure 4.17: Resistance distribution in the device under 2-terminal pinch-off condition.



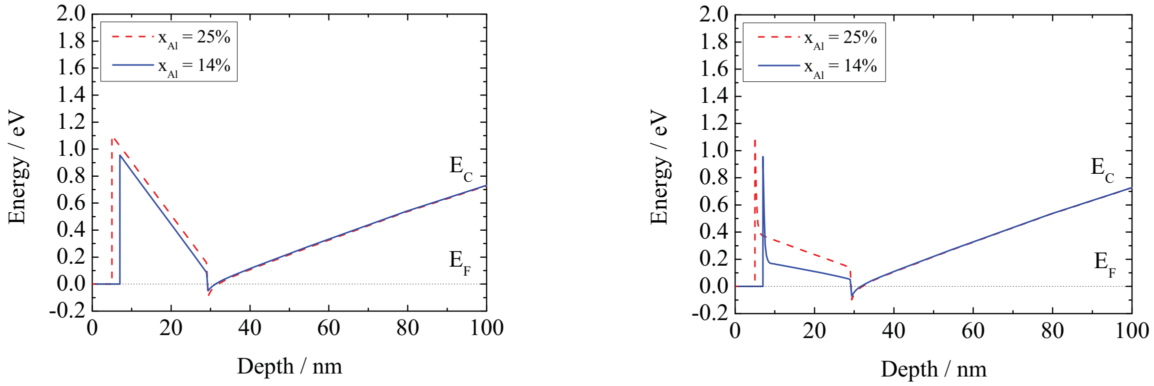
(a) Simulated vertical electric field with Gate bias $V_{GS} = -10\,\text{V}$.

(b) Simulated horizontal electric field with Gate bias $V_{GS} = -10\,\text{V}$.

Figure 4.18: Simulated electric field in the AlGaN barrier for different Aluminum fractions.

Aluminum fraction. This parameter is the electric field E. Fig. 4.18 shows the electric field within the device with applied bias. These simulations have been performed using a trap density of $N_{DT} = 1 \cdot 10^{17}\,\text{cm}^{-3}$. It can be seen that the vertical electric field is higher for the higher Aluminum fraction whereas the maximum horizontal field is nearly independent of it. This is due to the higher polarization field in the AlGaN layer which adds as an offset to the applied external field leading to a higher level of leakage.

Region II shows for excessive trap densities a higher leakage for lower Aluminum fraction. In this region the higher vertical electric field at higher Aluminum fraction is no longer the dominating effect. The reason for the higher level of leakage at lower x_{Al} and trap densities



(a) Simulated conduction band diagram for a trap density of $N_{DT} = 1 \cdot 10^{17}\,\mathrm{cm}^{-3}$.

(b) Simulated conduction band diagram for a trap density of $N_{DT} = 1 \cdot 10^{21}\,\mathrm{cm}^{-3}$.

Figure 4.19: Simulated conduction band diagram for different Aluminum fractions and trap densities.

$N_{DT} > 1 \cdot 10^{20}\,\mathrm{cm}^{-3}$ becomes clear when looking at the respective conduction band diagrams of the Schottky diode for a low and high trap density. The simulated conduction band diagrams are depicted in Fig. 4.19. For excessive trap densities the conduction band in the AlGaN barrier is bended reducing the effective Schottky barrier thickness drastically whereas for moderate trap densities the bending is not pronounced. Now, comparing the band diagrams at high trap density in Fig. 4.19(b) it turns out that the remaining energy barrier between quantum well and Schottky barrier is higher for $x_{Al} = 0.25$ which leads to a lower level of leakage compared to $x_{Al} = 0.14$. There are two reasons for this higher energy barrier. First of all, the conduction band discontinuity ΔE_C is larger due to the higher Aluminum fraction which can be seen in Fig. 4.19(b) and also from equation (3.3). Secondly, the Schottky barrier hight is higher for larger x_{Al} because of the larger band gap of AlGaN. In both cases a Nickel-based Gate contact was assumed with the workfunction of Nickel $\chi_{Ni} = 5.1\,\mathrm{eV}$. In the end, we can conclude that the energy configuration of the respective Schottky diode is dominating over the higher vertical electric field for very high trap densities as in region II.

4.2.2 Transistor Leakage

After the detailed discussion of the Schottky diode leakage, the investigation is now extended to the real transistor or 3-terminal operation. According to the conclusions from the previous section it is necessary to assume a trap density at the Schottky interface of at least $N_{DT} =$

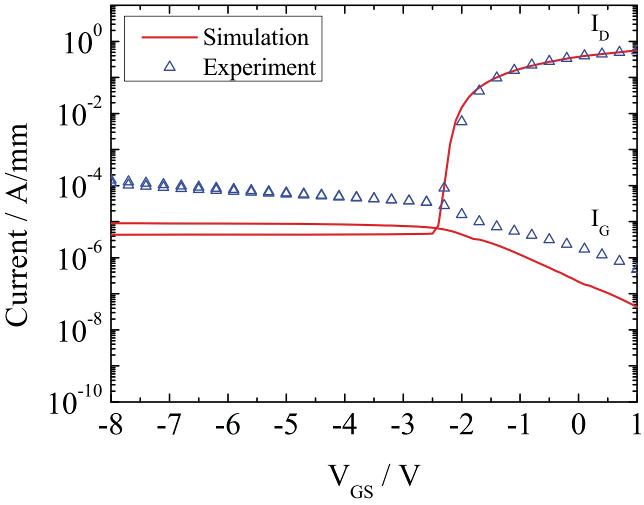


Figure 4.20: Measured and simulated 3-terminal leakage current at $V_{DS} = 10\,V$ on epitaxy with $x_{Al} = 0.18$.

Process	**Sample I**	**Sample II**	**Sample III**	**Sample IV**
SiN (n)	PECVD (2.3)	ICPECVD (2.0)	PECVD (2.3)	ICPECVD (2.0)
Relative overetch	30 %	51.6 %	51.6 %	89.6 %
Chemistry	CF_4	SF_6	SF_6	SF_6

Table 4.2: Design of experiment to assess 3-terminal leakage current.

$5 \cdot 10^{19}\,\mathrm{cm}^{-3}$ to reach experimental values for 2-terminal leakage. In the following 3-terminal simulations a constant trap density of $N_{DT} = 1 \cdot 10^{20}\,\mathrm{cm}^{-3}$ is assumed and the simulations have been performed at a drain bias of $V_{DS} = 10\,V$. The simulated and measured transfer characteristics are plotted in Fig. 4.20. It is becomes obvious that the pure assumption of traps below the Gate contact is not sufficient to reproduce the experimental leakage current.

To investigate the missing contribution to the leakage current an experiment has been carried out in which the over etch time and the chemistry of the dry etch process was varied as well as the passivation deposition technique which is believed to change the dielectric properties of the SiN passivation. These dielectric properties are represented by the optical refractive index n. The design of experiment is summarized in Table 4.2. After complete processing of the samples, the transfer characteristics have been measured and compared to each other. The comparison of the experimental results is depicted in Fig. 4.21. It turns out that the overetch has no impact in the leakage level. Moreover, the measurement results show a clear dependence of the leakage cur-

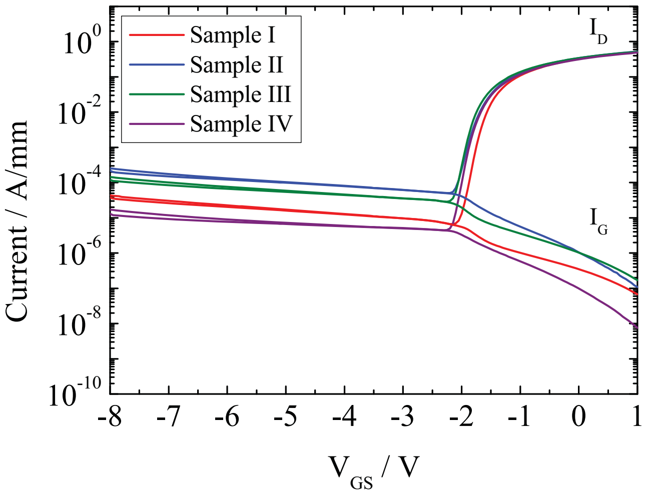


Figure 4.21: Comparison of the experimental results obtained from the leakage assessment experiment.

rent on the applied passivation. However, Sample II seems not to follow that trend. The reason for the higher leakage is an Argon plasma applied to the semiconductor surface in order to clean it. This plasma is known to cause additional plasma damage to the semiconductor resulting in an additional rise in leakage current. Sample I shows the lowest leakage of all. One reason for this could be that CF_4-based plasma produce ions which are lighter than those of SF_6-based plasma causing less plasma damage.

The main difference in the passivation is the corresponding optical refractive index n determined by optical ellipsometry. The refractive index, furthermore, increases with the Si content in the SiN passivation and its physical density. ICPECVD deposited SiN is known to be more dense than SiN deposited by PECVD. Furthermore, the higher refractive index of the ICPECVD deposited SiN also indicates a higher amount of Si in the SiN layer. Both facts lead to a higher density of fixed charges in the bulk SiN. We now consider these fixed charges throughout the whole first SiN layer and vary the density in the simulation to investigate their effect on the 3-terminal leakage current. The dependence of the leakage current on the passivation charge density is depicted in Fig. 4.22. As can be seen in Fig. 4.23, a density of $Q_{\mathrm{SiN}} = 9 \cdot 10^{17}\,\mathrm{cm}^{-3}$ for the passivation charges is needed to fit experimental data. The reason for the increase in leakage current with increasing passivation charge becomes clear when extracting again the electric field in the Schottky barrier throughout the device. The vertical electric field is plotted in Fig. 4.24. It can be seen that the vertical electric field increases with increasing passivation charge density.

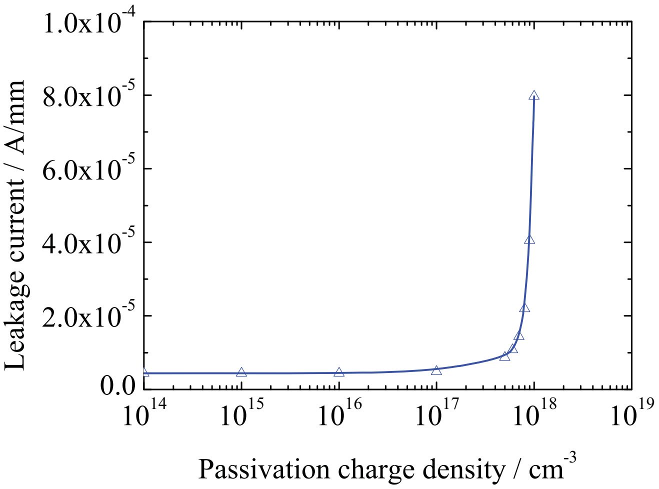


Figure 4.22: Simulated 3-terminal leakage current at $V_{\mathrm{GS}} = -7\,\mathrm{V}$ and $V_{\mathrm{DS}} = 10\,\mathrm{V}$ versus passivation charge density Q_{SiN}.

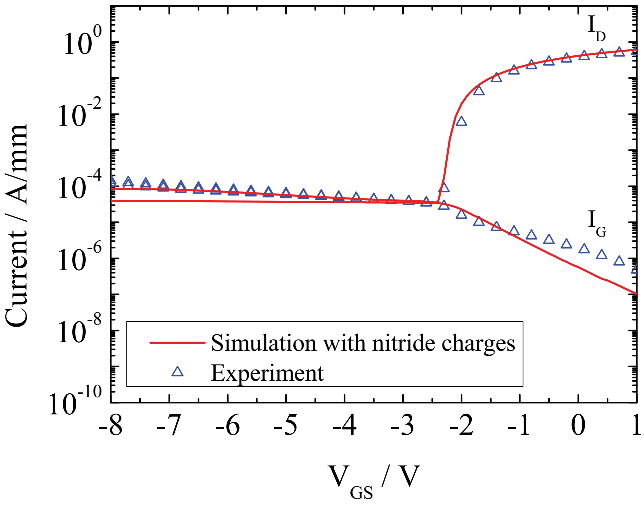
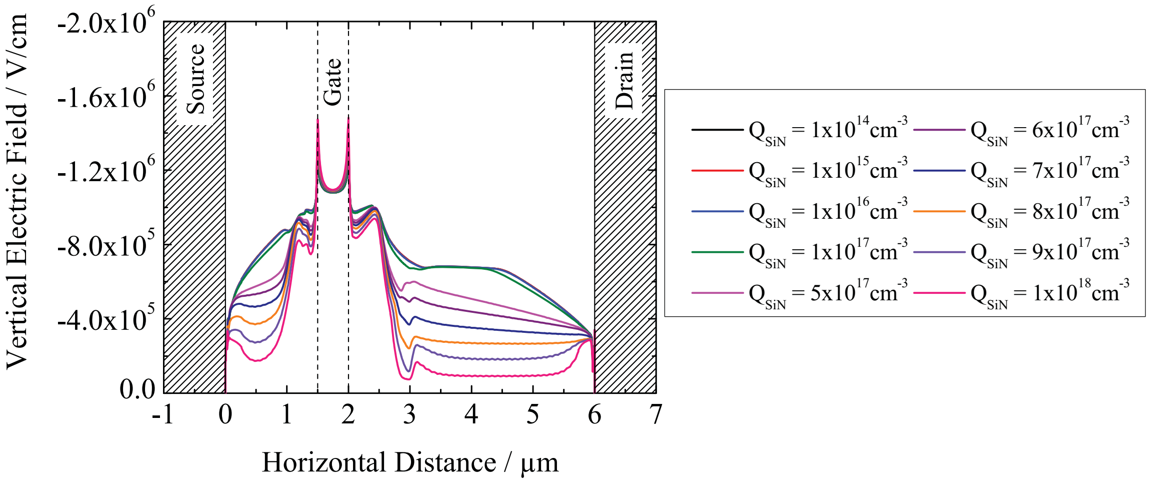
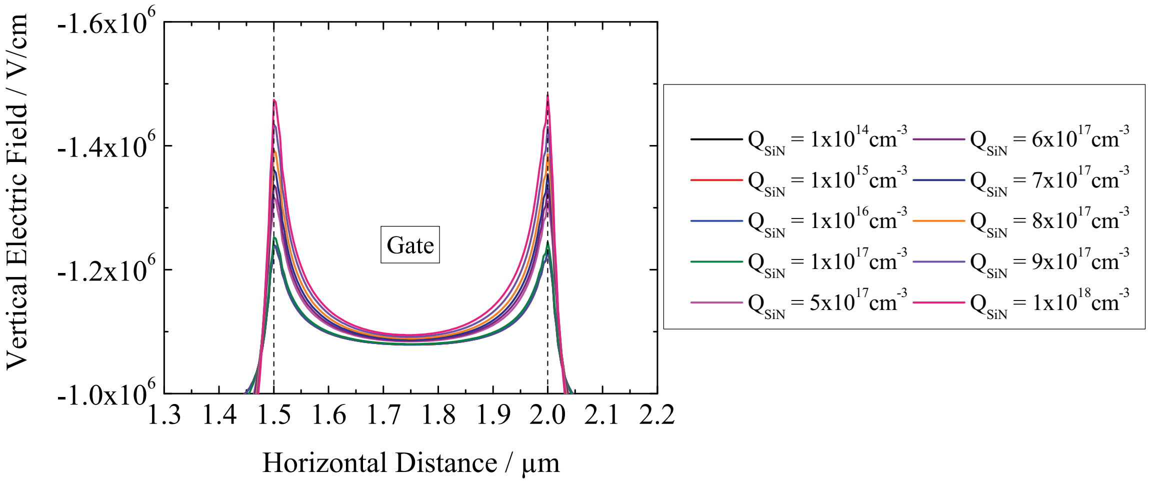


Figure 4.23: Measured and simulated 3-terminal leakage current at $V_{\mathrm{DS}} = 10\,\mathrm{V}$ on epitaxy with $x_{\mathrm{Al}} = 0.18$ and a passivation charge of $Q_{\mathrm{SiN}} = 9 \cdot 10^{17}\,\mathrm{cm}^{-3}$.



(a) Simulated vertical electric field in the AlGaN barrier layer throughout the whole device.



(b) Simulated vertical electric field in the AlGaN barrier layer below the Gate contact.

Figure 4.24: Simulated vertical electric field in the AlGaN barrier layer for different charge densities in the passivation at $V_{\mathrm{GS}} = -7\,\mathrm{V}$ and $V_{\mathrm{DS}} = 10\,\mathrm{V}$.

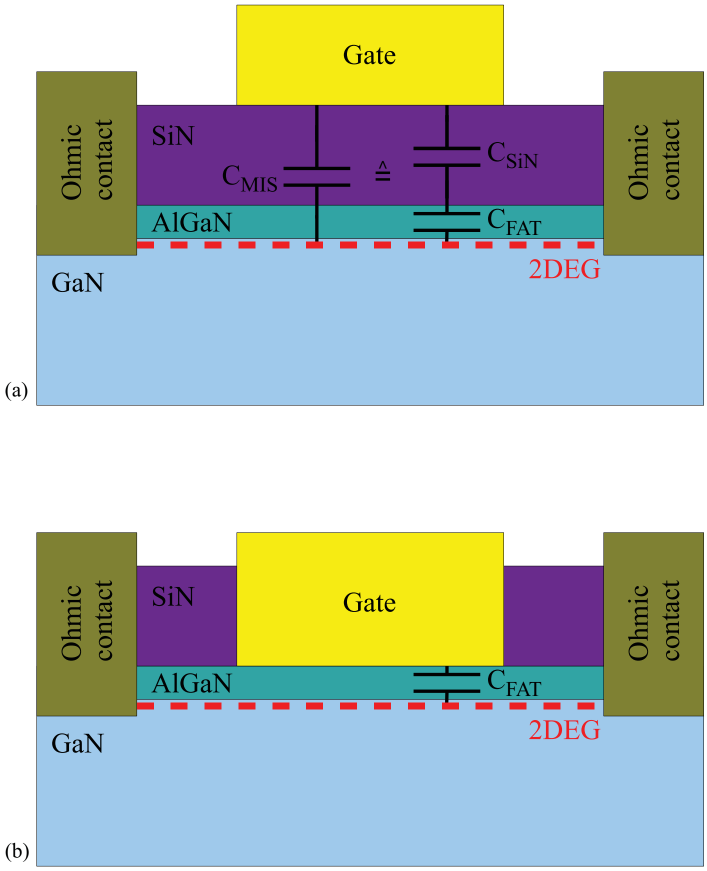


Figure 4.25: Schematic drawing of the capacitance contributions in a MISFET (a) and a FATFET (b) structure.

Especially the field at the gate contact increases by 25 % in the simulated range. This tremendous increase in electric field causes the increase in 3-terminal leakage and is the dominating effect.

4.2.3 Silicon Nitride Passivation Layer Analysis

To proof the impact of charges in the SiN passivation layer on the transistor leakage, we analyze the density of charges in different SiN layers leading to different levels of 3-terminal leakage current. For this analysis C-V measurements have been performed on large area MISFET and FATFET structures of same size. As can be seen schematically in Fig. 4.25 there are two major contributions to the overall capacitance of the MISFET structure caused by the SiN layer and the AlGaN barrier layer as mathematically expressed in (4.11).

$$\frac{1}{C_{\mathrm{MIS}}} = \frac{1}{C_{\mathrm{FAT}}} + \frac{1}{C_{\mathrm{SiN}}} \tag{4.11}$$

To separate the SiN layer contribution from the whole MISFET capacitance, the capacitance caused by the AlGaN barrier layer is determined by C-V measurements on a FATFET structure of same size as the MISFET. Knowing the capacitance C_{FAT} of the FATFET and the capacitance C_{MIS} of the MISFET, the capacitance of the SiN layer C_{SiN} can be calculated as in equation (4.12).

$$C_{\mathrm{SiN}} = \frac{C_{\mathrm{FAT}} \cdot C_{\mathrm{MIS}}}{C_{\mathrm{FAT}} - C_{\mathrm{MIS}}} \tag{4.12}$$

To calculate and separate the charge density in the SiN layer deposited onto the semiconductor surface, the charge density of the FATFET corresponding to the sheet charge density of the heterostructure needs to be subtracted from the total charge density determined in the MISFET. This can be mathematically expressed by equation (4.13).

$$Q_{\mathrm{SiN}} = Q_{\mathrm{MIS}} - Q_{\mathrm{FAT}} = \int_{V_{G,1}}^{V_{G,2}} C_{\mathrm{MIS}} \,\mathrm{d}V - \int_{V_{G,1}}^{V_{G,2}} C_{\mathrm{FAT}} \,\mathrm{d}V \tag{4.13}$$

For the experiment, the SiN surface passivation has been modified on two samples resulting in the transfer characteristics of the respective devices plotted in Fig. 4.26. The modification in the surface passivation results in a 3-terminal leakage current which is one order of magnitude lower compared to the reference sample. On these samples the MISFET and FATFET structures have been characterized by C-V measurements at 1 MHz. The measured C-V graphs of both structures are plotted in Fig. 4.27 and 4.28. The C-V graphs show in all cases the expected evolution from pinch-off to open channel. The transition between both regions can be seen by an increase of the capacitance at the pinch-off voltage of the structure. In case of the FAFET the capacitance drops again at the gate voltage where the Schottky diode starts to conduct short-circuiting the capacitance. This technique to determine the charges in SiN layers has already been elaborated by Fagerlind et al. [80]. From these measurement the sheet carrier density of the heterostructure and the charge density in the SiN layer has been calculated using equation (4.13). The results are summarized in table 4.3. It can be seen that the sheet charge density is comparable in both cases as expected since the same epitaxial structure has been used for both samples in order to exclude the effect of the epitaxy on the device leakage current. However, the charge density in the SiN layer is lower by a factor of two for the modified SiN layer compared to the

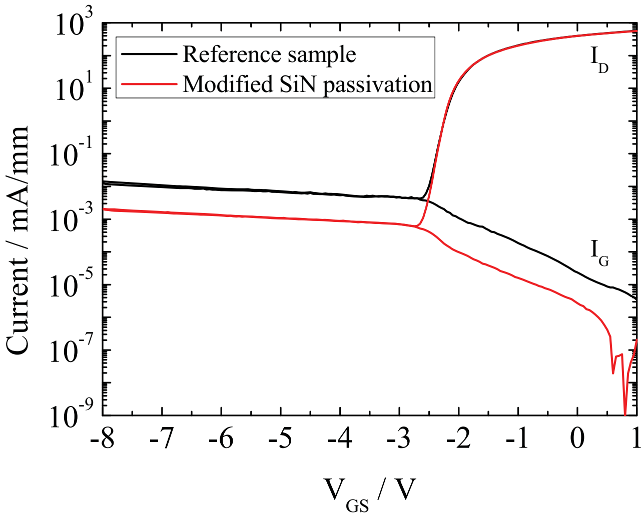


Figure 4.26: Transfer characteristic of 1 x 100 μm devices at $V_{\mathrm{DS}} = 10\,\mathrm{V}$ with different surface passivation.

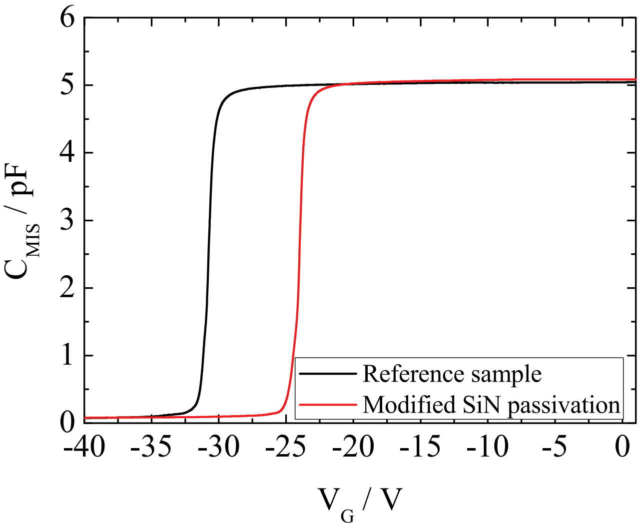


Figure 4.27: C-V graphs of a MISFET structure with different surface passivation.

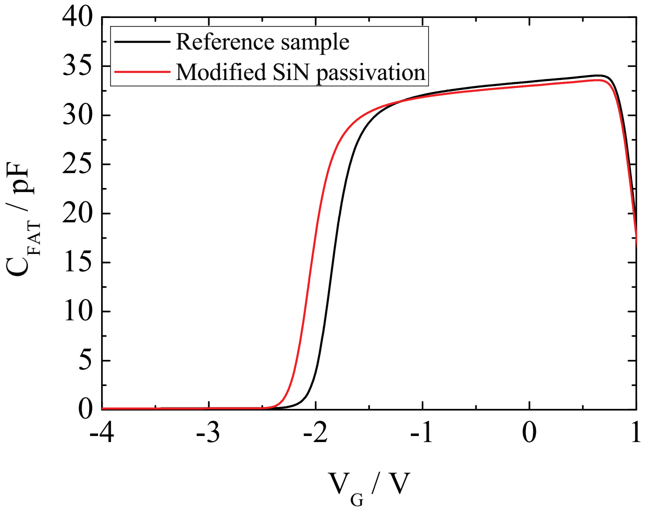


Figure 4.28: C-V graphs of a FATFET structure with different surface passivation.

Structure	$\mathbf{n_S}$	$\mathbf{n_{SiN}}$
Reference	$5.89 \cdot 10^{12}\,\mathrm{cm}^{-2}$	$4.12 \cdot 10^{12}\,\mathrm{cm}^{-2}$
Modified	$6.19 \cdot 10^{12}\,\mathrm{cm}^{-2}$	$1.82 \cdot 10^{12}\,\mathrm{cm}^{-2}$

Table 4.3: Summary of calculated sheet charge and SiN charge densities for the reference structure and the modified SiN passivation.

reference sample. As shown at the beginning of this subsection, the modified SiN passivation also yields a leakage current level which is an order of magnitude lower compared to the reference sample. Since we can exclude a potential impact of the epitaxial layers and we furthermore take the already discussed simulation results into account, we can conclude that the surface passivation and the linked nitride charges have severe impact on the level of leakage current in 3-terminal operation. It is worth mentioning that in the simulation the assumed charges have been distributed homogeneously throughout the whole SiN layer. In real devices, however, it is more likely that the charges are located directly at the semiconductor-passivation interface. Nevertheless, the model is valid since in both cases the physical mechanism is a modification of the surface potential which leads to a drastic increase of the electric field near the gate contact under pinch-off operation and therefore leads to an increased level of 3-terminal leakage current.

4.3 Self-Heating

4.3.1 Thermal Resistance

The self-heating of a high-power device and the related thermal management is also a crucial topic. Micro-Raman thermography measurements are a technique to measure the device temperature with very high spatial resolution as already discussed. This measurement technique was used for the determination of the *thermal resistance* of a device which is an important parameter for the judgment of the thermal management. The definition of the thermal resistance R_{th} is given by the analytical expression of the junction temperature T_{j} in equation (4.14). In this equation T_{amb} is the ambient temperature applied to the backside of the DUT via the chuck of the setup.

$$T_{\mathrm{j}} = R_{\mathrm{th}} \cdot P_{\mathrm{diss}} + T_{\mathrm{amb}} \tag{4.14}$$

Experimentally, the thermal resistance is determined by micro-Raman measurements measuring the device temperature versus the applied dissipated power density P_{diss}. When taking two junction temperatures $T_{\mathrm{j},1}$ at $P_{\mathrm{diss},1}$ and $T_{\mathrm{j},2}$ at $P_{\mathrm{diss},2}$ the thermal resistance can be calculated by equation (4.15).

$$R_{\mathrm{th}} = \frac{\left(T_{\mathrm{j},2} - T_{\mathrm{amb}}\right) - \left(T_{\mathrm{j},1} - T_{\mathrm{amb}}\right)}{P_{\mathrm{diss},2} - P_{\mathrm{diss},1}} = \frac{\Delta T_{\mathrm{j}}}{\Delta P_{\mathrm{diss}}} \tag{4.15}$$

This means that the thermal resistance is equivalent to the slope of the measured relation between T_{j} and P_{diss} as schematically depicted in Fig. 4.29. It is a measure of the temperature rise in the

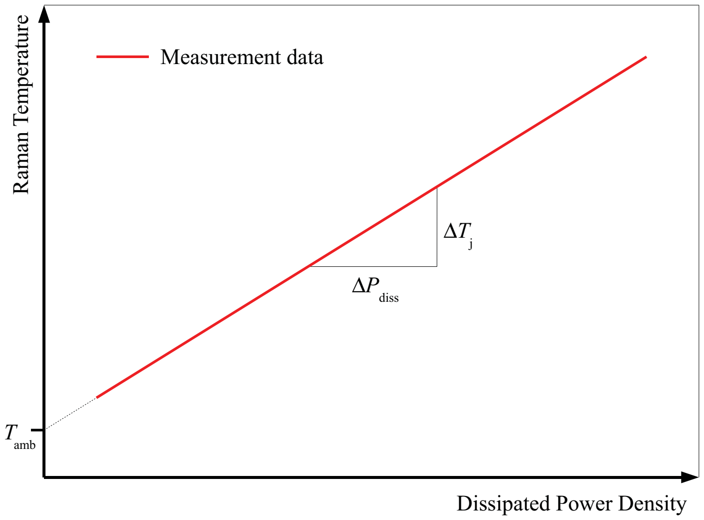


Figure 4.29: Schematic plot of the experimental determination of R_{th}.

device with a certain increase in the dissipated power density and therefore also independent on the ambient temperature T_{amb}.

4.3.2 Field-Dependent Self-Heating Effects

The device temperature was measured on a 8 x 250 μm device with a gate length of $L_G = 250$ nm and on a 2 x 43 μm device with a gate length of $L_G = 500$ nm on-wafer using micro-Raman thermography. The measurement results are plotted in Fig. 4.30. During these measurements the dissipated power density was varied at fixed drain voltages of $V_{DS} = 25$ V and $V_{DS} = 50$ V. The measurement data show a significantly higher device temperature for the 8-finger device. This is due to a thermal crosstalk between the gate fingers. Each gate finger acts as a single heat source giving an additional temperature rise to its neighbours because of the overlapping temperature profiles in the bulk semiconductor material. As this is an accumulative process with the number of gate fingers, the measured device temperature is higher for a higher number of fingers. However, the more striking observation from these measurement results is the difference in device temperature with applied drain voltage at constant dissipated power level. In the subsection before, we stated that the thermal resistance R_{th} is constant due to a linear approximation of the superlinear relation between device temperature and dissipated power. Therefore, we expect no dependence of R_{th} on any electrical parameter. Now, from Fig. 4.30 the thermal resistance seems to be dependent on the applied drain voltage. For further investigation of this effect, the device temperature has been simulated for various dissipated power densities at fixed

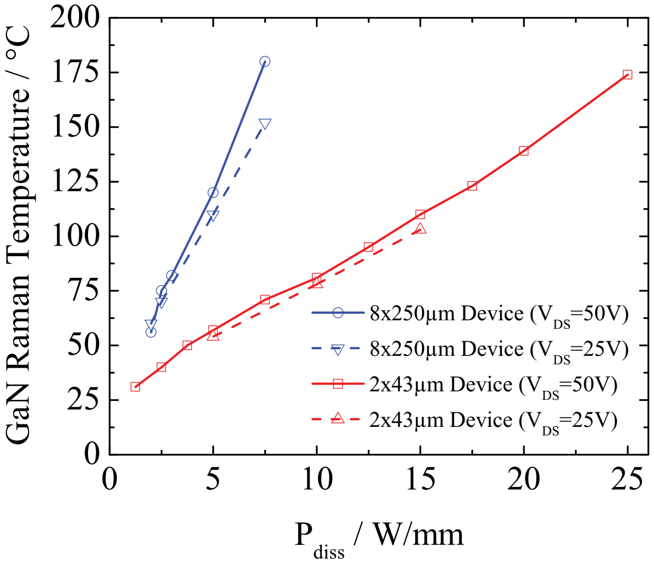
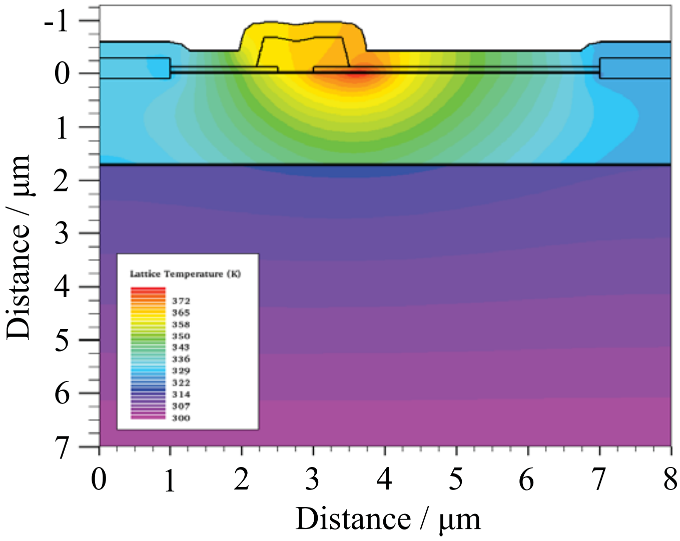
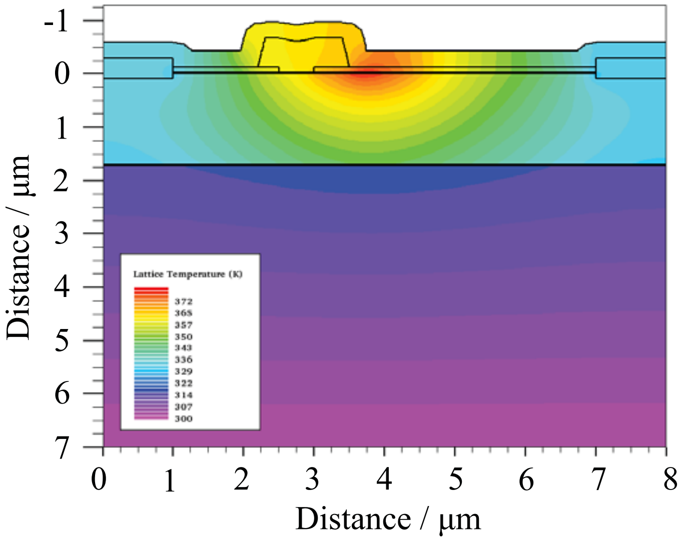


Figure 4.30: Results of micro-Raman thermography measurements on an 8 x 250 μm and a 2 x 43 μm device for drain voltages of $V_{\mathrm{DS}} = 25\,\mathrm{V}$ and $V_{\mathrm{DS}} = 50\,\mathrm{V}$.

drain voltages of $V_{\mathrm{DS}} = 25\,\mathrm{V}$ and $V_{\mathrm{DS}} = 50\,\mathrm{V}$ exactly as in the experiment and the simulation results will be compared to see if the physical electro-thermal model reproduces the same effect. Fig. 4.31 shows two-dimensional temperature maps at same dissipated power density for both drain voltages. From this simulation data, we now extract the horizontal temperature profile in the channel of the device and at a depth of 1 μm in the GaN buffer layer where the Raman signal is detected. The extracted temperature profile is plotted in Fig. 4.32. The data shows that the maximum junction temperature in the device is the same for both drain voltages meaning that the junction temperature of the device is just determined by the dissipated power density and so the thermal resistance is not a function of the applied drain voltage. However, when we extract the temperature at a distance of 4 μm and at a depth of 1 μm in the GaN buffer layer we find the local temperature at $V_{\mathrm{DS}} = 25\,\mathrm{V}$ to be 10 % lower than the temperature at $V_{\mathrm{DS}} = 50\,\mathrm{V}$ as we also found in the experiment. This means that the lower Raman temperature in the experiment is just a consequence of the location were the Raman temperature is taken because at $V_{\mathrm{DS}} = 50\,\mathrm{V}$ the temperature profile in the device is broader and the device hot-spot is shifted towards the drain contact with higher drain voltage. The higher V_{DS}, furthermore, indicates that the externally applied electric field is the reason for the observed broadening and the shift of the temperature profile.



(a) Simulated two-dimenaional temperature map for a dissipated power density of $P_{\text{diss}} = 13.5\,\text{W}/\text{mm}$ at $V_{\text{DS}} = 25\,\text{V}$.



(b) Simulated two-dimenaional temperature map for a dissipated power density of $P_{\text{diss}} = 13.5\,\text{W}/\text{mm}$ at $V_{\text{DS}} = 50\,\text{V}$.

Figure 4.31: Comparison of the simulated temperature maps for constant dissipated power density at two different drain voltages.

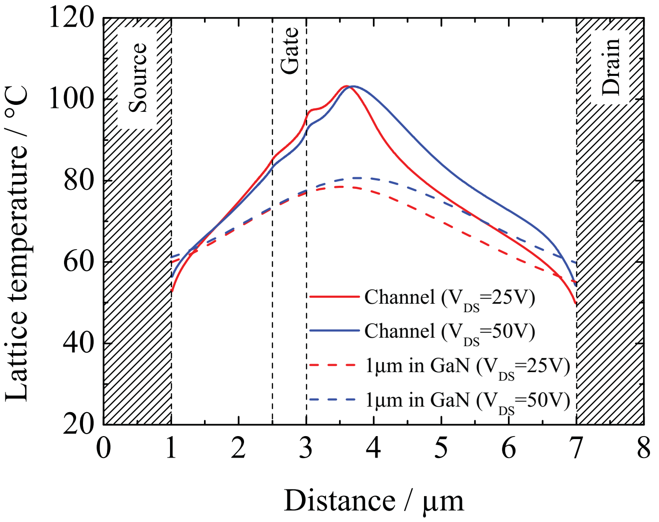
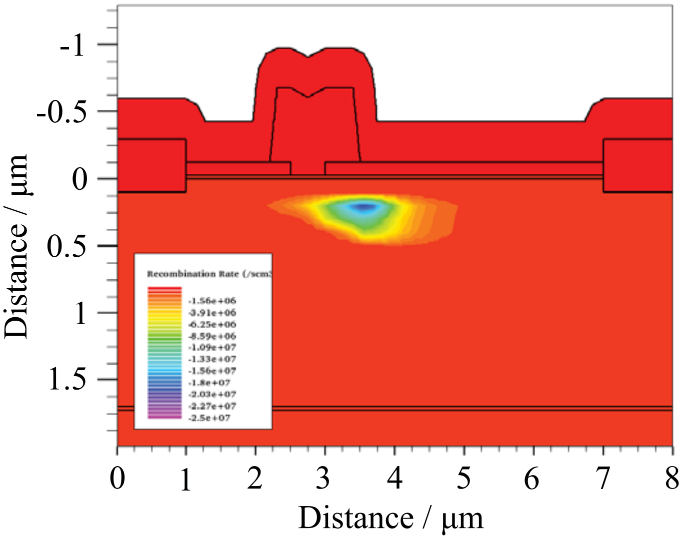


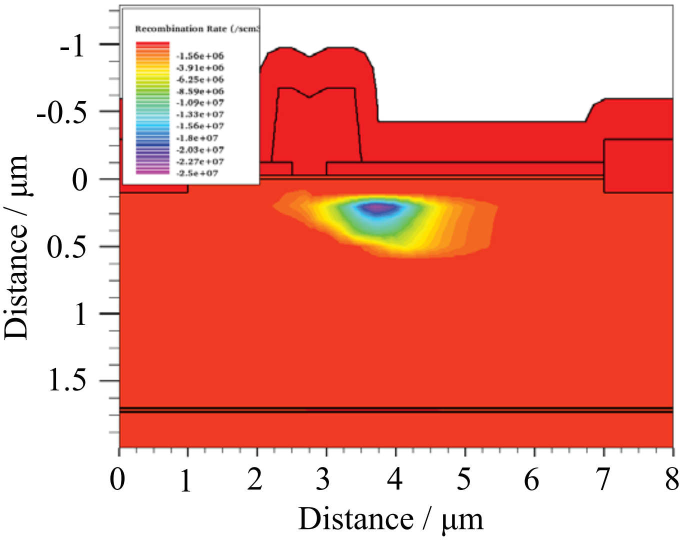
Figure 4.32: Horizontal temperature profile in the channel of the device and at a depth of 1 μm in the GaN buffer layer for drain voltages of $V_{DS} = 25\,V$ and $V_{DS} = 50\,V$.

After further analysis of the simulation data we find the reason for the broadening of the temperature profile to be related to recombination processes in the device. In Fig. 4.33 two-dimensional maps of the recombination rate of the free charge carriers is shown for both applied drain voltages at constant dissipated power density. It can be seen from this figure, that the extension of the region for high recombination is larger at $V_{DS} = 50\,V$ compared to $V_{DS} = 25\,V$. Also the maximum recombination rate increases with increasing V_{DS}. This fact leads to a higher recombination of hot electrons in the gate-drain region which are generated under these high field conditions. Each recombination process of hot electrons, furthermore, generates a single phonon so that an additional temperature rise in the gate-drain region is observed which leads to a broadening of the temperature profile at higher V_{DS}.

The analysis of the simulation data also shows, that the shift of the hot-spot in the device towards the drain contact again is a consequence of the externally applied electric field because the point of maximum electric field shifts in the same way as the hot-spot. This shift, however, can be influenced by the assumed density of surface states n_{st} at the semiconductor-passivation interface. The simulated dependence of the hot-spot position on the assumed density of surface states is depicted in Fig. 4.34. The data show that the sensitivity on the drain voltage increases when the surface state density is decreased. Furthermore, it can be noticed that the Γ-gate overhang has an effect on the hot-spot shift in a way that it causes an additional reduction of the sensitivity. Due to this, we can conclude that the dominating region is below the Γ-gate overhang. The variation



(a) Simulated two-dimensional map of the recombination rate for a dissipated power density of $P_{\mathrm{diss}} = 13.5\,\mathrm{W/mm}$ at $V_{\mathrm{DS}} = 25\,\mathrm{V}$.



(b) Simulated two-dimensional map of the recombination rate for a dissipated power density of $P_{\mathrm{diss}} = 13.5\,\mathrm{W/mm}$ at $V_{\mathrm{DS}} = 50\,\mathrm{V}$.

Figure 4.33: Comparison of the simulated map of the recombination rate for constant dissipated power density at two different drain voltages.

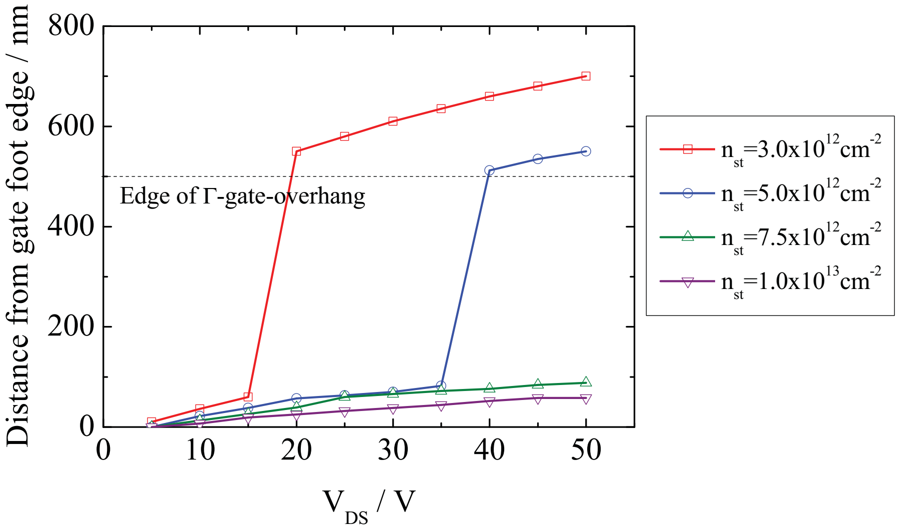
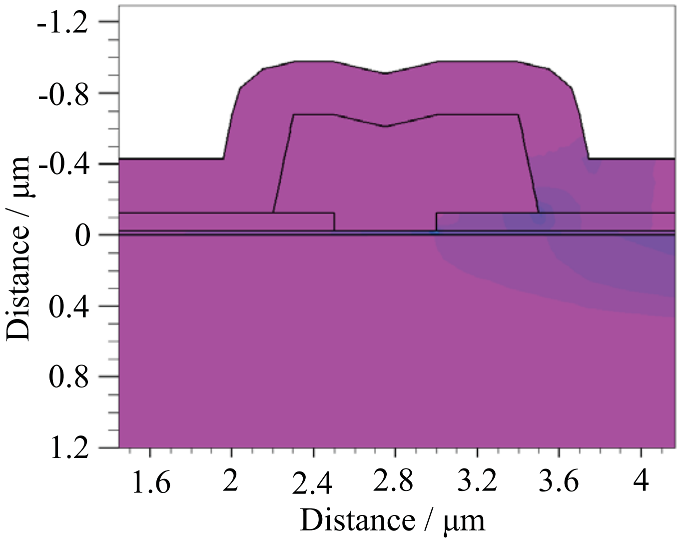
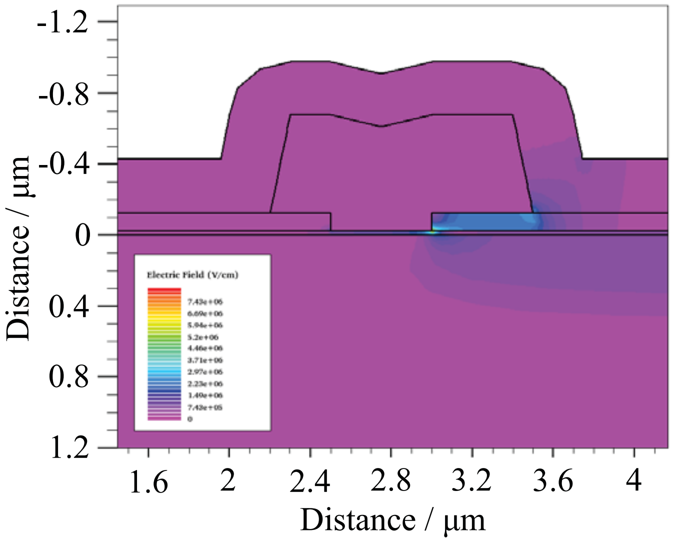


Figure 4.34: Simulated dependence of the hot-spot position on the assumed density of surface states n_{st} versus applied drain voltage.

of the surface state density modifies the surface potential and changes the electric field below the Γ-gate overhang because of the small gap between gate head and semiconductor surface. The surface potential increases with increasing n_{st} so that the electric field below the gate head is also increased. This leads to a stronger localization of the maximum electric field at the gate contact and reduces therefore the shift of the electric field peak and, thus, the shift of the hot-spot. The increase in electric field with increasing n_{st} can be seen in Fig. 4.35. If we take the results of the investigations from [57–59] and section 4.1 into account, in the end, we can conclude that devices with a reasonably good passivation and, thus, low surface state density and low current collapse, will always observe such a shift of the electric field peak and thermal hot-spot with increasing V_{DS}, since surface state densities in the range of $n_{\mathrm{st}} = 1 \cdot 10^{13}\,\mathrm{cm}^{-2}$ are typically observed in non-passivated devices. This should be taken into account when performing thermal characterization at different drain voltages using techniques with a spacial resolution comparable to that of micro-Raman thermography.



(a) Electric field distribution for a surface state density of $n_{\text{st}} = 3 \cdot 10^{12}\,\text{cm}^{-2}$.



(b) Electric field distribution for a surface state density of $n_{\text{st}} = 1 \cdot 10^{13}\,\text{cm}^{-2}$.

Figure 4.35: Comparison of the electric field distribution in the gate region for a low and high surface state density.

Chapter 5

Technology Aspects for RF Performance Improvement

THIS chapter deals with the study of technological issues impacting the RF performance of AlGaN/GaN HEMTs. First, the impact of layout changes on RF gain is assessed through simulations. After that, the most promising variations have been realized experimentally and the characterization results are presented. Finally, some limiting issues will be discussed.

5.1 Simulation Study

In this simulation study the impact of layout changes on the current gain $|H_{21}|$, the power gain (MSG and MAG) is studied. All simulations have been performed at a bias condition of $V_{\mathrm{DS}} = 30\,\mathrm{V}$ and $I_{\mathrm{DS}} = 300\,\mathrm{mA/mm}$. Layout changes studied are mainly related to the gate module where the thicknesses of the two passivation layers is changed in order to influence the parasitic capacitances in the device. The study is performed on a device structure with a gate length of $L_{\mathrm{G}} = 250\,\mathrm{nm}$ and a *source-terminated field-plate* (STFP).

Of course, the first layout change of choice when aiming for an increase in RF gain is the reduction of the gate length of the device. However, there are two reasons in this case not to follow that option. In Fig. 5.1 a comparison between the reference and a reduced gate length of $L_{\mathrm{G}} = 150\,\mathrm{nm}$ is plotted. It can be seen from the simulation that the benefit from the reduced gate length is just visible in the current gain of the device. According to equation (5.1) it can be concluded that the increase in transit frequency f_{T} is on the one hand due to an increase in the transconductance g_{m}.

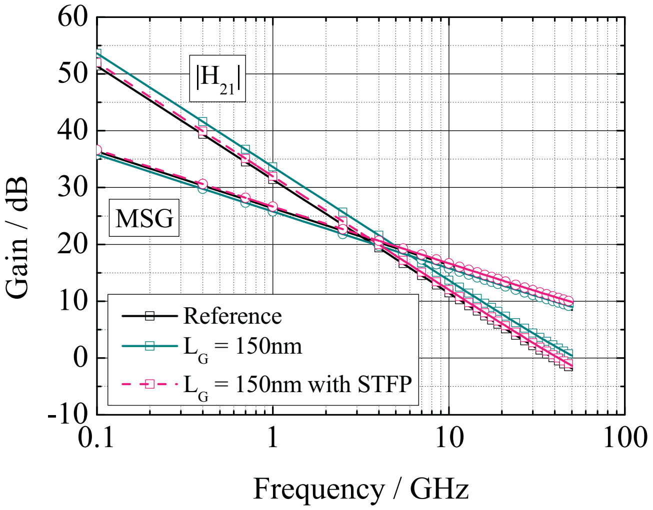


Figure 5.1: Simulation result on the impact of reduced gate length on RF gain at $V_{\mathrm{DS}} = 30\,\mathrm{V}$ and $I_{\mathrm{DS}} = 300\,\mathrm{mA/mm}$.

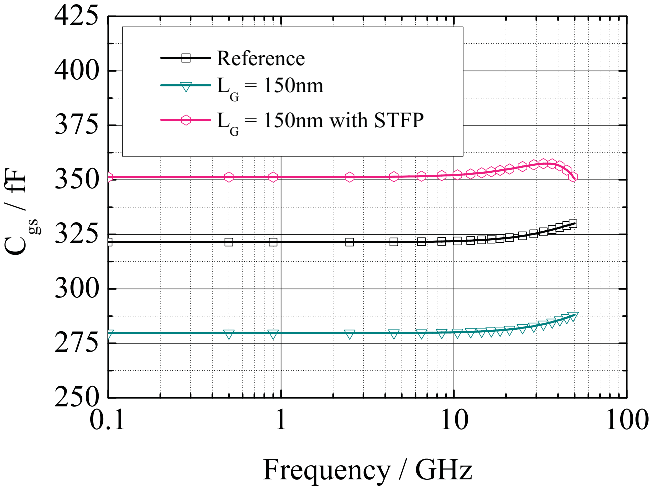


Figure 5.2: Simulation result on the impact of reduced gate length on C_{gs} at $V_{\mathrm{DS}} = 30\,\mathrm{V}$ and $I_{\mathrm{DS}} = 300\,\mathrm{mA/mm}$.

However, due to the fact that the STFP is compensating for the increase in f_T it can be seen that the small-signal capacitance C_gs is influenced.

$$f_\mathrm{T} = \frac{g_\mathrm{m}}{2\pi C_\mathrm{gs}} \tag{5.1}$$

The impact of the gate length reduction can be seen in Fig. 5.2. It needs to be mentioned that the seen frequency dependence in this and all following capacitance related figures is a consequence of the applied small-signal model. At higher frequency distribution effects become dominant which are not covered by a model assuming lumped elements. Therefore the frequency dependence of the capacitances is artificial and can therefore be neglected. The simulation results show, on the other hand, no change in MSG which is the better measure for power amplification. Moreover, a reduced gate length yields always a reduction in breakdown voltage of a device since short channel effects will become more and more pronounced and for the same external biasing internal electric field become higher at the gate contact due to the smaller gated area. Both facts imply that this option is not feasible for a high-power device in X-band but could be of interest for higher frequency bands.

The next logical step is then to focus on the small-signal capacitances C_gs and C_gd in the device. The most important role is due to the feedback capacitance C_gd. To assess this by means of device simulations the gate length was kept constant and the thicknesses of the SiN layers as well as the layout of the STFP have been varied on order to change the parasitic capacitances. The respectively change SiN layers are schematically indicated in Fig. 5.3. A summary of the simulation results is shown in Fig. 5.4. It can be seen that the strongest positive impact on the MSG/MAG is due to the reduction of the SiN layer thickness in combination with a STFP. Due to the reduced distance between the STFP and the Γ-gate contact the feedback capacitance is reduced at the expense of an increased input capacitance. This becomes clear when extracting the small-signal capacitances from the simulated S-parameters. The extracted values are plotted in Fig. 5.5 and 5.6. For completeness, in Fig. 5.7 also the output capacitance is plotted. However, this parameter is not further analyzed in this work although it is an important parameter for the design of broad-band power amplifiers. From the simulation results we can expect an increase in MSG by approx. $+1.4\,\mathrm{dB}$ for the combination of 100 nm Gate-SiN and 200 nm STFP-SiN and by approx. $+2.3\,\mathrm{dB}$ for the combination of 50 nm Gate-SiN and 200 nm STFP-SiN compared to the Reference of 100 nm Gate-SiN and 300 nm STFP-SiN. It has to be mentioned that this modification is only beneficial for a device with STFP. For a device without STFP this would reduce the gain due to an increase in C_gd as can be also seen in Fig. 5.6.

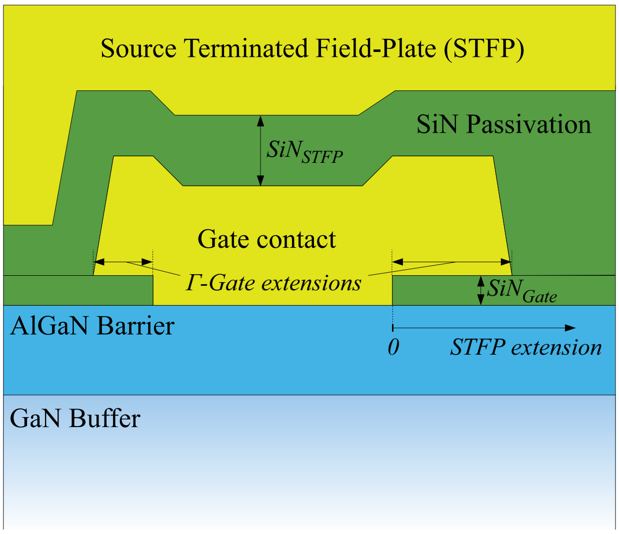


Figure 5.3: Illustration of geometries to be changed in the simulation study.

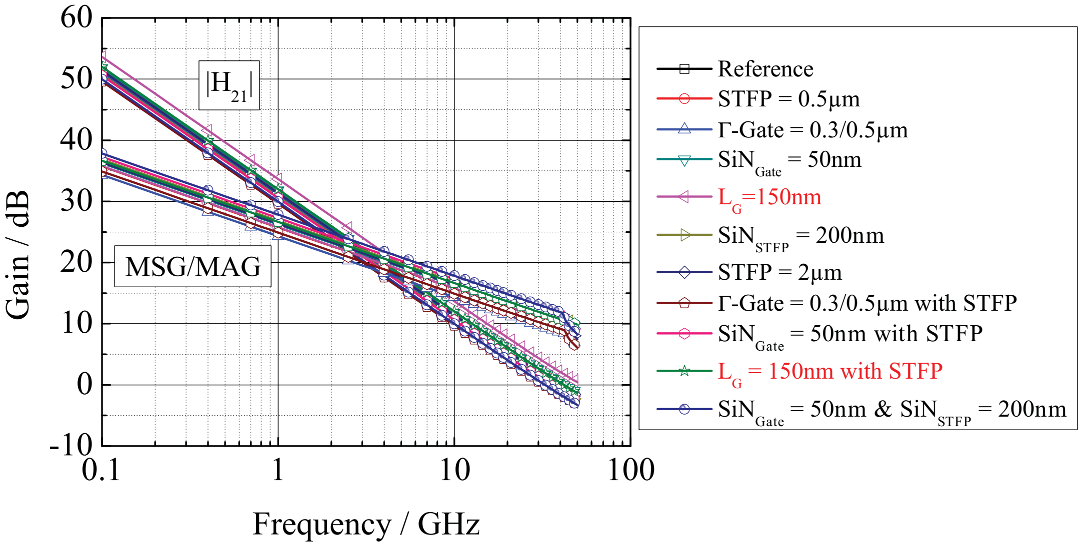


Figure 5.4: Simulation results on the impact of SiN variation and layout changes on RF gain at $V_{DS} = 30\,\text{V}$ and $I_{DS} = 300\,\text{mA/mm}$.

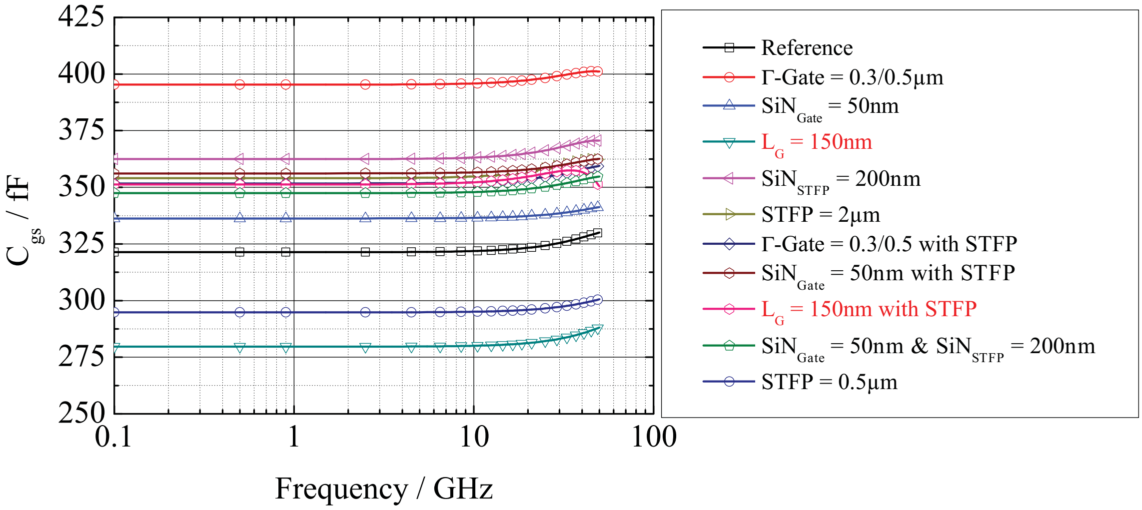


Figure 5.5: Simulation results on the impact of SiN variation and layout changes on C_{gs} at $V_{DS} = 30\,\text{V}$ and $I_{DS} = 300\,\text{mA/mm}$.

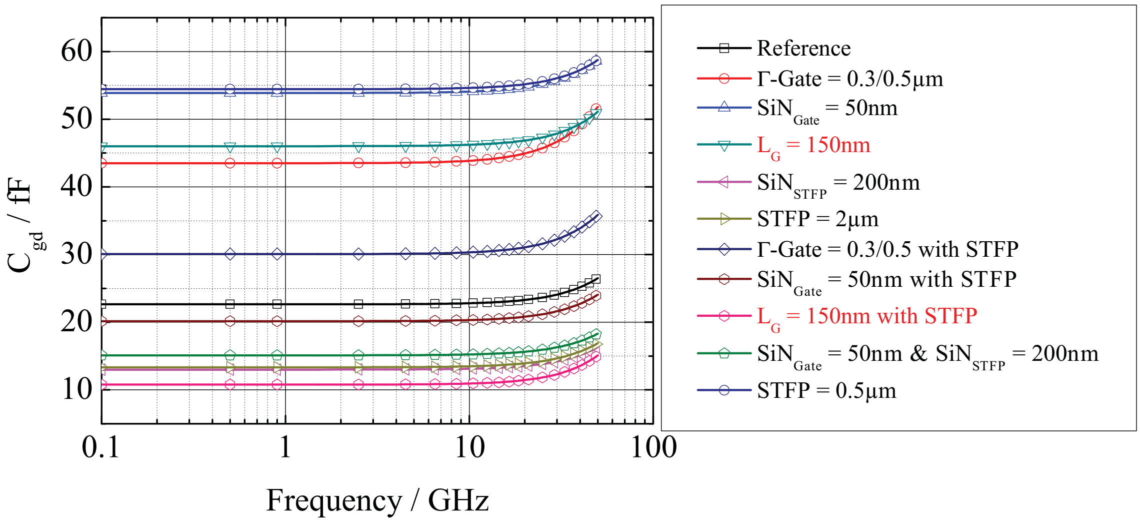


Figure 5.6: Simulation results on the impact of SiN variation and layout changes on C_{gd} at $V_{DS} = 30\,\text{V}$ and $I_{DS} = 300\,\text{mA/mm}$.

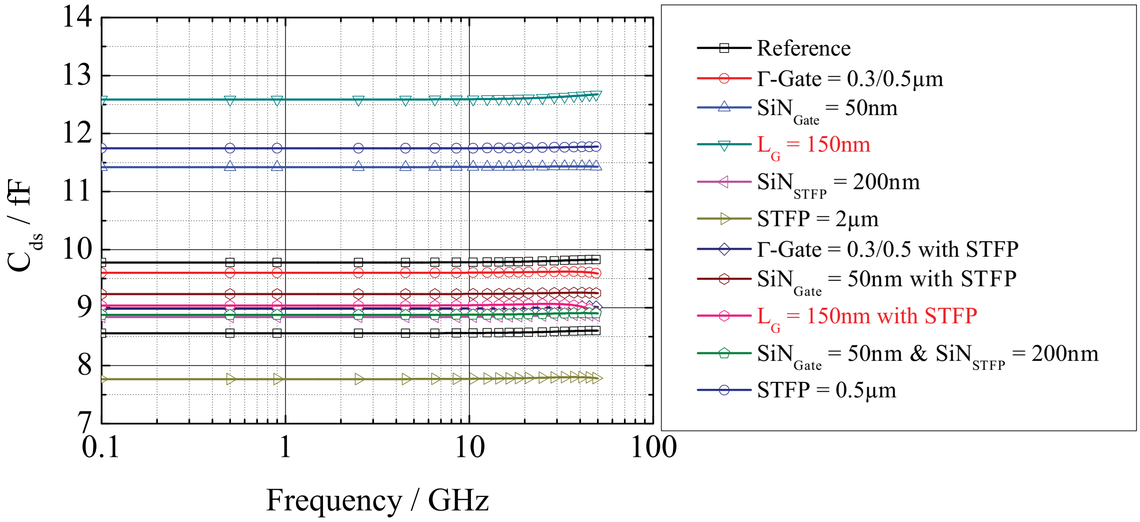


Figure 5.7: Simulation results on the impact of SiN variation and layout changes on C_{ds} at $V_{DS} = 30\,V$ and $I_{DS} = 300\,mA/mm$.

5.2 Experimental Results

In order to validate the simulation results, devices were processed with a variety of different SiN layer thicknesses. However, it needs to be mentioned that the epitaxial HEMT structures used had a higher sheet carrier density n_S than initially assumed in the simulations. After processing, these devices have been characterized by S-parameter measurements at $I_{DS} = 300\,mA/mm$ and $V_{DS} = 5\ldots40\,V$. The measurement results are depicted in Fig. 5.8. The results show that the general trend seen in the simulations is present. The importance of the presence of a STFP is also visible in the measurement data since the gain improvement becomes more with increasing V_{DS} which is an indication for the effectivity of the STFP. However, the absolute gain improvement of just $+0.7\,dB$ seems to be disappointing, but this can be explained.

5.3 Limitations

For a better understanding of the disappointing results in the previous section it is necessary to analyze the shape of the gate contact. In Fig. 5.9 a SEM picture of part of the gate contact is depicted. It can be seen that both sides of the gate head line are seamed by gate metal fringes. These fringes are most likely generated during the lift off process. These metal fringes lead to

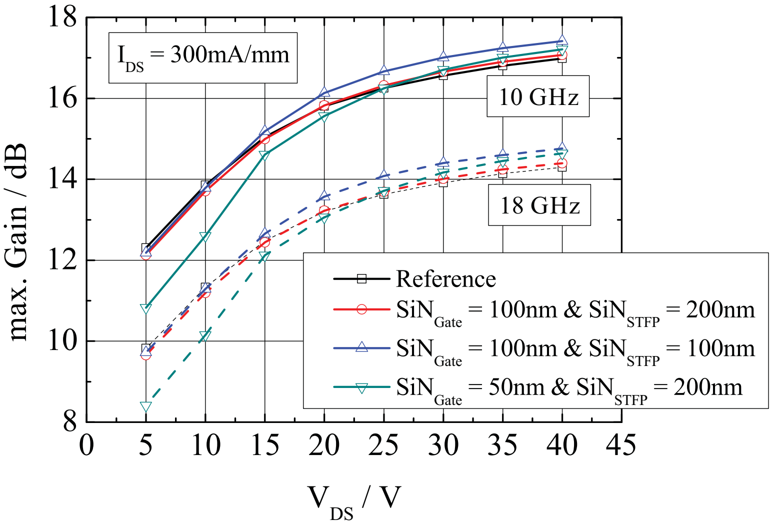


Figure 5.8: MSG at 10 GHz and MAG at 18 GHz extracted from S-parameter measurements performed on devices processed with different SiN layer thicknesses at $I_{DS} = 300\,\mathrm{mA/mm}$ and various V_{DS}.

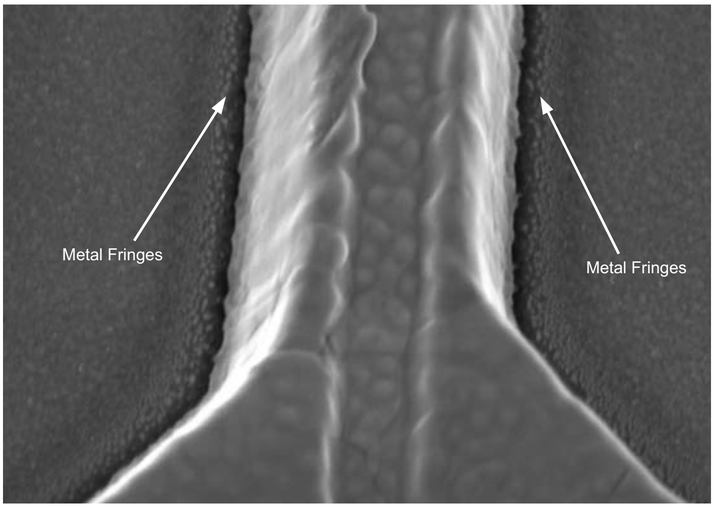


Figure 5.9: SEM picture of the gate contact showing metal fringes on both sides of the gate head line.

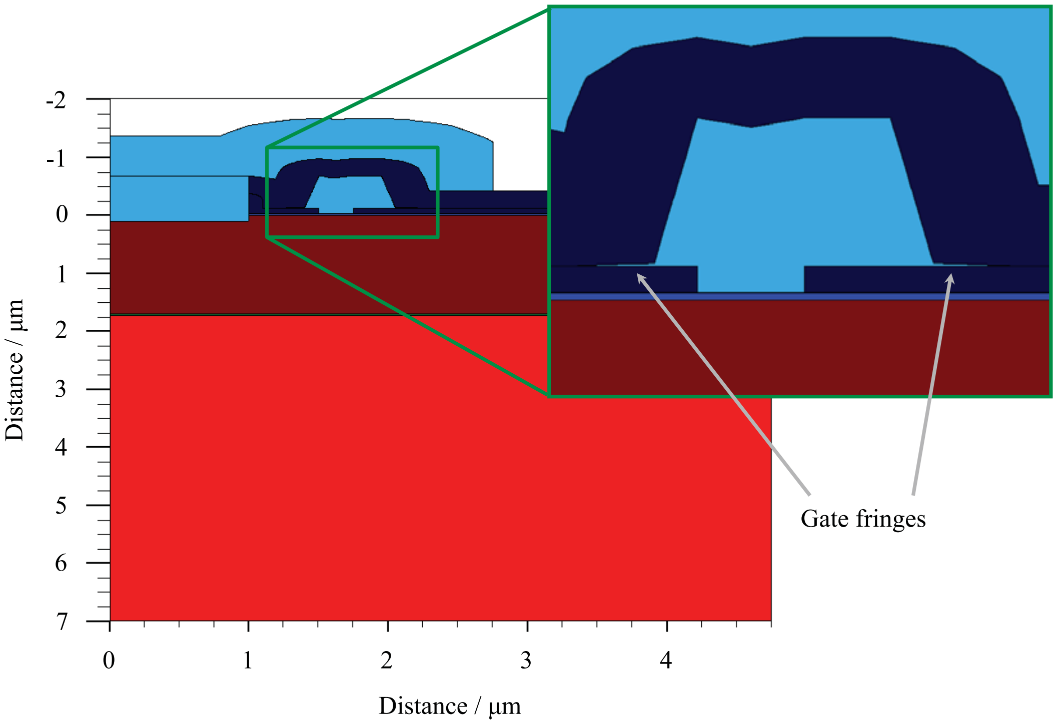


Figure 5.10: Simulation structure including gate metal fringes.

an increase of the gate head size and thus increase the feedback capacitances. This fact has been published in [81]. In another simulation, the fringes have been accounted for as shown in Fig. 5.10. With this structure the small-signal gain has been re-simulated using the characterized SiN layer thicknesses. The simulation results shown in Fig. 5.11 indicate that due to the presence of these gate metal fringes the margin of gain improvement by SiN layer thickness reduction is reduced by approx. 1 dB. Taking an additional uncertainty of the simulation model into account, it can be concluded that the very low gain improvement achieved in the previous section can be explained by this technological root cause.

The next step would now be to find a process that is capable to remove those fringes successfully in order to further improve the small signal RF gain of the devices. An Argon-milling step right after the lift-off process of the gate metal [81], however, showed very promising preliminary results as depicted in Fig. 5.12.

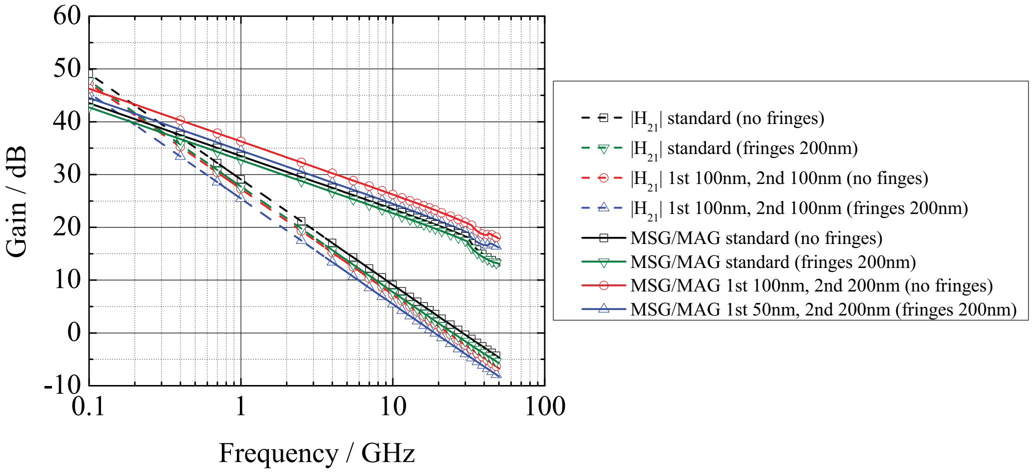


Figure 5.11: Simulation results on the impact of gate metal fringes on gain margin at $V_{\mathrm{DS}} = 30\,\mathrm{V}$ and $I_{\mathrm{DS}} = 300\,\mathrm{mA/mm}$.

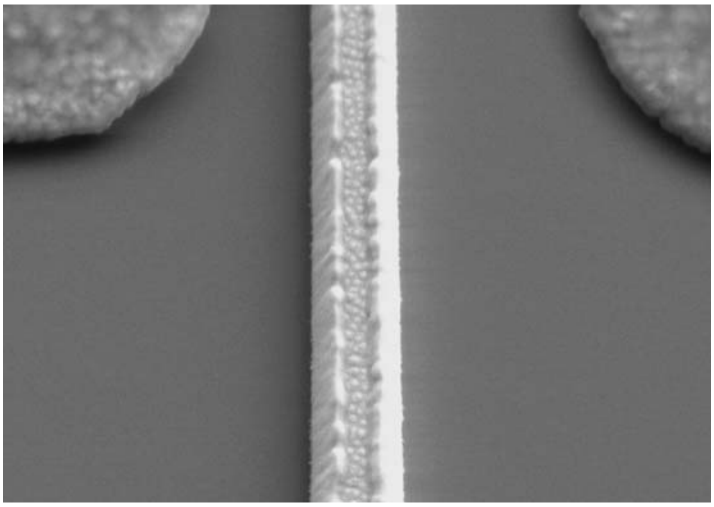


Figure 5.12: SEM picture of the gate contact after Argon-milling showing no metal fringes on either sides of the gate head line.

Chapter 6

Summary and Conclusion

Since several years now AlGaN/GaN HEMTs have attracted much attention in research and development especially for high-power RF and microwave applications. The main material parameters and related figures of merit have been discussed and calculated in chapter 2. It has been shown that GaN offers outstanding material properties leading to a predominant material system for discrete devices and MMICs for high-power high-frequency applications.

This work aimed to support and improve the understanding of AlGaN/GaN HEMTs in terms of non-ideal effects and operation. As these effects require a deep look into the physics of semiconductor heterostructures, a 2-dimensional device simulation tool was used to develop a model for the investigated HEMT structures in order to investigate effects observed by different characterization techniques. To provide the basic operation principle of AlGaN/GaN HEMTs, in the first part of chapter 3 some simple theoretical calculations of the I-V characteristics have been carried out. These calculations show mainly the strong influence of epitaxial properties among which the high polarization of the group-III-nitrides is the main characteristic in the device operation principle. Based on these results, in the second part of the chapter, physical models have been developed for three different operation regimes. It turned out that it is very important to carefully model the surface and interfaces of the epitaxial structure since those charges placed there have strong impact on the electric field distribution and therefore on the I-V characteristics of the simulated device. Therefore, the following modelling scheme has been applied:

- Use layout geometries as close as possible to the real device in order to achieve a realistic field distribution.
- Use the polarization charge to fit the sheet charge density n_S and the threshold voltage V_th.

- Use the donor-like surface traps density and the drift saturation velocity of electrons to fit the drain saturation current I_{DSS}.
- Use the location of the thermal contact in the substrate to fit the measured device temperature in on-state.
- Use an donor-like trap density below the gate and fixed charges in the device passivation to fit the two-terminal and three-terminal leakage currents of the device in off-state.

The electro-thermal model has been developed for the investigation of the on-state operation of the devices. For the off-state operation a sub-threshold model has been developed used for the investigation of leakage currents. The RF operation is covered by an RF model capable to simulate the device operation under small-signal RF excitation. This model is mainly used for the investigation and improvement of the RF gain of the devices.
Chaper 4 then dealt with non-idealities in the device which have severe impact on the device performance. First, the well-known effect of dispersion or current collapse has been discussed. This effect is one of the major limitations of RF power performance. Investigations by device simulations show that traps at the surface are ionized during operation. These ionized traps act as a virtual gate which depletes the 2DEG leading to a reduction in drain current by an increase in drain resistance R_{D}. Low-frequency s-parameter measurements have been used to characterize the transconductance dispersion and a time constant of the trapping phenomena in the nanosecond regime has been derived. Since the two-tone linearity is directly linked to the transconductance of a device, it was shown that also two-tone linearity measurements on device level exhibit a dispersive characteristic with nearly the same time constant as the transconductance dispersion. This fact implies that the current collapse itself has also severe impact on the two-tone linearity. Another trap related effect, as it turned out in this chapter, is device leakage. Device simulations showed that these traps are located below the gate. For the reproduction of the measured two-terminal diode leakage current a significant trap density of the order of $10^{19}\,\mathrm{cm}^{-3}$ was determined. However, the pure assumption of traps below the gate contact was not sufficient to reproduce the three-terminal transistor leakage. Experiments showed a strong impact of the passivation layer on the level of leakage. Further simulation studies indicated that due to the variation in deposition techniques and processing parameters the amount of charges in the dielectric layer must have changed. These charges influence the electric field especially in the gate region which has furthermore strong impact on the leakage current. Using C-V measurements on large area MISFETs and FATFETs these charges have been analyzed. According to this investigations, the charges impacting the device leakage are located very close to the semiconductor

surface. Therefore, the first seconds of the passivation deposition are the crucial step in the device processing regarding device leakage.

A more indirect effect of traps can be seen experimentally on the self-heating of those devices under on-state operation. Micro-Raman thermography measurement show a difference in device temperature of approximately 10 % at the same dissipated power density but at different drain voltages implying a bias dependence of the thermal resistance of those devices. This effect again has been investigated by device simulations. These simulations show a shift of the electric field peak in the device with increasing drain voltage away from to gate towards the drain contact. Furthermore, the recombination rate and the related recombination region is increased leading to an additional temperature rise. Traps at the surface, however, influence the field peak shift in a way that with increasing trap density the electric field peak shift is less sensitive to the drain voltage.

Taking all discussed trap related effects into account, we can conclude that the passivation layer of the device is one of the most crucial processing steps during device manufacturing. The optimization of this passivation layer is always a trade-off between device leakage and current collapse since a high charge density in the dielectric is beneficial for the current collapse due to the compensation of traps with different polarity but leads on the other hand to an increased leakage current. A possible way to go in the future could be a multi-layer approach giving the best trade-off between dispersion and leakage current due to the opportunity to engineer the charge distribution in order to optimize the device performance.

The last chapter of this thesis dealt with the optimization of the device performance with respect to the RF gain of the device. The basis for the RF gain improvement provided a simulation study where the device layout was changed and the response of the MSG/MAG on these variations has been extracted from the simulated small-signal parameters. It turned out during this study that the intrinsic small-signal capacitances of the device are the key parameters for gain improvement. However, there is also a drawback of this way of gain improvement due the fact that the optimum layout of the device is different for a device with and without STFP. For a device with STFP it is necessary to put the STFP as close to the gate head as possible by reducing the thickness of the second passivation layer which lies in between. This leads to a change in the capacitance distribution in a way that the gate-drain capacitance is reduced whereas the gate-source capacitance is increased at the same time. For devices without STFP, on the other hand, the thickness of the second SiN layer has obviously no impact on the capacitances. Here, one needs to focus on the first SiN layer thickness. This thickness needs to be increased to reduce the gate-drain capacitance. However, this leads to a reduction of the gain for a device with STFP since the impact of

Layout Change	**C_{gs}**		**C_{gd}**		**MSG/MAG**	
Device	STFP	no STFP	STFP	no STFP	STFP	no STFP
first SiN thickness reduced	↑	↑	↓	↑	↑	↓
second SiN thickness reduced	↑	-	↓	-	↑	-
gate length reduced	↑	↓	↓	↑	↔	↔
STFP length reduced	↓	-	↑	-	↑	-
STFP length increase	↑	-	↓	-	↓	-
Γ-Gate dimension increased	↑	↑	↑	↑	↓	↓

Table 6.1: Qualitative change in RF parameters due to layout changes in the device.

the STFP on the electric field distribution and therefore on the capacitances is reduced due to the increased distance to the semiconductor surface. A summary of the qualitative changes in RF parameters due to layout changes in the device is compiled in table 6.1. The simulated increase of the RF gain by $+2.3\,\mathrm{dB}$ resulted in an experimental value of $+0.7\,\mathrm{dB}$. Further investigations showed that due to the processing of the device metal fringes are located at both sides of the gate head. Simulations showed that these fringes are responsible for the small gain improvement since they reduce the margin of gain improvement with increasing lateral extension. This fact gives rise to the need for the future to properly control the gate contact processing or to introduce a processing step in order to remove the metal fringes.

To conclude this thesis, it is worth mentioning that AlGaN/GaN HEMT devices are very interesting devices from a scientific point of view like the content of this thesis has shown and there is still a lot work to be done in order to fully understand the device physics and in the end drive the development of this technology to an industrial level. The real scientific challenge, however, is to find out which among all the well-known effects in a HEMT device is dominating the device performance of an AlGaN/GaN HEMT in order to optimize the device. To this end well established techniques of investigation are perfectly suited and should be preferred since these techniques are well understood and, thus, minimize characterization uncertainties. Eliminating characterization uncertainties increases the confidence level of achieved experimental results and enhances therefore the research and development process of new technologies like AlGaN/GaN HEMTs.

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Appendix A

List of Acronyms and Symbols

Acronyms

Acronym	**Name**
HEMT	High Electron Mobility Transistor
MODFET	Modulation Doped Field Effect Transistor
MESFET	Metal Semiconductor Field Effect Transistor
FET	Field Effect Transistor
HBT	Heterojunction-Bipolartransistor
MMIC	Monolithic Microwave Integrated Circuit
Si	Silicon
SiGe	Silicon-Germanium
GaAs	Gallium Arsenide
InP	Indium Phosphide
GaN	Gallium Nitride
InN	Indium Nitride
AlN	Aluminum Nitride
SiC	Silicon Carbide
Al_2O_3	Sapphire
SiN	Silicon Nitride
Ni	Nickel
Au	Gold
FCC	face-centered-cubic

Acronym	Name
2DEG	2-dimensional electron gas
JFOM	Johnson's Figure of Merit
KFOM	Keyes's Figure of Merit
BFOM	Baliga's Figure of Merit
BHFFOM	Baliga's High-Frequency Figure of Merit
TCAD	Technology Computer-Aided Design
DLTS	Deep-Level Transient Spectroscopy
MOCVD	Metal-Organic Chemical Vapor Deposition
TDRC	Temperature-Dependent Relaxation Current
STFP	Source-Terminated Field-Plate

Symbols

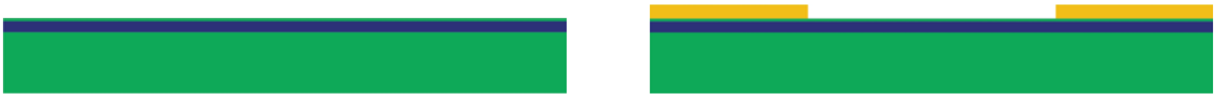
Symbol	Name	Unit
E_{G}	Band gap	eV
χ	Electron affinity	eV
N_{C}	Effective conduction band density of states	cm^{-3}
N_{V}	Effective valence band density of states	cm^{-3}
E_{B}	Electric breakdown field	$\mathrm{V} \cdot \mathrm{cm}^{-1}$
v_{sat}	Drift saturation velocity	$\mathrm{m} \cdot \mathrm{s}^{-1}$
μ	Low-field charge carrier mobility	$\mathrm{cm}^2 \cdot \mathrm{V}^{-1} \cdot \mathrm{s}^{-1}$
ε	Permittivity	1
σ_{th}	Thermal conductivity	$\mathrm{W} \cdot \mathrm{cm}^{-1} \cdot \mathrm{K}^{-1}$
P^{sp}	Spontaneous polarization charge	$\mathrm{C} \cdot \mathrm{m}^{-2}$
P^{pe}	Piezoelectric polarization charge	$\mathrm{C} \cdot \mathrm{m}^{-2}$
σ	Polarization induced net charge	$\mathrm{C} \cdot \mathrm{m}^{-2}$
n_{S}	Sheet charge density	cm^{-2}
V_{p}	Pinch-off voltage	V
ϕ_{b}	Schottky barrier hight	eV
ΔE_{C}	Conduction band discontinuity	eV
N_{D}	Donor doping concentration	cm^{-3}
V_{GS}	Gate-Source voltage	V

Symbol	**Name**	**Unit**
V_{DS}	Drain-Source voltage	V
I_{D}	Drain current	A
$\mathscr{E}_{\mathrm{crit}}$	Electric field at the onset of drift saturation	$\mathrm{V \cdot m^{-1}}$
W_{G}	Gate width	mm
L_{G}	Gate length	nm
n_{st}	Surface trap density	$\mathrm{cm^{-2}}$
CC_{G}	Gate-related current collapse	%
CC_{D}	Drain-related current collapse	%
N_{DT}	Donor-like trap density (volume charge)	$\mathrm{cm^{-3}}$
n_{DT}	Donor-like trap density (sheet charge)	$\mathrm{cm^{-2}}$
n_{AT}	Acceptor-like trap density (sheet charge)	$\mathrm{cm^{-2}}$
$L_{\mathrm{G,virt}}$	Virtual gate length	nm
Q_{SiN}	Passivation charge density	$\mathrm{cm^{-3}}$
MSG	Maximum Stable Gain	dB
MAG	Maximum Available Gain	dB
k	Rollet's Stability Factor	1

Appendix B

Process Sequence

On the following page the process sequence of the fabrication of the active device is schematically shown.

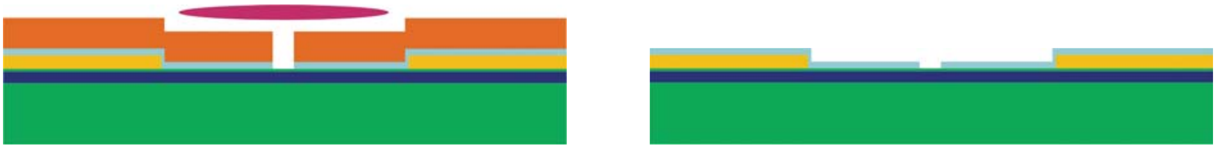


(a) Bare epitaxial wafer.

(b) Formation of the ohmic contacts by lift-off technique and rapid thermal anneal.

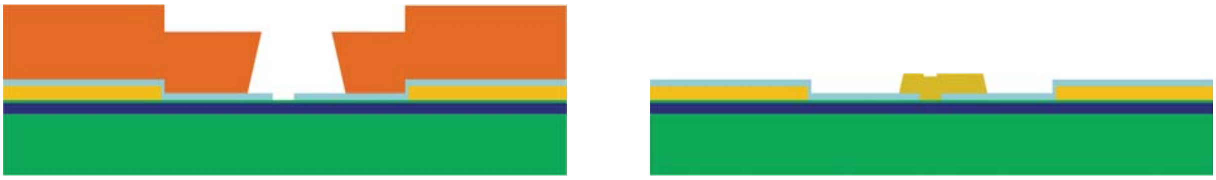
(c) Deposition of SiN passivation layer.

(d) E-beam lithography of the gate foot.



(e) Dry eching of the gate foot trench.

(f) removalmof the E-beam resist.



(g) E-beam lithography of the gate head.

(h) Gate metal evaporation and lift-off of the gate contact and end of the process.

Figure B.1: Schematic process flow of the fabrication of the AlGaN/GaN transistor.

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