Leibniz Ferdinand Braun Institut

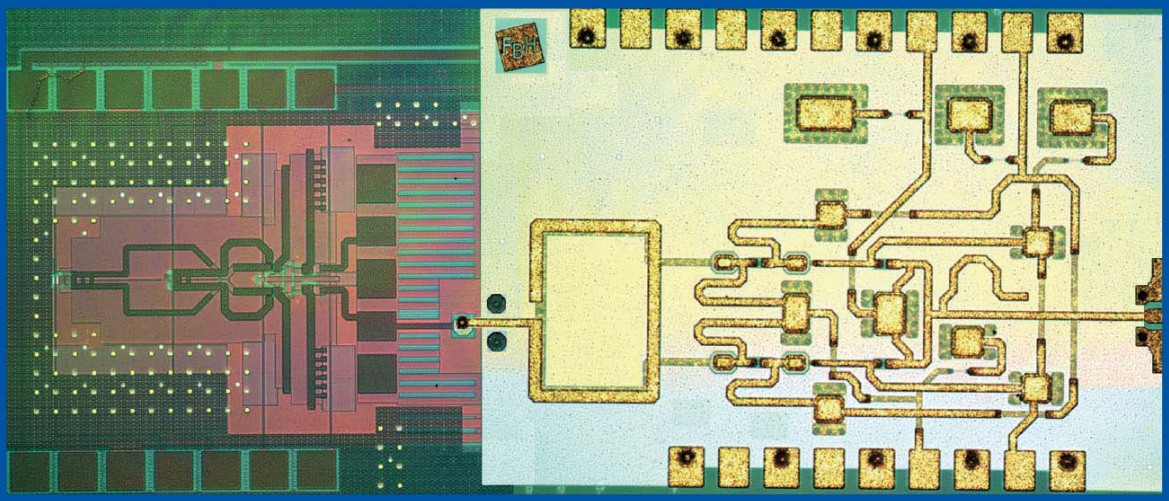
37

Innovationen mit Mikrowellen & Licht

Forschungsberichte aus dem

Ferdinand-Braun-Institut,
Leibniz-Institut
für Höchstfrequenztechnik

Signal Generation for Millimeter Wave and THz Applications in InP-DHBT and InP-on-BiCMOS Technologies



Muhammad Maruf Hossain

aus der Reihe:

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Signal Generation for Millimeter Wave and THZ Applications in InP-DHBT and InP-on-BiCMOS Technologies

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Innovations with Microwaves and Light

Research Reports from the Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik

Preface of the Editors

Research-based ideas, developments, and concepts are the basis of scientific progress and competitiveness, expanding human knowledge and being expressed technologically as inventions. The resulting innovative products and services eventually find their way into public life.

Accordingly, the *"Research Reports from the Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik"* series compiles the institute's latest research and developments. We would like to make our results broadly accessible and to stimulate further discussions, not least to enable as many of our developments as possible to enhance everyday life.

FBH runs a transferred-substrate InP-HBT process with transit frequencies in the 400 GHz range. In cooperation with the Leibniz institute IHP this process is also available in an InP-on-BiCMOS version. In this report, a variety of monolithic integrated circuits is presented which demonstrate the potential of our InP technology. The impressive results include fundamental oscillators for frequencies from 96 GHz to 290 GHz, multipliers such as a full G-band (140-220 GHz) frequency doubler as well as a wideband 328 GHz quadrupler, and the worldwide first hetero-integrated sources beyond 200 GHz, with output frequencies of 250 and 330 GHz.

We wish you an informative and inspiring reading

Prof. Dr. Günther Tränkle
Director

Prof. Dr.-Ing. Wolfgang Heinrich
Deputy Director

The Ferdinand-Braun-Institut

The Ferdinand-Braun-Institut researches electronic and optical components, modules and systems based on compound semiconductors. These devices are key enablers that address the needs of today's society in fields like communications, energy, health and mobility. Specifically, FBH develops light sources from the visible to the ultra-violet spectral range: high-power diode lasers with excellent beam quality, UV light sources and hybrid laser systems. Applications range from medical technology, high-precision metrology and sensors to optical communications in space. In the field of microwaves, FBH develops high-efficiency multi-functional power amplifiers and millimeter wave frontends targeting energy-efficient mobile communications as well as car safety systems. In addition, compact atmospheric microwave plasma sources that operate with economic low-voltage drivers are fabricated for use in a variety of applications, such as the treatment of skin diseases.

The FBH is a competence center for III-V compound semiconductors and has a strong international reputation. FBH competence covers the full range of capabilities, from design to fabrication to device characterization.

In close cooperation with industry, its research results lead to cutting-edge products. The institute also successfully turns innovative product ideas into spin-off companies. Thus, working in strategic partnerships with industry, FBH assures Germany's technological excellence in microwave and optoelectronic research.

Signal Generation for Millimeter Wave and THz Applications in InP-DHBT and InP-on-BiCMOS Technologies

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To my beloved daughter "*Insha*" and "*My Parents*"

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This research work was a journey of a lifetime and it would not have been come to an end if I did not get the support in many ways from many persons in different times under various circumstances. It is a great opportunity to express my gratitude to all of them for their support before moving any further.

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Abstract

Increasing research activities in the mm-wave and sub-THz bands using different technologies have reached significant achievements over the past few years. A variety of commercial and defense applications are expected to be based on mm-wave and sub-Terahertz integrated circuits in the near future. Silicon-based technologies such as RF-CMOS and SiGe-BiCMOS have shown steady progress, but they are struggling to fulfill the demands due to their limitations in power-handling capability with increasing device speed. III-V technologies offer a higher potential in this regard, but do not allow high levels of integration. In order to move beyond silicon-based technologies while still providing high level of density and complexity, wafer level integration of III-V technologies has become highly interesting due to the overall benefit in terms of performances and complexities.

Accordingly, this work focuses on MMIC signal sources in Transferred Substrate (TS) InP-DHBT technology and successful wafer-level circuit integration in InP-on-BiCMOS technology. It is divided in three major parts. In the first part, it presents 96 GHz and 197 GHz fundamental sources using a 0.8 µm InP TS-DHBT process, which deliver +9 dBm and 0 dBm output power with 25% and 4.6% overall DC-to-RF efficiency, respectively. The first part also comprises a 290 GHz harmonic oscillator, which exhibits -9.5 dBm output power and shows 0.5% overall DC-to-RF efficiency. Furthermore, it demonstrates 162 GHz and 270 GHz push-push sources utilizing InP TS-DHBTs on a BiCMOS process, which achieve -4.5 dBm and -9.5 dBm output power and combined overall DC-to-RF efficiencies of 1.5% and 0.4%, respectively.

In the second part, multiplier-based signal sources are demonstrated. It presents a full G-band (140-220 GHz) frequency doubler, which delivers +8.2 dBm at 180 GHz and more than +5 dBm in the range 160-200 GHz as well as +2.5 dBm at 220 GHz. The doubler circuit exhibits a power efficiency of 16 % in this frequency range. Also, a 250 GHz single-ended frequency tripler is presented, with -4.4 dBm output power and 3% of DC-to-RF efficiency. The highest frequency is reached by a wideband 328 GHz quadrupler, which delivers -7 dBm output power at 325 GHz and exhibits 0.5 % DC-to-RF efficiency.

The final part is devoted to hetero-integrated circuits and the necessary design considerations. Two 250 GHz and 330 GHz sources are demonstrated that deliver -1.6 dBm and -12 dBm output power, respectively. These are the first hetero-integrated signal sources in this frequency range reported so far.

Kurzfassung

Die Forschungsaktivitäten in den Millimeter-Wellen- und Sub-THz-Frequenzbändern nehmen stetig zu. Mit unterschiedlichen Technologien konnten in den letzten Jahren erhebliche Fortschritte erzielt werden.

Man kann davon ausgehen, daß in naher Zukunft eine Vielzahl von kommerziellen und militärischen Anwendungen auf integrierten Schaltkreisen im Millimeter-Wellen- und Sub-THz-Frequenzbereich beruhen wird.

Auf Silizium basierende Technologien, wie RF-CMOS und SiGe-BiCMOS, entwickeln sich stetig weiter, unterliegen aber harten Einschränkungen in Bezug auf die erreichbare Maximalleistung bei den steigenden Einsatzfrequenzen.

Diese Probleme lassen sich durch den Einsatz von III-V-Halbleiter-Technologien umgehen, wobei der erreichbare Integrationsgrad signifikant geringer ist.
Die Heterointegration auf Wafer-Ebene erlaubt die Kombination der Vorteile beider Ansätze. Dabei werden beide Technologien in einem Halbleiter-Prozess verwendet, wodurch hohe Einsatzfrequenzen bei hoher Signalleistung und hoher Integrationsdichte realisierbar werden.
Die vorliegende Arbeit beschäftigt sich mit Signalquellen, die als integrierte Schaltungen in der Transfersubstrat (TS) InP-DHBT Technologie oder hetero-integriert in InP-on-BiCMOS-Technologie hergestellt wurden. Die Arbeit gliedert sich in drei Hauptteile.

Im ersten Teil werden Signalquellen bei 96 GHz und 197 GHz vorgestellt. Diese wurden im InP-TS-DHBT-Prozess mit einer Emitterbreite von 0.8 µm gefertigt. Die Schaltungen liefern Ausgangsleistungen von 9 dBm und 0 dBm bei Effizienzen von 25 % und 4.6 %. Darüber hinaus wird ein 290 GHz Oszillator auf der dritten Harmonischen vorgestellt, welcher -9.5 dBm Ausgangsleistung bei einer Effizienz von 0.5 % liefert. Ferner werden zwei Push-Push-Quellen bei 162 GHz und 270 GHz aus dem InP-on-BiCMOS-Prozess gezeigt. Diese erreichen Ausgangsleistungen von -4.5 dBm und -9.5 dBm mit Effizienzen von 1.5 % und 0.4 %.

Der zweite Teil der Arbeit beschäftig sich mit Signalquellen, die auf Frequenzvervielfachern basieren. Es wird ein Verdoppler für das gesamte G-Band (140 GHz bis 220 GHz) vorgestellt, welcher 8.2 dBm Ausgangsleistung bei 180 GHz und mehr als 5 dBm Ausgangsleistung von 160 GHz bis 220 GHz liefert. Bei 220 GHz wird noch eine Leistung von 2.5 dBm erreicht.

Der Verdoppler arbeitet mit einer Leistungseffizienz von 16 %. Weiterhin wird ein Frequenzverdreifacher bei 250 GHz präsentiert. Dieser erreicht -4.4 dBm Ausgangsleistung

und eine Effizienz von 3 %. Die höchste Ausgangsfrequenz wird mit einem breitbandigen Vervierfacher um 328 GHz erreicht. Dieser liefert 7 dBm bei 325 GHz mit einer Effizienz von 0.5 %.

Der dritte Teil der Arbeit ist den heterointegrierten Schaltungen und der dafür erforderlichen Entwurfsmethodik, gewidmet. Zwei Quellen bei 250 GHz und 330 GHz mit Ausgangsleistungen von -1.6 dBm und -12 dBm werden vorgestellt. Dabei handelt es sich um die ersten heterointegrierten Signalquellen in diesen Frequenzbereichen.

Acknowledgement

Abstract

Contents

1 Introduction

1.1. Motivation

Recently, a variety of commercial and defense applications that demand for sub-Terahertz and mm-wave integrated circuits have emerged [1]. The frequency range between 100 GHz and 1 THz offers large bandwidth for high-speed communications as well as improved performance of sensors and imaging systems due to short wavelengths. All these systems require signal sources for local oscillators or signal generation. The sources are key building blocks for such applications. Performance targets include particularly a combination of high output power, low phase noise and high DC-to-RF efficiency. In the past years, significant progress has been made in sources for the mm-wave and sub-terahertz frequency range, using various semiconductor technologies. Mostly, these sources have been realized in push-push configuration [2], [3]. Few of them are fundamental frequency sources [4], [5] but they are relatively power-hungry and deliver less output power. Hence, developing efficient fundamental frequency sources at sub-THz and mm-wave frequencies is still the subject of intensive research.

Integrated sources based on frequency multiplication offer many advantages for mm-wave and THz frequencies applications. At present, in the microwave frequency bands fundamental sources are commercially available and mature enough offering high output power and efficiency, low noise, electronic tuning and compact design [6], [7]. Usually, millimeter-wave and terahertz frequency multipliers exhibit broadband, high power handling capabilities and high efficiency. Therefore, a microwave source combined with a millimeter-wave or terahertz frequency multiplier provides a compact broadband tunable source at frequencies from 30 GHz to well above 1 THz [8], [9].

The major challenge in signal generation at such frequencies is that the active devices have to be operated close to, or even above their transit frequencies and close to breakdown voltage as well. Additionally, the quality factor of the passive components degrades compared with lower frequencies. Recently, SiGe and CMOS circuits have been demonstrated operating at frequencies beyond 250 GHz [10], [11]. Nevertheless, due to their more relaxed geometrical dimensions, compound semiconductors such as InP offer better power capabilities. This is why InP is used in the research work presented here.

But it is not sufficient to have individual circuits with decent performance. Integrated components and modules with increased functionality are crucial for successful implementation of system on-chip solutions. At millimeter-wave and THz frequencies system-on chip solutions further improve performance because the number of interconnects is reduced. Nowadays, system-on chip solutions based on CMOS and BiCMOS technologies cover both analog and digital circuits and reach operating frequencies beyond 250 GHz [12], [13]. However, this is achieved at the cost of lower breakdown voltage and thus reduced output power. On the other hand, compound semiconductors such as InP exhibit operating frequencies approaching 1 THz with high power capabilities [14]. Therefore, wafer-level hetero-integration of InP circuits with BiCMOS promises great potential. This is a main motivation behind the research work presented here. Recently, research on InP-on-BiCMOS device level integration has been reported by the DARPA funded consortium [15], [16] and there are ongoing activities to combine GaN-on-Si CMOS [17].

1.2. Research Objectives

This thesis investigates realization of signal sources for the frequency range beyond W band in InP TS-DHBT and InP-on-BiCMOS technologies. Since the transferred-substrate process has been made available only recently, emphasis of the work is on exploring capabilities in terms of performance and demonstrating the potential of the hetero-integration technology. The specific research objectives include:

- Design and characterize fundamental and harmonic fixed-frequency oscillators up to 300 GHz using the InP TS process.

- Design and characterize signal sources based on multipliers for frequencies beyond 200 GHz using the InP TS process as well as the InP-on- BiCMOS versions.

1.3. Thesis Organization

The dissertation is organized as follows: Chapter 2 discusses the InP TS process and the hetero-integrated InP-on-BiCMOS process technology. Chapter 3 describes the active and passive modelling as well as measurement methodology. Chapter 4 presents the general theory of oscillators as well as the design and measurement results of the oscillators in InP TS and InP-on-BiCMOS process technology.

Chapter 5 then is devoted to the circuit topologies and the measured results of the various frequency multipliers developed. Chapter 6 deals with the details of the design procedure and the results of the hetero-integrated signal sources. At the end, Chapter 7 summarizes the contributions of the research work presented in this dissertation and gives an outlook for future designs at mm-wave and THz frequencies.

2 Technology

Still growing needs for faster data communication rates and to fill up new application areas up to Terahertz (THz) frequencies raise the question how far traditional semiconductor technologies can satisfy these markets. To address this challenge, advanced semiconductor devices with maximum oscillation frequencies (f_{MAX}) of 1 Terahertz or beyond have been developed [18]. Device scaling plays the most important role in this journey. Si technologies based on Si CMOS or SiGe BiCMOS HBTs are preferred for various applications owing to the high integration level, mature design environment, low power and low cost (for high volume). However, its device operation speed is limited by the intrinsic material properties of Si. In contrast, high speed III-V technologies based on GaAs or InP benefit from excellent electron transport characteristics such as high mobility and speed. This is clearly shown in Fig. 1, which compares recently reported unity current gain, f_t and unity power gain, f_{MAX}; values of various III-V and Si-based devices. It is obvious from the plot that the speed of III-V devices, both HBTs and HEMTs, dominate over that of Si devices, exhibiting best f_{MAX} exceeding 1.2 THz. It is also true that the operation speed of Si-based devices has been significantly improved over the past years, now reaching up to 500 GHz (see Fig. 2.1) in terms of f_{MAX}, which is sufficient for circuits operating well beyond 100 GHz. This is achieved with aggressive device scaling, which increases mask and processing cost. This aggressive device scaling significantly reduces the breakdown voltage and hence the available RF output power. On the other hand, compound semiconductors such as InP exhibit high power capabilities at operating frequencies beyond 200 GHz. This is also clearly visible in Fig. 2.2, which shows recent power trends realized in various circuits on different technologies.

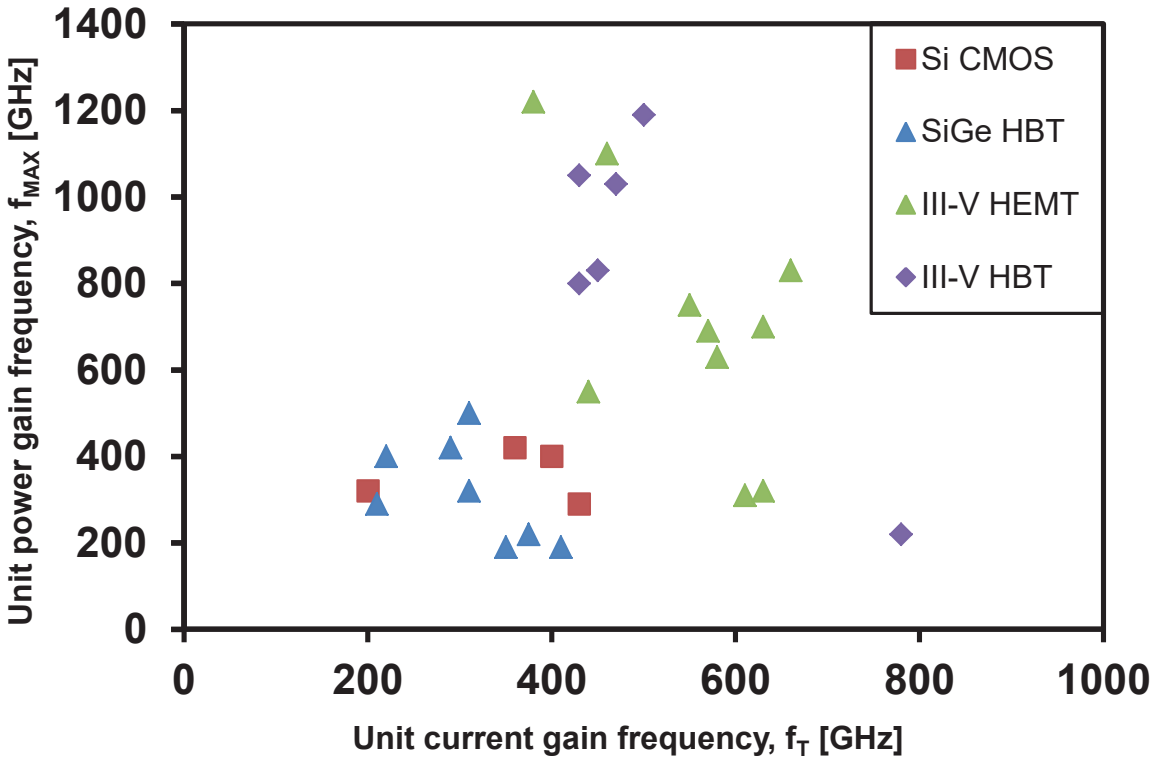


Fig. 2.1. f_T and f_{MAX} of recently reported devices achieved on different technologies [19].

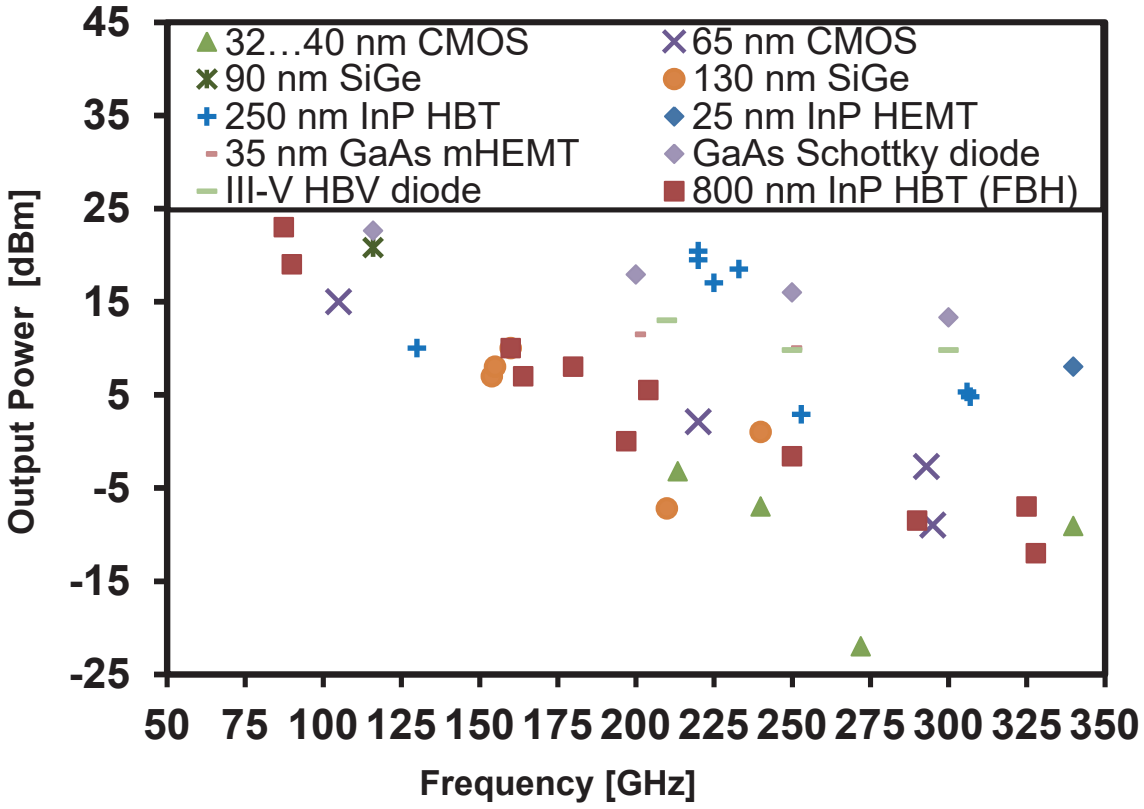


Fig. 2.2. Performance of recently reported circuits operating near or beyond 100 GHz on different technologies.

The III-V based devices achieve higher f_T and f_{MAX} values and they deliver higher output power compared to the Si-based technologies. But, their capability in terms of circuit complexity and functionality is lower than for the Si technologies, i.e., CMOS or SiGe BiCMOS. Therefore, combining Si based technologies with a III-V compound semiconductor such as InP offers the possibility to realize compact circuits with benefits from both technologies. This solution combines the high-integration capabilities of the silicon process and the high-frequency high-power potential of compound semiconductor (see Fig. 2.3). Such integrated components and modules with increased functionality are crucial for successful implementation of system-on-chip solutions. At millimeter-wave frequencies and beyond system-on-chip solutions show superior performance compared to other approaches, due to the reduced number of chip-to-chip interconnects in the systems, which become increasingly lossy at high frequencies.

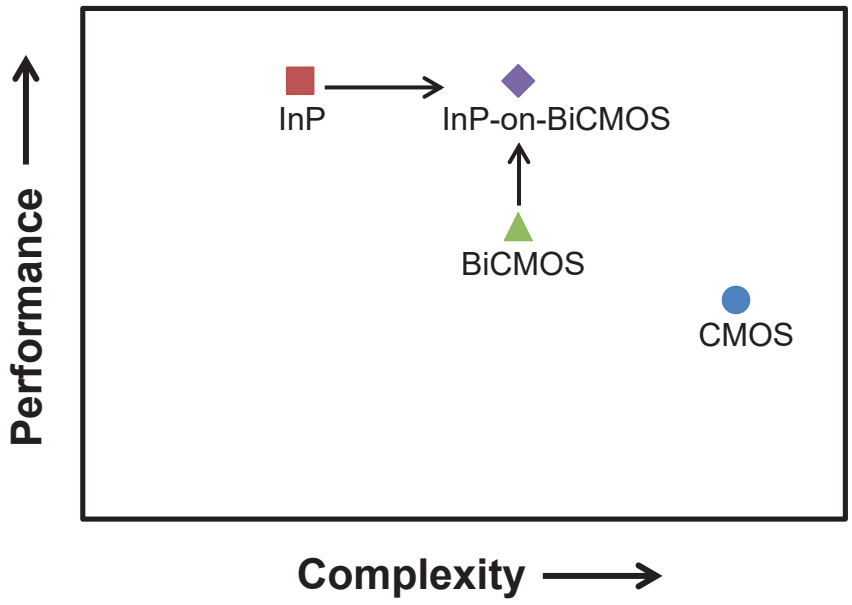


Fig. 2.3. Performance vs complexity in different technologies.

In this work, the main focus is on circuit designs for the FBH 0.8 µm transferred-substrate (TS) InP-DHBT process. The transfer of the substrate, i.e. removing the InP, embedding the HBT in BCB and using AIN as a host substrate, offers several advantages: less extrinsic capacitance, relaxed geometry and better heat conduction by means of replacing InP substrate by AIN substrate. The TS InP-DHBT process flow is briefly discussed in Section 2.2 while Section 2.3 describes the heterogeneous (InP-on-BiCMOS) process.

2.1 Transferred Substrate (TS) Process Flow

The TS InP DHBT epitaxial layer composition is similar to conventional DHBTs, but with reduced sub-collector thickness and additional etch stop layers at the bottom for substrate removal. The first step, the front-side process, is the same as for conventional InP-DHBTs. In this step, base and emitter metal is introduced, then emitter mesa is etched and at the end the base metal is deposited. After that, planarization of the device is done by benzocyclobutene (BCB) and then the ground metallization is formed. This completes the front-side process (see Fig. 2.4. a). In the next step the complete structure is bonded upside down onto an AlN wafer with a 2-µm layer of benzocyclobutene (BCB) (see Fig. 2.4. b). After curing the BCB the two wafers form a firm compound. Then the whole structure is flipped as shown in Fig. 2.4. c and the InP substrate including all unnecessary semiconductor material (e.g., the extrinsic collector under the base contacts and base pad) are removed by etching back-to-front, until only the epitaxial layers of the active circuit elements remain. This approach substantially reduces device parasitics, since the transistor is embedded in BCB (ε_r=2.65) instead of InP (ε_r=11). Thus, operating frequency is increased without transistor downscaling. These features of the transferred-substrate technology make it ideally suited for high-frequency power applications. After removing the InP substrate, collector mesa is etched. At this step, the collector metal is open to access, which can be independently scaled according to the electrical and thermal requirements (see Fig. 2.4. d). In a final step, necessary vertical interconnects are formed and base metal resistor, MIM capacitors (dielectric material: SiNx) and thin-film microstrip transmission lines complete the TS MMIC process. Fig. 2.5 shows the schematic cross-section of the final InP TS DHBT process structure. The TS version used in this work is based on a 0.8 µm InP-DHBT technology, which offers f_T/f_{MAX} values above 320 GHz with BVCEO = 4V [20]. The process has three Au metal layers with 1µm, 1.5µm and 4.5 µm thickness, respectively, with a dielectric constant of 2.65. For more details of the TS process flow see [20].

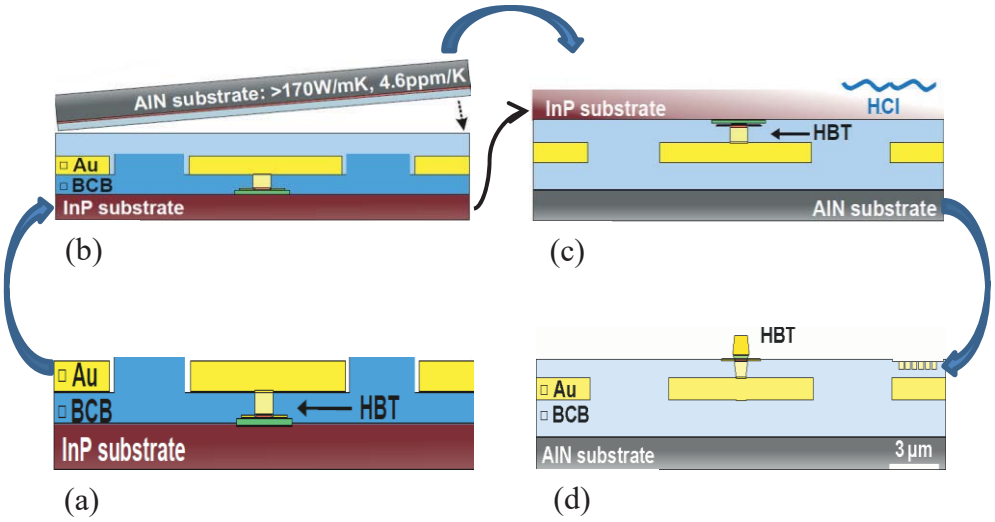


Fig. 2.4. Process flow of the transferred-substrate (TS) InP DHBT fabrication.

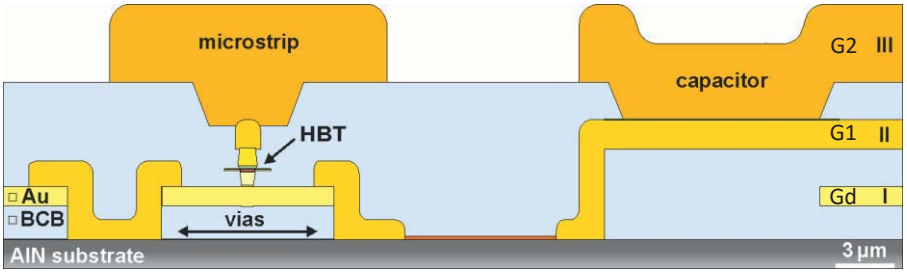


Fig. 2.5. Schematic cross-section of the final layer structure.

2.2 InP-on-BiCMOS Process Flow

The novelty of the heterogeneous integration InP-on-BiCMOS in comparison with other approaches is the integration of already processed BiCMOS wafers with InP DHBT wafers, providing low-loss interconnects. This ensures minimum interference between the two processes and keeps the high level of maturity of the Si technology from the very beginning. Basically, the process flow is the same as that for AlN substrate discussed above but using a BiCMOS wafer instead of the AlN substrate. In a first step, the desired circuits in BiCMOS technology are processed and, in parallel, the InP D-HBT circuits are prefabricated up to the transistor level using the TS process discussed in Section 2.1. Then, the BiCMOS and the InP wafers are joined by means of wafer-level BCB bonding (see Fig. 2.6). After that the InP substrate including all unnecessary semiconductor material is removed, until only the epitaxial layers of the active circuit elements remain. In the last step, deep vias are etched to

connect the uppermost Si metallization level to the InP part and the remaining InP metallization levels are completed (see Fig. 2.7).

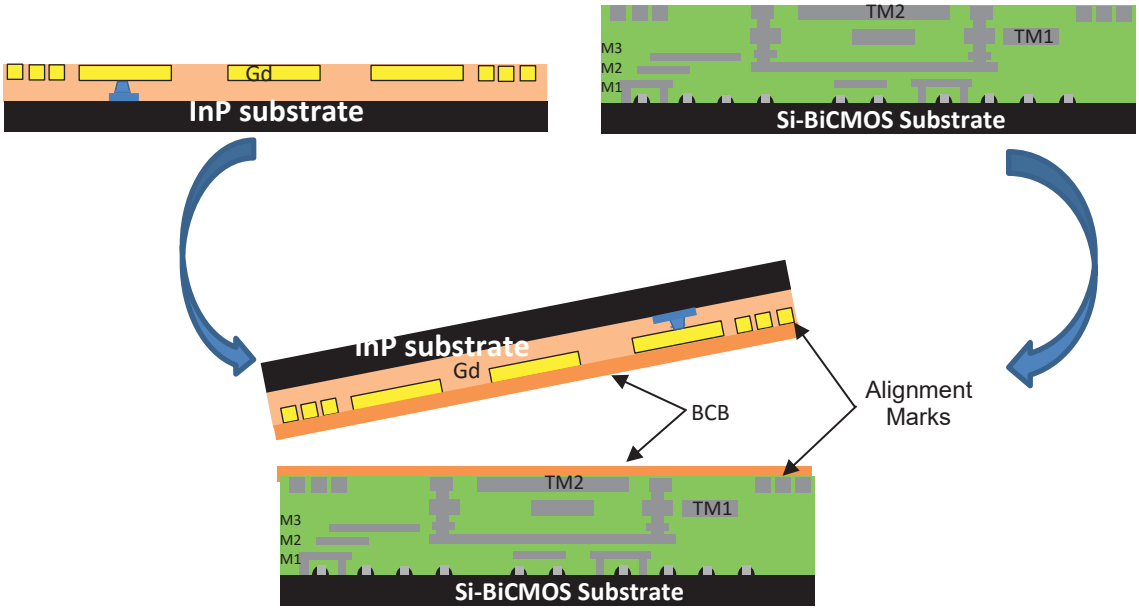


Fig. 2.6. Schematic cross-section of the transferred-substrate InP-on-BiCMOS process.

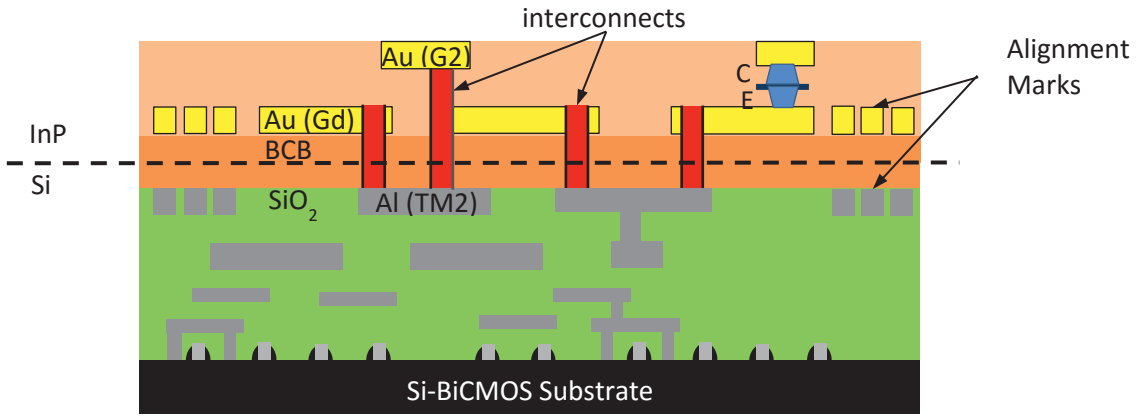


Fig. 2.7. Schematic cross-section of the final InP-on-BiCMOS environment.

Fig. 2.8 shows the resulting layer stack of the hetero-integration process. On the BiCMOS side, it comprises a 0.25 µm technology with f_T/f_{MAX} = 180/220 GHz, the InP part is based on a 0.8 µm TS InP-DHBT technology, which offers f_T/f_{MAX} values above 320 GHz. For

further details of the InP-on-BiCMOS process see [21, 22]. Table 2.1 summarizes the specifications of the InP-on-BiCMOS process .

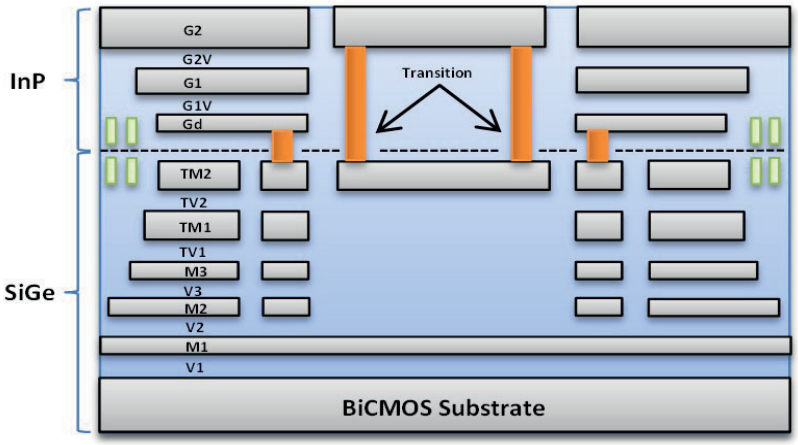


Fig. 2.8. Layer stack of the hetero-integration process.

Table 2.1

Summarized specifications of the InP-on-BiCMOS process

Process	**Emitter width [µm]**	**HBT Type**	**f_T/f_{MAX} [GHz]**	**No. of metal Layers [Thickness]**	**Passives**	**BV_{CEO} [Volts]**
TS InP	0.8	Common emitter Common base	>320	3 gold (1.5µm, 2.5µm, 4.5µm)	MIM capacitors, resistor (base metal)	>4.5
SiGe BiCMOS	0.25	Common emitter Common base	180/220	5 aluminium (1 µm, 2µm, 3µm)	MIM capacitors, resistors	>1.9

3 Device Modelling and Measurement Setup

The major challenge in circuit design at mm-wave and THz frequencies is that the active devices have no accurate model and they have to be operated close to or even above their transit frequencies as well as close to breakdown voltage. Additionally, circuits are more sensitive to parasitics which result in capacitances, resistances, distributed effects etc. Thus, the quality factor of the passive components degrades compared to lower frequencies. The objective of this chapter is to discuss modeling and characterization of the active and passive elements at frequencies beyond 100 GHz. The results were used in the design of the circuits presented in Chapters 4, 5 and 6.

3.1 Passives

Passive circuit elements are critical components of MMIC design. The passive structures discussed here include transmission lines, resistors, capacitors, the high frequency RF pads, DC pads, vias and the interconnection between the InP and the BiCMOS part on the wafer.

3.1.1 Transmission Line Theory

In high frequency circuit design transmission lines are described by a distributed-parameter network, where voltages and currents vary in magnitude and phase over its length. This is governed by equations 3.1 and 3.2, where the $e^{\gamma z}$ term represents wave propagation in the +z direction and the $e^{-\gamma z}$ term represents wave propagation in the –z direction. The complex propagation constant γ is given by equation 3.3, whose real part α is the attenuation constant and the imaginary part β represents the phase constant [23].

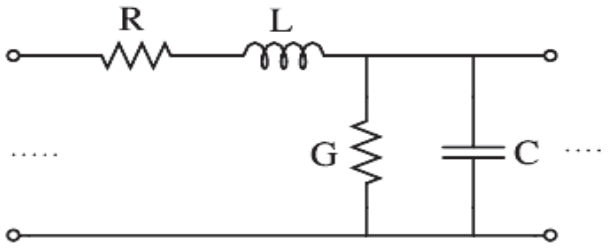


Fig. 3.1. Transmission line equivalent circuit.

L represents the total inductance of the two conductors, and the C their capacitance. The series resistance R denotes the resistance due to the finite conductivity of the conductors, and the shunt conductance G is due to dielectric loss in the material between the conductors.

Generally, γ is a function of frequency. Equation 3.4 provides Z_0, the characteristic impedance of the transmission line.

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \tag{3.1}$$

$$I(z) = I_0^+ e^{-\gamma z} - I_0^- e^{\gamma z} \tag{3.2}$$

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{3.3}$$

$$Z_0 = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{3.4}$$

In many practical cases, however, the loss of the line is small and can be neglected, which results in a simplification of the above results. Setting R=G=0 yields the propagation constant according to equation 3.5. As expected for a lossless line, the attenuation constant α is zero. The characteristic impedance simplifies to equation 3.6

$$\gamma = \alpha + j\beta = j\omega\sqrt{LC} \tag{3.5}$$
$$\beta = \omega\sqrt{LC} \quad and \quad \alpha = 0$$

$$Z_0 = \sqrt{\frac{L}{C}} \tag{3.6}$$

Therefore, one has for the wavelength

$$\lambda = \frac{2\pi}{\beta} = \frac{2\pi}{\omega\sqrt{LC}} \tag{3.7}$$

And for the phase velocity

$$v_p = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}} \tag{3.8}$$

One important feature of the transmission lines is that it causes an impedance transform. A load impedance Z_L at the end of a line l is transformed to input impedance Z_{in} as given by:

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan\beta l}{Z_0 + jZ_L \tan\beta l} \tag{3.9}$$

Some special cases are discussed as follows:
Consider the lossless transmission line terminated in a short circuit $Z_L = 0$, then

$$Z_{in} = jZ_0 \tan \beta l \tag{3.10}$$

Vice versa, a lossless transmission line terminated by an open, i.e. $Z_L = \infty$, yields

$$Z_{in} = -jZ_0 \cot \beta l \tag{3.11}$$

For the particular case of a lossless transmission line with a length of $l = \lambda/2$, one has

$$Z_{in} = Z_L \tag{3.12}$$

If the lossless line is a quarter-wavelength long or, more generally, $l = \lambda/4 + n\lambda/2$ for $n = 0, 1, 2, 3, \ldots$
, the input impedance is given by:

$$Z_{in} = \frac{Z_0^2}{Z_L} \tag{3.13}$$

Equation 3.13 describes the principle of a quarter-wave transformer, because it transforms the load impedance to its inverse scaled by the square of the characteristic impedance of the line.

3.1.1.1 Investigation of Different Transmission Lines

The choice of the transmission line is one of the important considerations in the design of MMIC circuits. In order to achieve low loss high quality factor matching networks, the transmission line choices have to be investigated before moving to the MMIC design environment. For that reason, different line geometries have been investigated. According to the process discussed in Section 2.2, top 4.5 µm thick gold (G2) metal is used as a thin film microstrip line with Gd as the ground conductor. The width of a 50 ohm microstrip line in G2 over Gd ground plane is about 12 µm (see Fig. 2.5). Fig. 3.2 shows the measured transmission and reflection coefficient of three different lines with 50 ohm characteristic impedance and lengths of 420 µm, 1250 µm and 1900 µm. Fig. 3.2 shows that the loss contribution of a 1 mm long transmission line is around 1 dB up to 110 GHz.

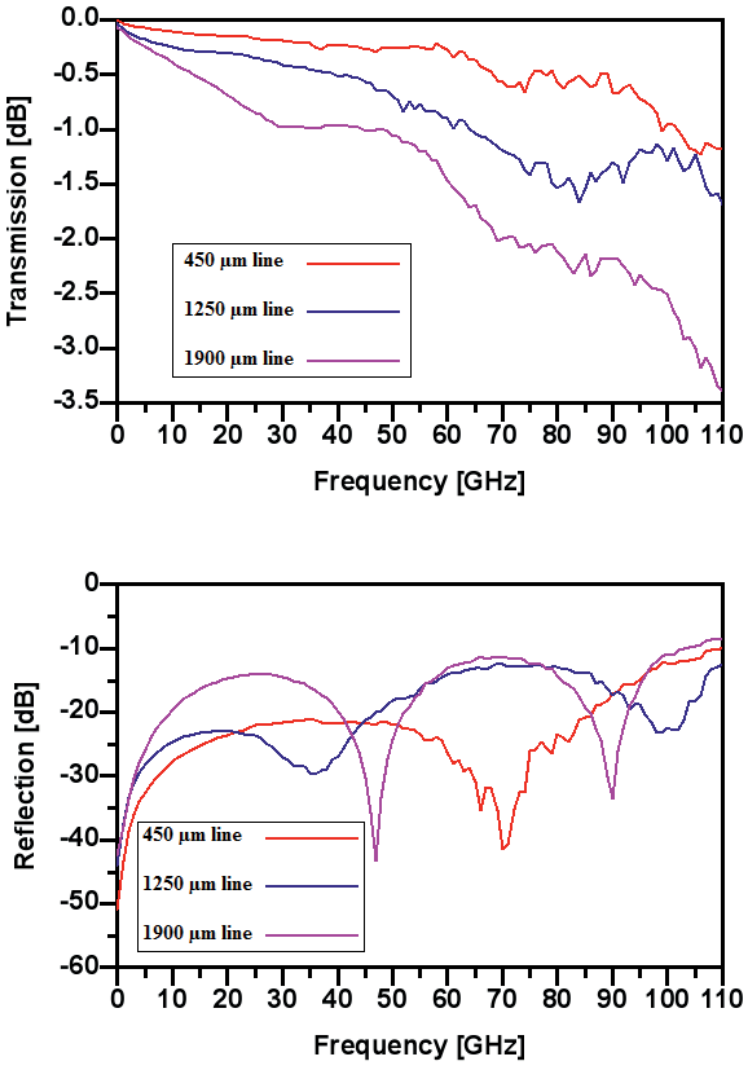


Fig. 3.2. Measured transmission and reflection coefficient of 420 µm, 1250 µm and 1900 µm long transmission lines in the TS InP process (50 ohm thin-flim microstrip with 12 µm strip width).

3.1.2 Resistors

In this work, base metal (B1) resistors have been used in the DC biasing network to avoid unwanted low frequency oscillations. In order to ensure stable circuit operation, also a small resistor (e.g. 5 ohm) was used at the input of the circuit. The resistors have not been employed for any matching network in order to avoid unnecessary losses. For resistor modeling, first a simulation was performed using a 2.5D EM-simulator and then a lumped equivalent circuit model was extracted in ADS. This equivalent circuit model is then applied in circuit simulation. Fig. 3.3 presents the layout and the equivalent circuit model of the 10 ohm resistor. C_1, C_2 (8 fF) and L_1, L_2 (8 pF) denote the parasitic capacitances and inductances, respectively.

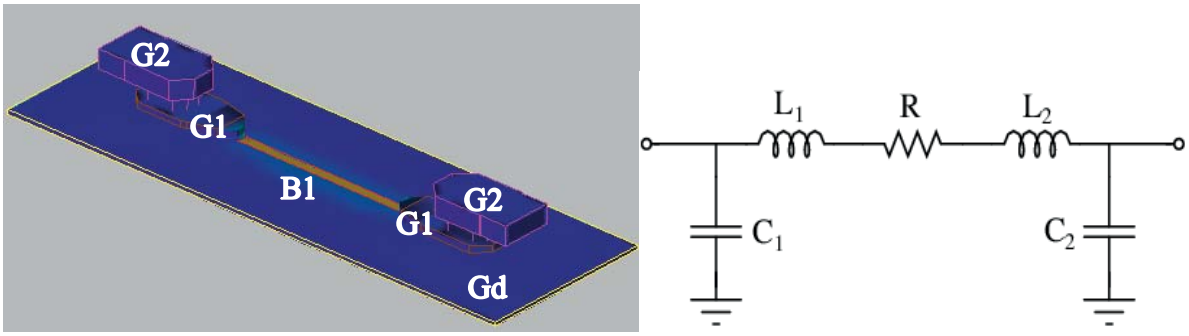
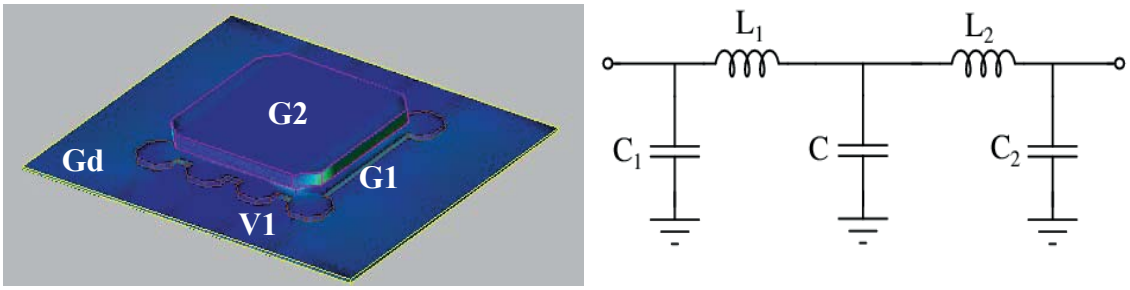


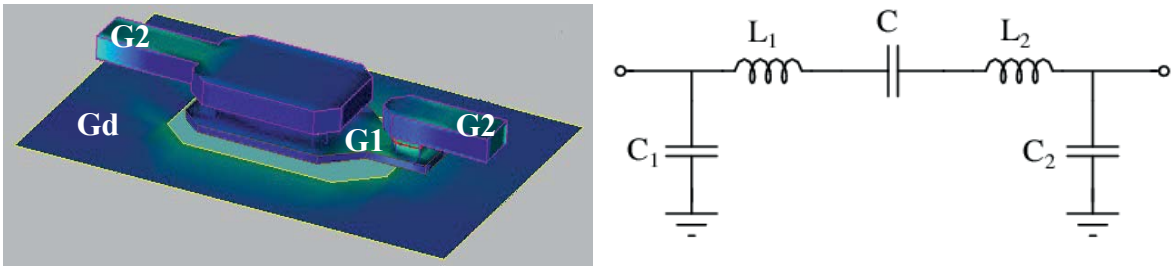
Fig. 3.3. Layout of the 10 ohm base metal (B1) resistor (left) and generalized equivalent circuit model (right)

3.1.3 Capacitors

There are two types of MIM capacitors that have been used in this work, depending on their orientation with regard to RF ground. One is the shunt capacitor and the other one is the serial capacitor. Since both capacitor versions include non-negligible parasitic effects, they have not been used for the matching networks. The shunt capacitor was applied only as bypass capacitor and the serial capacitor for DC blocking. Both capacitors have been individually EM simulated and described by an equivalent circuit model in ADS. Fig. 3.4 (a, b) shows the layout and lumped equivalent-circuit model of the 1000 fF capacitor. C_1, C_2 (6 fF) and L_1, L_2 (9 pH) denote parasitic capacitances and inductances, respectively.



a) Layout of the 1000 fF shunt capacitor (left) and generalized equivalent circuit model (right)



b) Layout of the 188 fF series capacitor (left) and generalized equivalent circuit model (right)

Fig. 3.4. Shunt and serial MIM capacitor layout and equivalent circuit model.

3.1.4 Ground Via

The ground via is an important element in the high frequency design environment. This applies to transistors and bias networks as well as to balun and band pass filter. Fig. 3.5 shows the structure of a ground via and its lumped circuit model. C (5 fF) , L (0.5 pH) and R (0.3 ohm) denote model parameters.

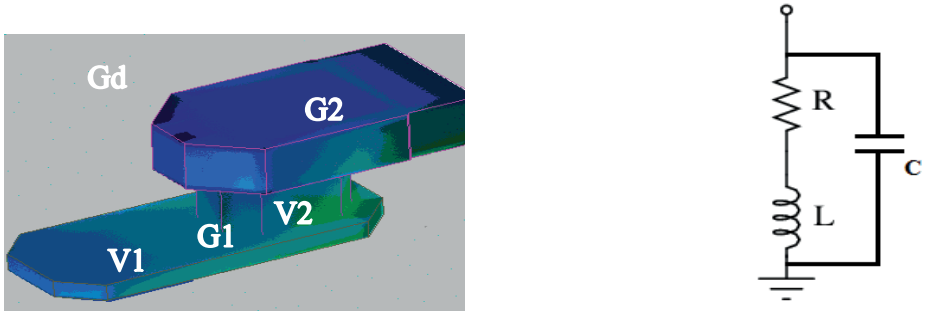


Fig. 3.5. Layout of the ground via (left) and generalized equivalent circuit model (right).

3.1.5 InP-BiCMOS Transition

In the hetero-integrated circuit design, the transitions between the BiCMOS and InP part represent one of the most important features. The main issues are to optimize them with regards to misalignment between the BiCMOS and InP wafers and to parasitic effects. Since thin-film microstrip lines are employed in both parts, the signal connection is realized between the top InP gold metal layer (G2) and the top BiCMOS aluminum metal layer (TM2). Vias close to the InP transmission line ensure that a common ground is shared between the InP and BiCMOS circuit parts. Optimization is performed by electromagnetic (EM) simulations employing the 3D solver CST Microwave Studio. After having the optimized results from the EM simulation, an equivalent lumped circuit was extracted in ADS. Fig. 3.6 shows the transition layout with its lumped equivalent circuit model. More details of the transition can be seen in [101], [107].

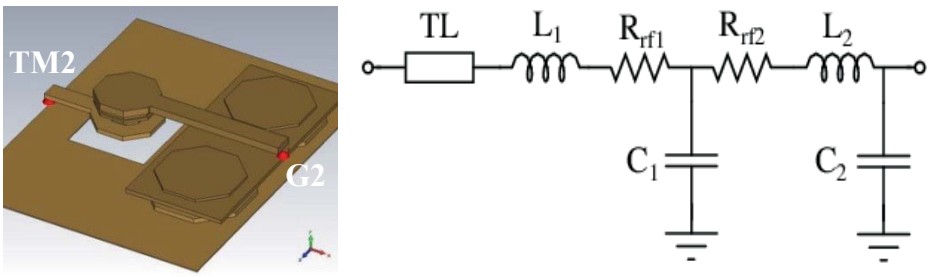
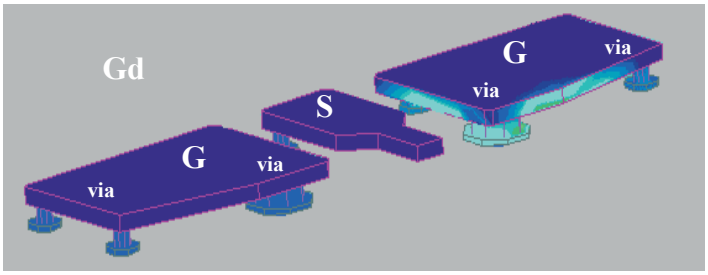


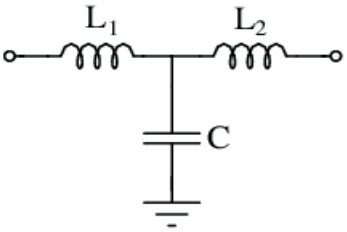
Fig. 3.6. Layout of the InP-BiCMOS transition (left) and generalized equivalent lumped circuit model (right).

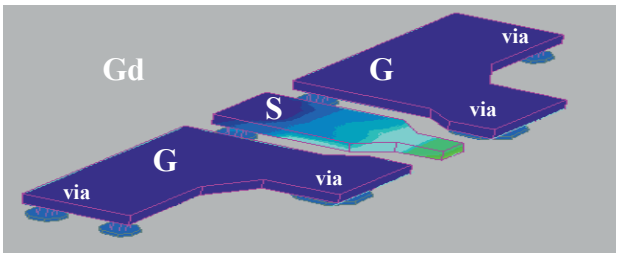
3.1.6 DC and High Frequency RF Pads

In this work, two different types of high frequency pads are realized because at different frequency bands the probe tips have different pitches. Both pads are used depending on the input and output frequency. Fig. 3.7 (a) shows the Ground-Signal-Ground (GSG) RF pad which is used for frequencies up to 250 GHz. This pad is optimized for probe pitches from 75 µm to 100 µm. In order to avoid mechanical problems during on-wafer probing, small mechanical vias were used around the pads corner (see layout). Fig. 3.7 (b) shows the second type of Ground-Signal-Ground (GSG) RF pad which is used for the frequencies beyond 250 GHz. This pad is optimized for probe pitches from 35 µm to 70 µm. Both pads were optimized using the 3D EM simulation tool CST microwave studio and equivalent circuits were realized in ADS. For DC biasing GSGSG DC pads were used. Fig. 3.8 shows the GSGSGS DC pad with 100 µm pitch. Ground pads also include thermal vias down to the AIN substrate, which spread the heat away from the circuit to the AIN substrate (see layout).



(a) Layout of the Ground-Signal-Ground (GSG) RF pad frequency up to 250 GHz (left) and generalized equivalent lumped circuit model (right).





(b) Layout of the Ground-Signal-Ground (GSG) RF pad frequency range from 250 to 350 GHz (left) and generalized equivalent lumped circuit model (right).

Fig.3.7. Ground-Signal-Ground (GSG) high frequency RF pads.

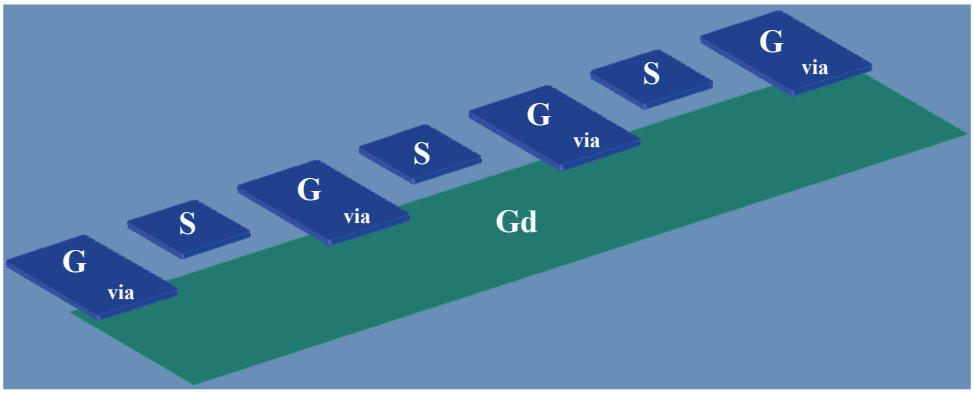


Fig. 3.8. Layout of the GSGSGSG DC pads.

3.1.7 Post-Layout Analysis

Post-layout analysis is one of the important steps before moving to chip fabrication in the design of mm-wave and THz circuits. The main purpose of the post-layout simulation is to verify the design compliance with those constraints that are not taken into account during pre-layout simulation. In this work, each circuit (without the active devices) was individually verified using ADS 2.5D EM-momentum post-layout simulation. This included all passives, RF and DC pads as well as circuit ground. Fig. 3.9 presents the resulting post-layout structure of a W-band fundamental oscillator.

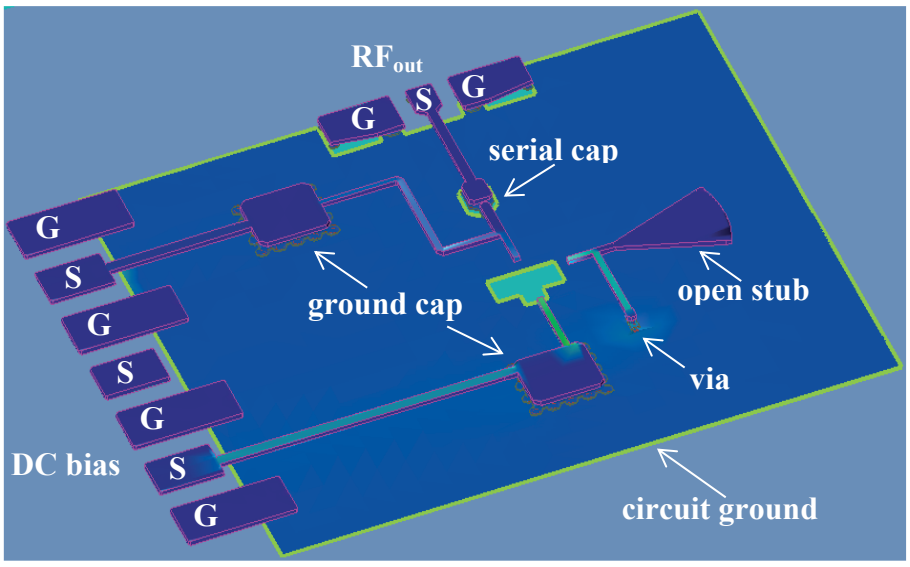


Fig. 3.9. Structure of a W-band fundamental Oscillator analyzed post layout using 2.5D EM ADS momentum.

3.2 Active Elements

For a successful design the active device performance has to be described properly. In MMIC circuit design at high frequencies, this is a difficult task because transistor behaviors become more complex with increasing frequencies. The description should include small-signal and large-signal characteristics as well as noise. All the characteristics depend on the device size, biasing point, temperature, process, parameter extraction methodology and frequency. These dependencies are not always linear and often must be determined experimentally to fit and/or correct the modeling equations. In this section, the transistor small and large signal model will be discussed.

3.2.1 Small and Large -Signal Model

Fig. 3.10 shows the simple HBT's small-signal model. At high frequency, such a simple model often fails to consider effects that are critical for high power high frequency design. Generally, complex model accuracy comes at an expense of simulation speed and resources. However, FBH has developed a TS HBT model that is a good compromise for achieving both high simulation speed and model accuracy. Fig. 3.11 illustrates the large-signal model accuracy in terms of output power and gain compression. More details regarding FBH TS HBT modeling can be found in [24].

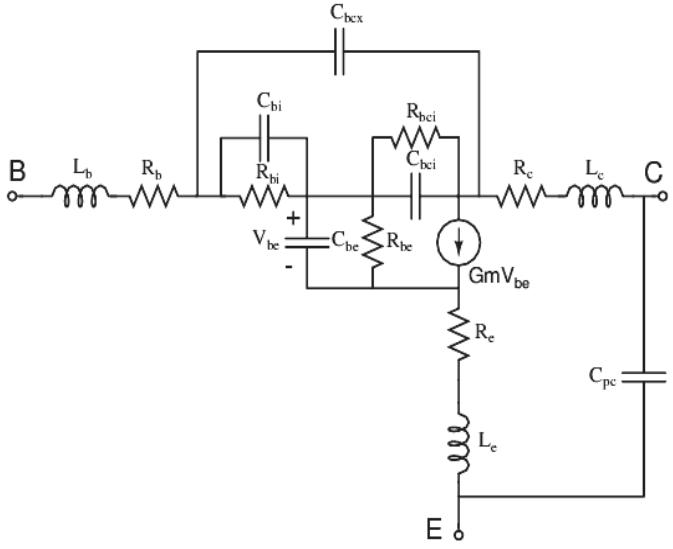


Fig. 3.10. Small-signal equivalent circuit model for the TS InP HBT device. The capacitance C_{bi} is included in the augmented small-signal equivalent circuit model [24].

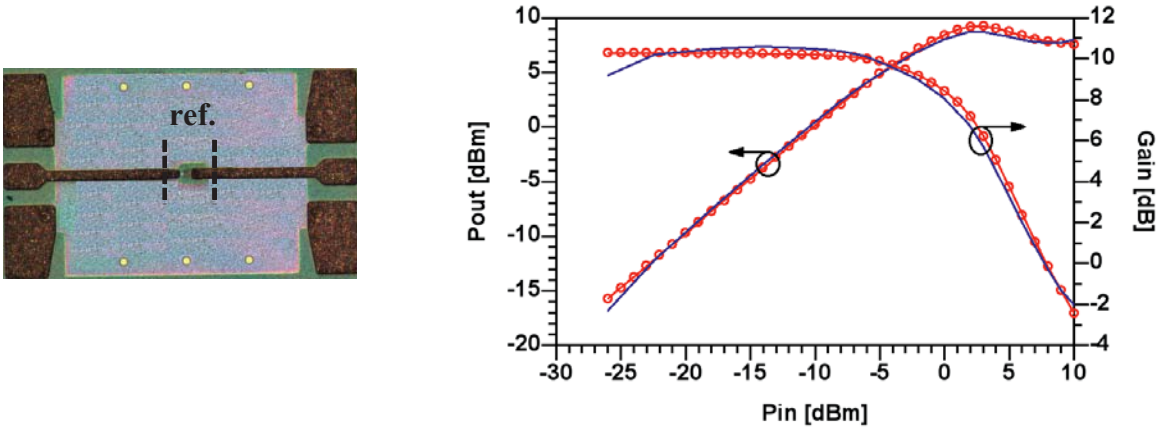


Fig. 3.11. Measured (solid line w. symbols) and simulated (solid line) large-signal performance of a single finger common emitter HBT at 77 GHz. The device is biased at V_{ce} = 1.4 V with a quiescent current of I_{cq} = 22.7 mA [24].

3.3 Measurements

After manufacturing the circuit, the final task is to investigate the performance of the circuit. However, to measure and characterize such mm-wave and THz components have always been a challenge. Generally, high frequency on-wafer circuit measurements reduce characterization time and cost, as they remove the need for additional work intensive dicing and packaging of chips which is the only other alternative method for circuit testing. On-wafer probing of circuits provides quick performance evaluation to improve designs for subsequent circuit fabrication iterations and for screening of circuits in a mass production environment. In this work, all the circuits have been characterized on wafer. The on-wafer measurements discussed here include S-parameter, spectrum and power measurements. Fig. 3.12 shows the on-wafer measurement setup to characterize oscillator circuits (in contrast to S-parameters).

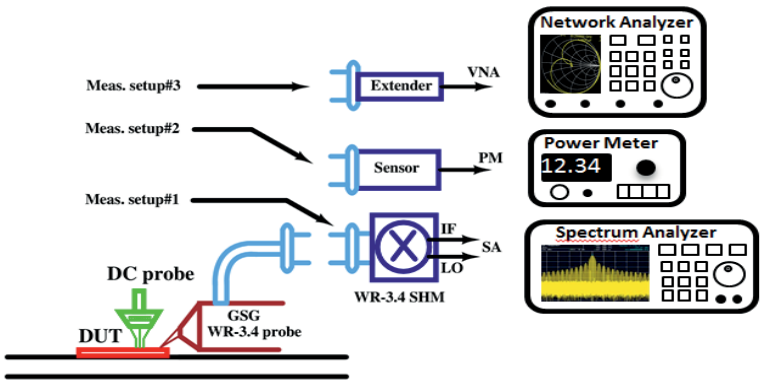


Fig. 3.12. Measurement setup for characterization of signal sources (meas. setup #1 for output spectrum, meas. setup #2 for power measurement, meas. setup #3 for S parameters)

3.3.1 S-parameters

S-parameters are the basic measured quantities. They describe how the device under test (DUT) modifies a signal that is transmitted or reflected in forward or reverse direction. In this work, S-parameters have been measured at different frequencies for passive and active components, using a R&S ZVA67 VNA with appropriate R&S frequency extension modules at different frequency bands (e.g. 75-110 GHz, 140-220 GHz, 220-325 GHz) and with respective probes from GGB and Cascade Microtech. For calibration the multiline Thru-Reflect-Line (mTRL) method has been used because its simplicity and accuracy [25, 26]. For multiline TRL calibration, the on-wafer standards short, 200 µm 'Thru' line, 100 µm symmetric 'Reflect' line, and a set of additional on-wafer transmission lines of different length (e.g. 420 µm, 1250 µm and 1900 µm) were used.

3.3.2 Spectrum

For oscillator characterization, bandwidth and spectral purity spectrum analysis is one of the most important steps. Using a normal setup of a spectrum analyzer, it is difficult to measure the mm-wave and THz frequencies because it has limited frequency range. Therefore, to extend the frequency range of the input signal, an external mixer needs to be used. In this case, the LO frequency is fed to the external mixer, where it is mixed with the RF input from the original input signal. In addition, the harmonics of the LO are mixed with the input signal and converted to new intermediate frequencies. Thus, a wider range of frequencies can be obtained with the same LO. The IF from the external mixer is then returned to the spectrum analyzer [27]. Depending on the required frequency band, the appropriate order of harmonic and the mixer type (3 ports) must be selected. Once the harmonic and the mixer type are selected, the given band conversion loss of the table will be read automatically by the spectrum analyzer. In this work, spectrum analysis was performed using R&S FSUP and FSW signal source analyzer. Since this measurement uses an external mixer, several unwanted harmonics product can be seen in the full band of spectrum. In order to ensure that the correct frequencies are picked, the two sweeps are performed alternately. Fig.3.13 shows two signal traces, one is the test signal (blue) at 248 GHz and the other one is the reference signal (black), which has been obtained by a shift to lower frequencies according to 2x IF/(N x harmonics). Input signals in the desired sideband that are converted by means of the set harmonics are displayed in both traces at the same position on the

frequency axis. Image signals and mixer products caused by other harmonics are displayed in both traces at different positions.

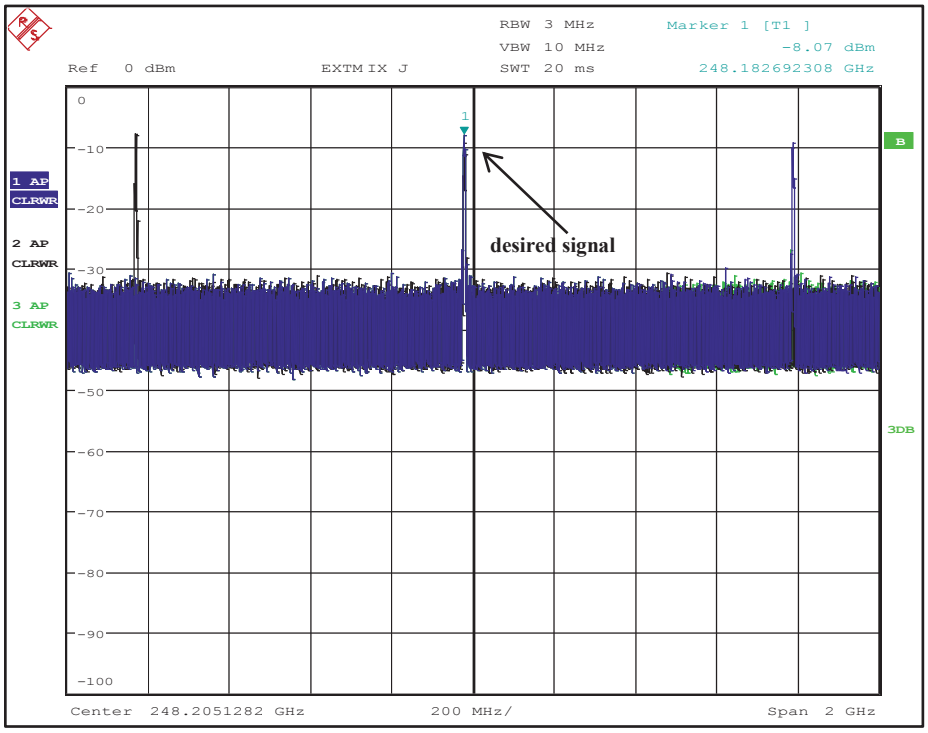


Fig. 3.13. Spectrum characterization: identification of the desired signal at 248 GHz using J band external mixer (Fig. 3.11 meas. setup #1).

3.3.3 Power

Accurate power measurements above 110 GHz are challenging due to the lack of traceable power sensors. Moreover, it is true that the power meter with power sensor provides accurate power detection, but it receives power in all other harmonics according to power sensor's bandwidth. In order to detect output power as accurately as possible, a preferred waveguide components have been used. In this work, all the circuits have been measured using an Erickson PM4 calorimeter. This meter is a wave guide based calorimeter which uses WR-10 (e.g. 75-110 GHz) wave guide input. The equation 3.14 shows the output power calculation during power measurement. The insertion losses of the probe and waveguide system are estimated given by the vendor at desired frequency bands.

$$P_{out\,(measured)} = DUT + Probe_{(WR\text{-}\,\#\#)} + Taper_{(WR\text{-}\#\#\ to\ WR\text{-}10)} + Waveguide_{(WR\text{-}10\ 90^\circ\ bend)} + Waveguide_{(WR\text{-}10\ 1''\ length)} + P_{(sensor).} \quad (3.14)$$

3.3.4 Oscillator Measurement Methodology

Characterization of the oscillator was performed in two major steps: First, the oscillation frequency was determined. For this purpose, a ground-signal-ground (GSG) wave guide probe with a sub harmonic mixer (SHM) from RPG for the desired frequency band was connected to the output. The down-converted signal was measured using a FSUP signal source analyzer from Rohde & Schwarz. The second step was to measure the peak power of the circuit. For this purpose, a GSG wave guide probe was connected to a 90-degree WR10 bend and a taper, which connects to the input of a power sensor and an Erickson PM4 power meter.

3.3.5 Multiplier Measurement Methodology

The multipliers were characterized in three steps. First, the input power of the multiplier was determined. For the input power, a signal generator from Rohde & Schwarz, a coaxial cable and a full-band WR-10 module, which includes X6 multiplier, attenuator and amplifier, followed by a ground-signal-ground (120-GSG-100-BT) WR-10 waveguide probe from GGB was characterized using a PM4 Erickson power meter. Second, output spectrum and bandwidth were determined. For this purpose, a ground-signal-ground waveguide probe with a dedicated frequency band sub-harmonic mixer (SHM) from RPG was connected to the output of the circuit and then the desired signal was detected using a Rohde & Schwarz spectrum analyzer. The next step was to measure the output power of the circuit as a function of input frequency. To extract the output power of the multiplier, a GSG waveguide probe was connected to a 90-degree WR-10 bend and a taper, followed by the power sensor of the Erickson PM4 power meter.

4 MM-Wave and Sub-THz Frequency Oscillators

This chapter deals with the design of the mm-wave and sub-THz frequency oscillators which is a very critical building block in a system. The demand for a highly efficient high output power generation and a low phase noise continues to pose interesting challenges especially for such high frequencies. First, the oscillator topology and the phase noise will be discussed. And then design and characterization of fixed frequency fundamental and harmonic oscillators on TS InP HBT and InP-on-BiCMOS technologies will be described. At the end of this chapter, a performance study of a 96 GHz fundamental oscillator using TS InP and InP-on-BiCMOS technologies will be presented.

4.1 Oscillator Circuit Topology

In the most general sense, an oscillator is a nonlinear circuit that converts DC power to an AC waveform. Most RF oscillators provide sinusoidal outputs, which minimizes undesired harmonics and noise sidebands. There are a large number of possible RF oscillator circuits using bipolar or field-effect transistor in either common emitter/source, base/gate, or collector/drain configurations [23]. The analysis of oscillators can be based on two fundamental models: the feedback model or the negative- resistance model. Various type of feedback networks lead to the well-known Hartley, Colpitts, Clapp, and Pierce oscillator circuits [23]. Depending on the oscillator configuration and characteristic, one model may be preferred over the other [28]. According to the feedback model two necessary and sufficient conditions must be met to sustain the steady-state oscillation, which is also known as the Nyquist or Barkhausen criterion. It requires that the gain around the feedback loop must be equal to unity and the total phase shift around the loop must be equal to zero or some multiple of 360 [29]. In a negative resistance model, the active circuit is modeled as a negative resistance in parallel with the resonator. If the Barkhausen criteria are satisfied this negative resistance will exactly cancel the equivalent parallel resistance of the tank circuit and will allow steady oscillation [28].

In order to achieve low phase noise, Cross-coupled or Colpitts type oscillators are commonly used. Although ring or relaxation type oscillator can be found in some applications, they show poor phase noise performance in most RF applications [30]. Furthermore, a reflection type oscillator (also called modified Colpitts) has an advantage regarding phase noise performance.

For the reflection type of oscillator, two ports of the active device are terminated by impedances in such a way that the negative resistance appears at the remaining port. And the third impedance is connected to ground to adjust the oscillation frequency. Fig. 4.1 shows the simplified schematic of a reflection-type oscillator. Each port of the active device is terminated by an external impedance to ground, denoted by Z_E, Z_B, and Z_C, respectively (see Fig. 4.1). These impedances describe the complete bias network, varactor, and also output load. To ensure oscillation startup, the product of the reflection coefficients from the active and passive parts of the circuit must be larger than unity with zero phase. This product is denoted as an open-loop gain. To evaluate this, the circuit has to be split up into two sub circuits. In Fig. 4. 1, the following oscillator is divided in to two sub circuits at the emitter of the transistor and the resulting open-loop gain is derived as [31]

$$r_P r_E = S_v \tag{4.1}$$

The reflection type oscillator has been studied widely in the literature [32, 33].

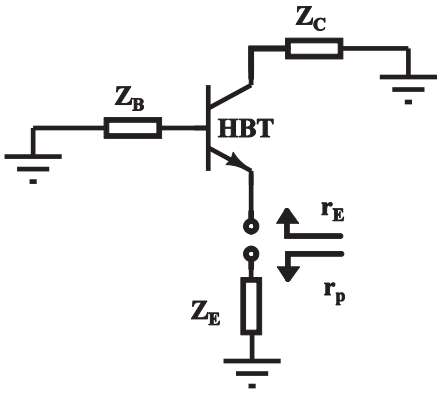


Fig. 4.1. Simplified schematic of the reflection type oscillator.

4.1.1 Phase Noise

One of the primary tasks in developing transmit and receive modules is to realize low oscillator phase noise. This is necessary not only in the development and production of state-of-the-art communications systems, but also in broadband applications such as radar. An ideal oscillator would have a frequency spectrum that consists of a Dirac delta function centered at the output frequency [37]. However, in general the real oscillators are implemented with physical devices. These devices have inherent noise which manifests itself in both the amplitude and phase of the oscillator output. The amplitude variations can be well-controlled and they have less impact on system performance. But phase variations may be in discrete

(mixer product or harmonics), or random (thermal or random noise sources) in nature [23]. Fig. 4.2 shows a typical phase noise plot with three different phase noise characteristic regions; namely, the $1/f^3$ region, the $1/f^2$ region and the frequency independent noise floor. The $1/f^3$ noise appears at very low frequency offset for active devices. Noise in $1/f^2$ is the primary concern of oscillator design. This region results from thermal noise sources in the oscillator. Finally, the flat section at high frequencies is usually seen in the measurement, and can be attributed to the noise floor of the circuit or measurement instrument. The phase noise of oscillators has been studied widely in the literature and noise modeling is discussed in the time domain [34] and also in the frequency domain [35, 36].

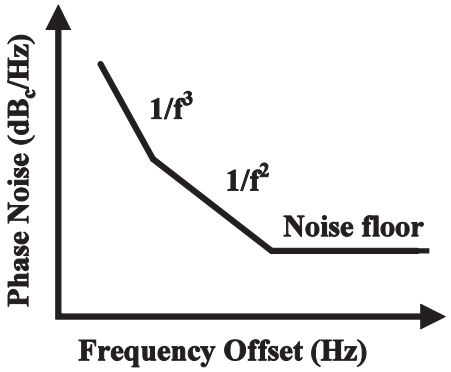


Fig. 4.2. Typical oscillator phase noise spectrum.

4.1.2 Push-Push Topology

The basic principle of push-push approach is to employ a symmetric topology with the spectral components at the fundamental frequency f_0 (and all odd harmonics) operated differentially, i.e., 180 degrees out-of-phase. The general signals of the two sub oscillators are given by

$$S_1(t) = \sum_{n=0}^{\infty} (a_n . \sin(n\omega_0 t + \varphi_n)) \tag{4.2}$$

$$S_2(t) = \sum_{n=0}^{\infty} (a_n . \sin(n\omega_0 t + \varphi_n + n\pi)) \tag{4.3}$$

The spectral components have the same amplitudes a_n and differ only in phase by $n\pi$ while n is the harmonic index. The output signal is the sum of the two sub oscillator signals

$$S(t) = \sum_{n=2,4,\ldots}^{\infty}(2.a_n.\sin(n\omega_0 t + \varphi_n)) \quad (4.4)$$

These signals are combined so that the fundamental signal and the odd harmonics cancel out due to the phase difference, while the second harmonic $2f_0$ and even harmonics add constructively (see Fig. 4.3). Hence, in a proper operating push-push oscillator, power is delivered to the load only at the even harmonics $2f_0$, $4f_0$, ….. Efficient operation of the circuit is obtained, when both sub oscillators operate at the same idling frequency f_0 and stable odd mode operation is ensured [38].

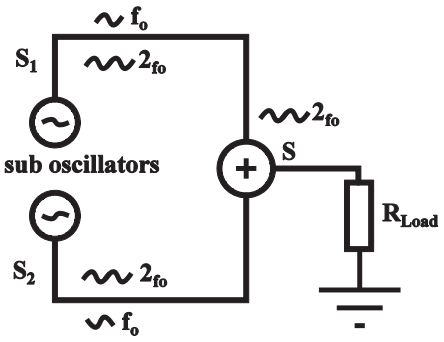


Fig. 4.3. The push-push principle.

4.2 Oscillators on Transferred Substrate (TS) DHBT Process

This section presents design and measured performance of a highly efficient 96 GHz, a 197 GHz fundamental oscillator and a 290 GHz harmonic oscillator. These oscillators have been fabricated using the transferred substrate (TS) DHBT process, which is described in Section 2.2.

4.2.1 Design and Characterization

4.2.1.1 96 GHz Fundamental Oscillator

The oscillator circuit developed uses a single emitter-finger HBT with an emitter size of 0.8 × 5 μm² and a f_T/f_{MAX} of 370/370 GHz. In order to keep power consumption as low as possible and to achieve the maximum oscillation frequency, the circuit is designed as single-transistor structure based on a reflection-type oscillator topology, with the HBT operated in common base configuration. The schematic diagram of the circuit is shown in Fig. 4.4. In this oscillator's design, the emitter port of the transistor is used as a split point to make the

oscillator sub circuits called active and passive part. The active part of the circuit consists of transmission lines TL_b, TL_{c1}, TL_{c2} and the HBT, the passive part of the circuit includes the radial stub and the transmission TL_e with a ground via.

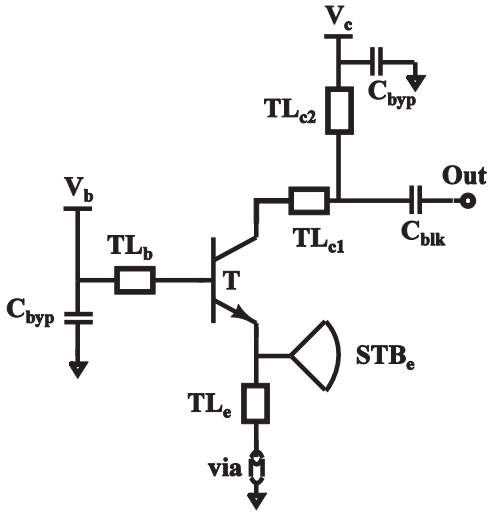


Fig. 4.4. Schematic of the 96 GHz fundamental oscillator.

A transmission-line section TL_b is used to boost the negative impedance seen when looking into the emitter and collector of the transistor (T). In addition, the impedances formed by the lines TL_{c1} and TL_{c2} on the collector side cause the transistor (T) to become more unstable. To achieve the required oscillation condition in the passive part of the oscillator, the transmission line TL_e and the parallel MIM capacitor are used to adjust the phase slope and magnitude. Fig. 4.5 shows the passive part of the oscillator circuit. In order to avoid a frequency shift due a small MIM capacitor value and its parasitic, a radial stub (STB_e) has been introduced. All transmission lines are realized as thin-film microstrip geometries. To fulfil the stable oscillation condition, the phase steepness of the reflection coefficient on the emitter port is set to zero by optimizing TL_{c1}, TL_{c2}, TL_e and the radial stub (STB_e) with a ground via. The collector lines TL_{c1} and TL_{c2} are also used for impedance matching and to maximize the output power. The circuit is designed so that it can operate without any resistive feedback or particular biasing topology, which would decrease efficiency. A blocking capacitor (C_{blk}) is included at the output to facilitate future integration with frequency multipliers or mixers. Finally, post layout simulation has been performed and optimized using ADS harmonic balance simulation tool, assisted by a 2.5D planar EM-simulator.

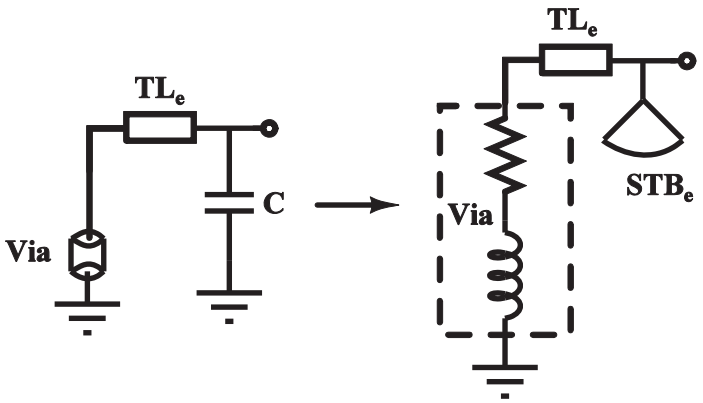


Fig. 4.5. Passive sub circuit at the emitter port of the oscillator.

Fig. 4.6 shows a chip photograph of the designed oscillator circuit. The chip area is 0.9x0.8 mm². The circuits were characterized on-wafer with the setup shown in Fig. 4.7. The output spectrum of the oscillator is investigated using a W band ground-signal-ground (GSG) with a pitch of 100 µm on-wafer WR-10 waveguide probe from GGB industries and WR-10 sub-harmonic mixer (SHM) from RPG. The principle of signal source characterization is described in Section 3.3.4. Fig. 4.8 shows the deembedded measured spectrum.

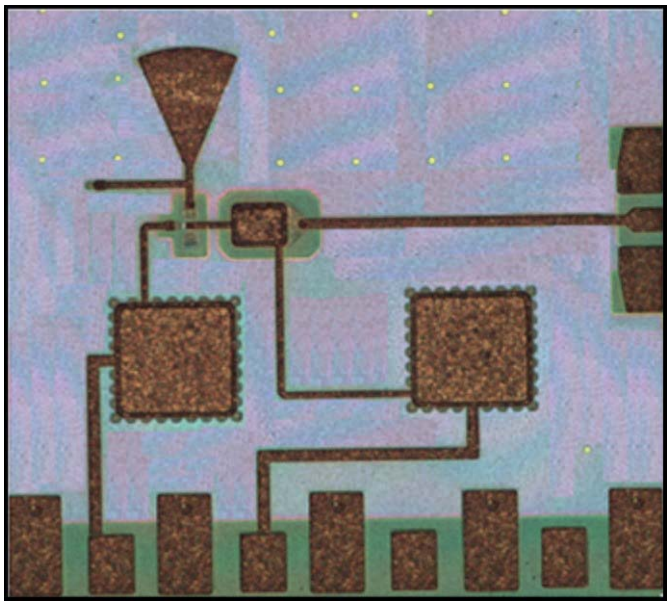


Fig. 4.6. Chip photo of the 96 GHz fundamental oscillator.

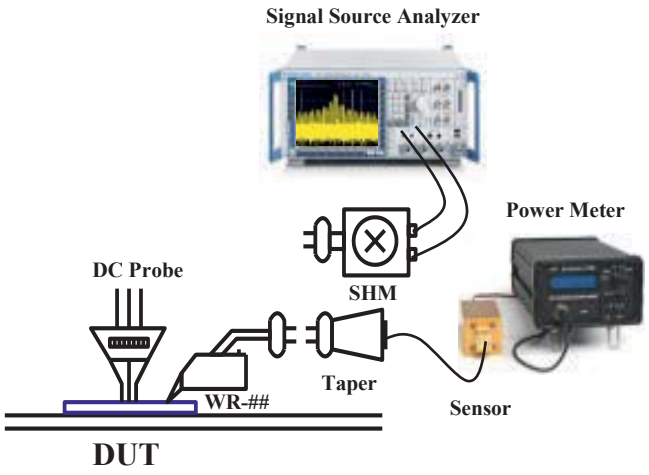


Fig. 4.7. Test setup for frequency spectrum and output power.

In order to measure actual peak power of the circuit, probe and waveguide system losses have to be deembedded. The insertion loss of the output probe is 1.35 dB as given by the vendor and the waveguide bend and tapers are estimated to contribute 3 dB insertion losses in the 96 GHz band. Accordingly, the measured output power values need to be corrected by +4.35 dB to account for the losses of probe, waveguide extension, and tapers. Thus, one arrives at an actual output power of +8.7 dBm. DC consumption is only 30 mW from a 1.6 volts power supply, which corresponds to 25 % DC-to-RF efficiency.

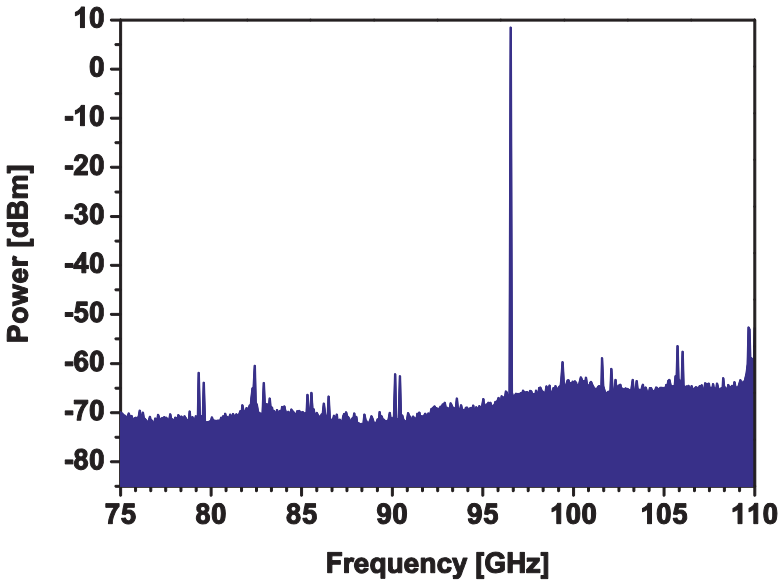


Fig. 4.8. Measured output frequency spectrum of the 96 GHz fundamental oscillator (cable and prober loss deembedded).

The phase noise measurement was performed using an FSUP signal source analyzer. A common easier and faster procedure has been followed in FSUP analyzer, where all important oscillator parameters, such as power, loop bandwidth and IF gains are set automatically in order to generate stable setting for the analyzer PLL loop. The measured phase noise characteristics of the implemented oscillator are presented in Fig. 4.9. One finds values of -90 and -118 dBc/Hz at offsets of 1 MHz and 10 MHz, respectively. According to equation 4.5, a figure of merit (FOM) of -176 and -184 is achieved, respectively. This is an excellent value for this frequency range and a free-running VCO.

$$FOM = L(\Delta f_m) - 20\log\left(\frac{f_0}{f_m}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right) \quad (4.5)$$

where $L(\Delta f_m)$ describes the phase noise at an offset frequency (Δf_m). The second term takes the oscillation frequency (fc) and the last term describes the dc power consumption. Table 4.1 benchmarks the performance of presented oscillator with other published results around 100 GHz frequency range on different technologies. As can be seen, the realized source offers high output power and achieves the best values for DC-to-RF efficiency. It has been published in [125].

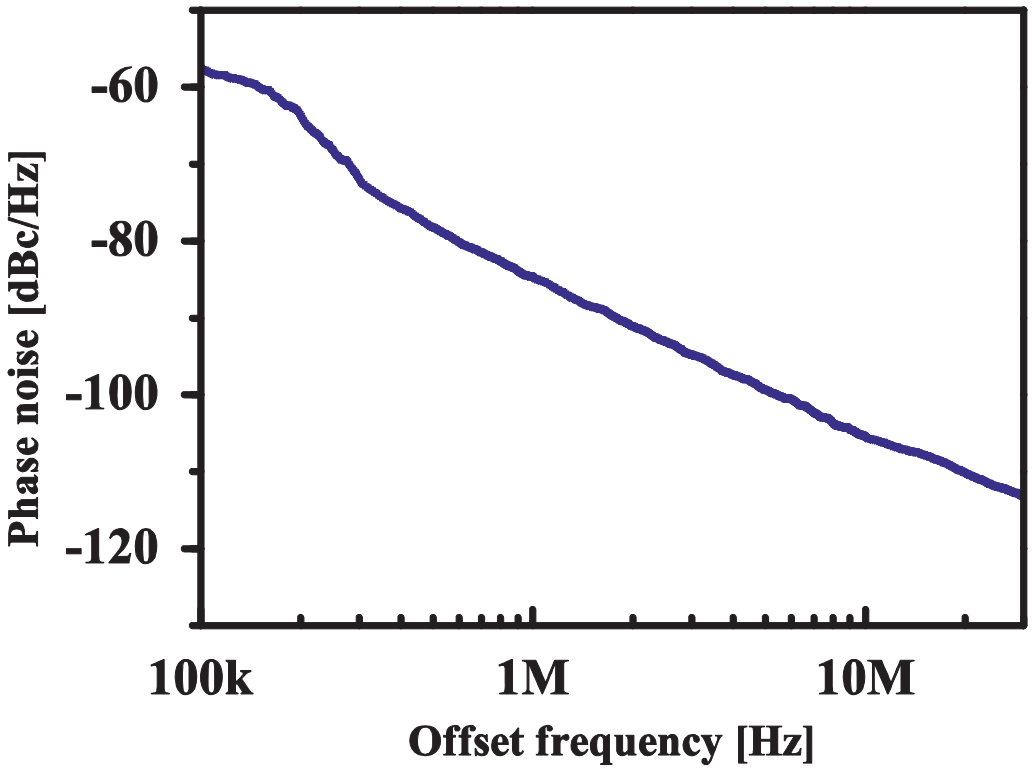


Fig. 4.9. Measured phase noise performance of the 96 GHz fundamental oscillator.

Table 4.1
State-of-the-art oscillator around 100 GHz in different technologies

Ref./ Year	Technology	Frequency [GHz]	P_{OUT} [dBm]	P_{DC} [mW]	**DC-to-RF Efficiency [%]**	Phase noise [dBc/Hz] @ Offset	FOM*
[39] 2007	1000nm InP DHBT	98	3	360	**0.55**	-90 @ 1 MHz	-164.3
[40] 2009	350nm SiGe HBT	80.75	12**	240	**6.6**	-97 @ 1 MHz	-171.3
[41] 2010	SiGe HBT	100	8	70	**9**	-88 @ 1 MHz	-169.6
[42] 2011	130nm SiGe HBT	92.5	6**	90	**4.52**	-102 @ 1 MHz -124.5 @ 10 MHz	-181.8 -184.3
[43] 2011	130nm SiGe HBT	83.6	-16	108	**0.0223**	-108 @ 10 MHz	-166.1
[44] 2013	65nm CMOS	103.3	-2	21	**3**	-112.1 @ 10 MHz	-179.2
[45] 2013	65nm CMOS	105	4.5	54	**5.2**	-93 @ 1 MHz	-176
[46] 2014	HEMT GaN	92.7	10	648	**1.54**	-90.2 @ 1 MHz	-161.4
This work	800nm TS InP DHBT	96	8.7	30	**24.7**	-90@ 1 MHz -118 @ 10 MHz	-176 -184

*calculated by using equation 4.5 ** differential output

4.2.1.2 200 GHz Fundamental Oscillator

In order to evaluate the performance of a fundamental oscillator beyond 100 GHz, a 200 GHz fundamental oscillator has been investigated. This oscillator circuit uses a single emitter-finger HBT with an emitter size of 0.8 × 5 μm² and f_T/f_{MAX} of 370/370 GHz. Similar design procedures as in Section 4.2.1.1 were followed. In this design, the TL_{e1} transmission line is used instead of a radial stub because the realized capacitor at such a high frequency is smaller compared to low frequency design (see Fig. 4.10). The complete schematic including bias network of the 200 GHz fundamental oscillator is shown in Fig. 4.10.

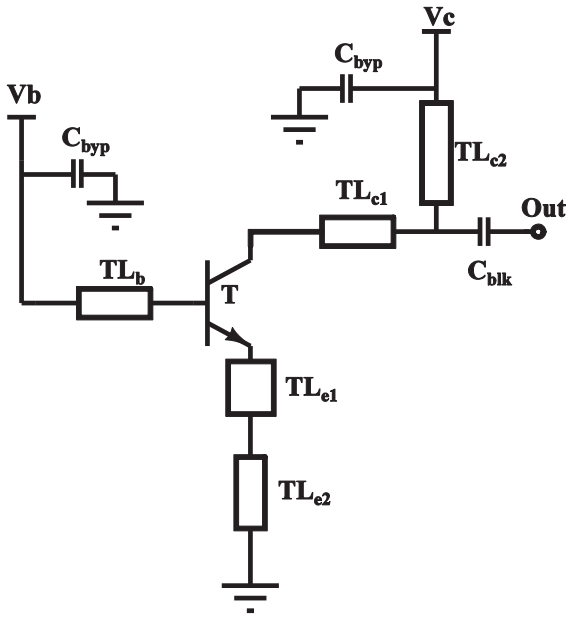


Fig. 4.10. Schematic of the 200 GHz fundamental Oscillator.

Fig. 4.11 shows a chip photograph of the designed oscillator circuit. The chip area is 0.85x0.6 mm². The circuits were characterized on-wafer with the setup illustrated in Fig. 4.7. The output spectrum of the oscillator is investigated using a G band ground-signal-ground (GSG) with a pitch of 50 µm on-wafer WR-5 waveguide probe from GGB industries and WR-5 sub-harmonic mixer (SHM) from RPG. The measurement procedure of the signal source is mentioned in Section 3.3.4. Fig. 4.12 shows the deembedded measured spectrum.

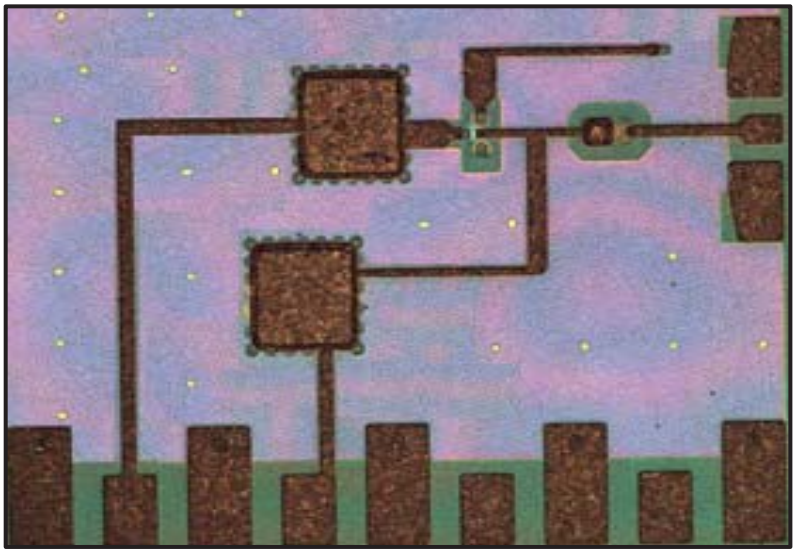


Fig. 4.11. Chip photo of the 200 GHz fundamental oscillator.

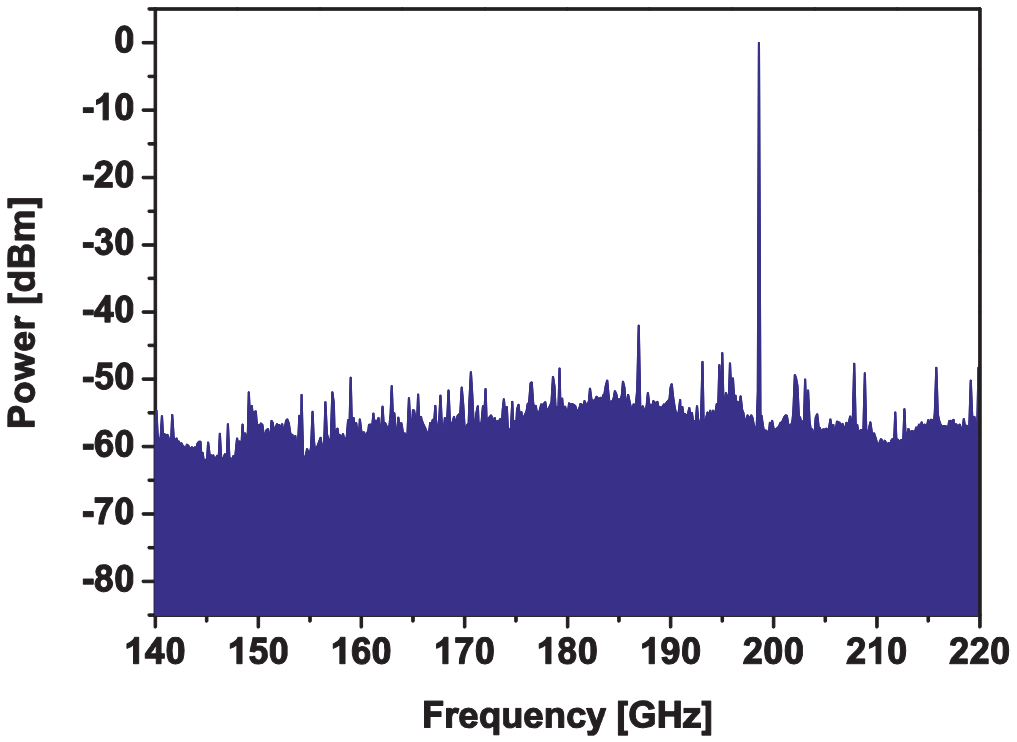


Fig. 4.12. Measured output frequency spectrum of the 200 GHz fundamental oscillator (cable and prober loss deembedded).

For power, the measured output power levels need to be corrected by a value of 7.5 dB to account for the losses of the probe, waveguide extension, and tapers. After correcting for the losses, one obtains an oscillator output power of 0 dBm. The DC power consumption is only 22 mW from a 1.4 volts power supply, which corresponds to 4.6 % DC-to-RF efficiency. Phase noise is estimated from the measured output spectrum to be below -82 dBc/Hz at 1 MHz offset. Table 4.2 benchmarks the performance of realized oscillator with other published frequency source results on different technologies. As can be seen, the realized source offers among the highest output powers in the 200 GHz frequency range and achieves the best efficiency. It has been published in [47].

Table 4.2
State-of-the-art oscillator in different technologies

Ref./ Year	Technology	Frequency [GHz]	P_{OUT} [dBm]	P_{DC} [mW]	**DC-to-RF Efficiency [%]**	Phase noise [dBc/Hz] @ Offset
[48] 2007	500nm InP DHBT	210	2	60	**2.6**	N/A
[49] 2008	35nm InP HEMT	330	-5.7	16	**1.7**	N/A
[50] 2009	90nm CMOS	196.5	-19	29	**0.087**	-94 @ 1 MHz
[51] 2010	253nm InP DHBT	267.4	-2.1	110	**0.56**	-96.6 @ 10 MHz
[52] 2010	130nm SiGe HBT	184.2	-11	95	**0.084**	N/A
[53] 2012	65nm CMOS	290	-1.2	325	**0.23**	-78 @ 1 MHz
[54] 2012	90nm CMOS	228	-6.2	86.4	**0.3**	-90.5 @ 1 MHz
[55] 2013	130nm SiGe HBT	201.5	-7.5	30	**0.64**	-87 @ 1 MHz
This work	800nm TS InP DHBT	197	0	22	**4.6**	-82@ 1 MHz

4.2.1.3 290 GHz Harmonic Oscillator

This section presents a 290 GHz harmonic oscillator. The harmonic oscillator was synthesized employing a third harmonic J-band cross-coupled oscillator topology. The oscillator is based on a fundamental cross-coupled designed at 96 GHz with the harmonic extraction using a Marchand balun. The Marchand balun is used as a band pass filter with sufficient fundamental and second harmonics rejection. Fig. 4.13 presents the simplified schematic diagram of the harmonic oscillator. The first consideration was to design a fundamental cross-coupled oscillator in both the small-signal and large-signal case. The cross-coupled oscillator circuit uses a single emitter-finger HBT with an emitter size of 0.8 ×5 μm² and ft/fmax of 280/300 GHz each. In order to keep power consumption as low as possible and to achieve the maximum oscillation frequency, the oscillator circuit is designed as single transistor structure. The transmission lines TL_{c1}, resonators using radial stubs (STB_e) and transmission lines (TL_{e1}, TL_{e2}) are optimized to generate negative impedance seen when looking into collector of the transistor pairs (T_1, T_2). All transmission lines are realized as thin-film microstrip geometries. The entire transmission line network in the layout including an additional cross connection and the vias were considered to fulfill the oscillation condition (see Fig. 4.13).

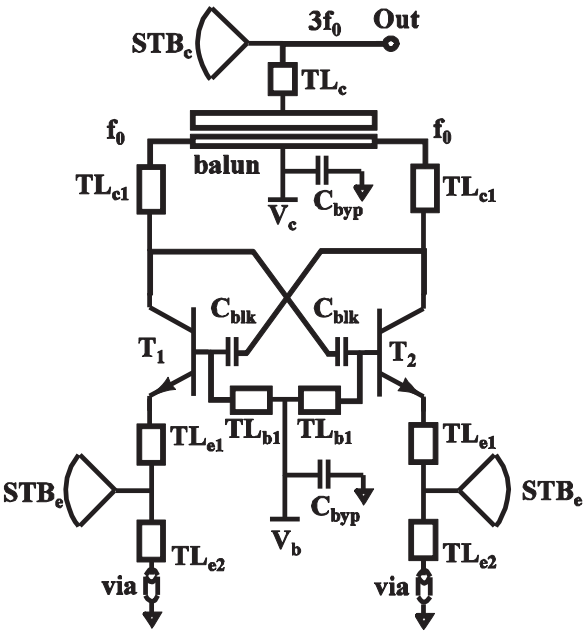


Fig. 4.13. Schematic of the harmonic Oscillator.

The capacitive coupling C_{blk} in the feedback path permits the base bias voltage to be adjusted through V_b. It also prevents the base collector junction from being forward biased, and therefore optimizes the signal amplitudes at the base nodes without driving the transistor into saturation. In this manner, the cross-coupled oscillator design is completed. After that a compact broad band Marchand balun was realized at 290 GHz center frequency. The transmission line TL_c and the radial stub STB_c are used for impedance matching and to maximize the output power. In order to avoid complex layout routing, the collector bias voltage V_c of the transistor pair (T_1, T_2) was fed through the balun. A harmonic balance analysis was performed to ensure the oscillator functionality. The transmission lines, including the Marchand balun were optimized using a 2.5D EM-simulator.

Fig. 4.14 shows the chip photograph of the harmonic oscillator circuit. The chip area of the oscillator circuit is 1×0.75 mm² including RF and DC pads. The output RF GSG pad is designed to fit both 100 µm and 50 µm pitch GSG on wafer probing. This RF pad is also optimized for future flip chip mounting. Thermal vias are visible on top of the chip photo, which extend down to the AlN substrate to spread the heat away from the transistor.

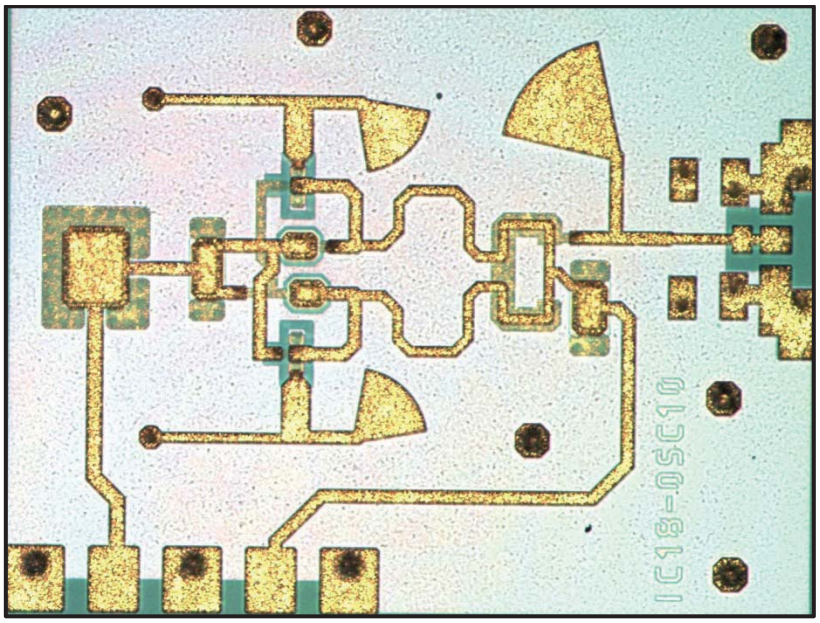


Fig. 4.14. Chip photo of the 290 GHz harmonic oscillator.

The output of the oscillator is measured using a J-band ground-signal-ground (GSG) on-wafer WR-3.4 waveguide probe from Cascade Microtech with a dedicated WR-3.4 sub-harmonic mixer (SHM) from RPG. The test setup for frequency spectrum and output power is shown in Fig. 4.7. The characterization of the circuit is described in Section 3.3.4. The measured output spectrum is presented in Fig. 4.15.

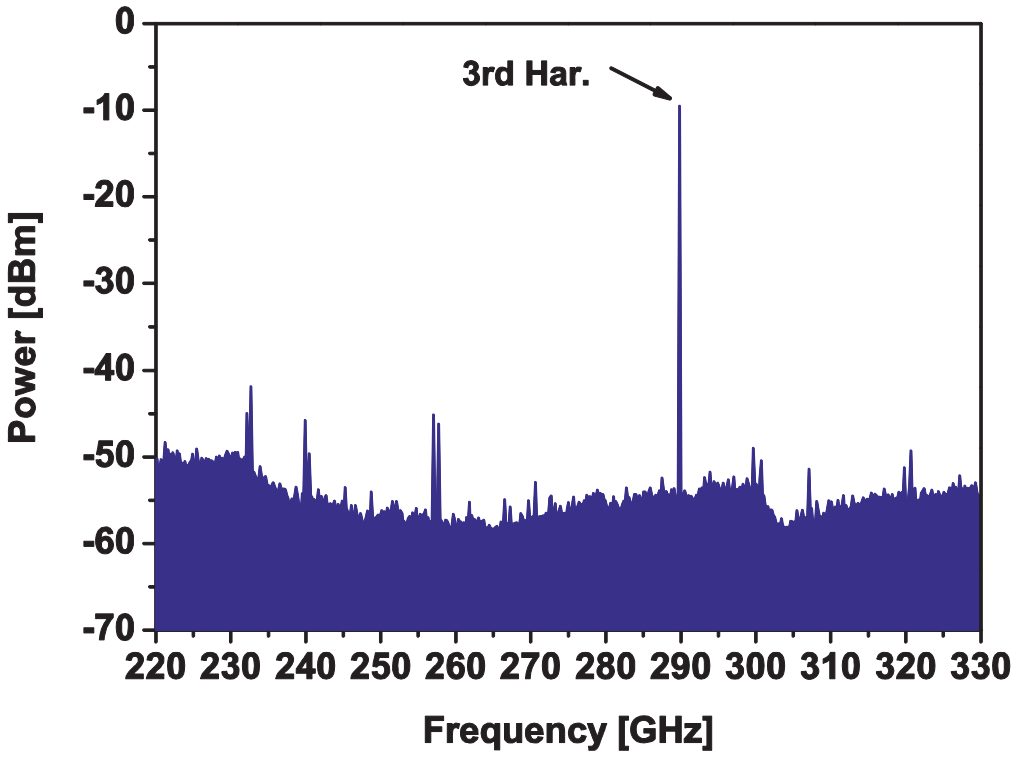


Fig. 4.15. Measured output frequency spectrum of the 290 GHz harmonic oscillator (cable and prober loss deembedded).

In order to investigate output power of the circuit, the waveguide system loss (this includes probe, waveguide and taper) needs to be estimated. The insertion loss of the output probe is 5.5 dB as provided by the vendor and the waveguide bend and tapers are considered to contribute 3 dB insertion loss in the 290 GHz band. After having all the losses, the measured output power values need to be corrected by +8.5 dB. Thus, one arrives at an actual output power of -8.5 dBm. The DC power consumption is only 28 mW from 1.5 volts power supply, which corresponds to 0.5 % DC-to-RF efficiency. An accurate phase noise measurement using a spectrum analyzer at such high frequencies is very difficult, due to the impact of the down-conversion mixer and the relatively high phase noise of the local oscillator (LO) used. Table 4.3 benchmarks the performance of realized harmonic oscillator with other published harmonic oscillator results using different technologies. As can be seen, the implemented oscillator offers good output power beyond 220 GHz frequency range and achieves the best efficiency values. It has been published in [56].

Table 4.3
State-of-art comparison reported harmonic oscillators beyond 220 GHz on different technologies

Ref./ Year	Technology	f_{MAX} [GHz]	Harmonic #	f_{OSC} [GHz]	P_{OUT} [dBm]	P_{DC} [mW]	**DC-to-RF Efficiency [%]**
[57] 2012	65nm CMOS	~200	4	290	-1.2	325	**0.23**
[57] 2012	65nm CMOS	~200	4	320	-3.3	339	**0.14**
[58] 2012	65nm CMOS	>195	3	288	-1.5	275	**0.23**
[59] 2011	130nm CMOS	135	3	256	-17	71	**0.03**
[59] 2011	65nm CMOS	~200	3	482	-8	61	**0.3**
[60] 2008	90nm CMOS	160	4	324	-46	12	**2.1e-6**
[61] 2012	90nm CMOS	~175	3	228	-6.5	86.4	**0.26**
[62] 2009	130nm SiGe	>280	4	312	-62.4	58	**0.01e-6**
[63] 2007	130nm SiGe	275	2	278	-20	132	**0.008**
[64] 2014	130nm SiGe	450	2	367	-8	64	**0.25**
[65] 2014	800nm InP TS D-HBT on BiCMOS	300	2	270	-9.5	31	**0.4**
This work	800nm InP TS D-HBT	300	3	290	-8.5	28	**0.5**

4.3 Oscillators On InP-on-BiCMOS Process

This section presents design and measured performance of two 162 GHz and 270 GHz push-push oscillators. The advantages of push-push oscillators are that they can provide relatively high mm-wave output power, exhibit low phase noise and allow extending the output frequency close to the maximum oscillation frequency of the transistors or even beyond. It can also be used for locking the oscillator with a PLL loop operating at the fundamental frequency instead of the second harmonic [66], thus saving one divide-by-two stage. These oscillators have been fabricated using transferred substrate (TS) InP-DHBT on SiGe BiCMOS process. The InP-DHBT-on-BiCMOS process offers both InP HBT and BiCMOS technologies but in this case only the InP part has been used. The InP-on-BiCMOS process is described in Section 2.3.

4.3.1 Design and Characterization

4.3.1.1 Push Push Oscillator Design

In this section, the proposed push-push oscillator was synthesized based on a reflection-type oscillator topology. The first consideration was to design one sub-oscillator in both the small-signal and large-signal case. The sub-oscillator circuit uses a single emitter-finger HBT with an emitter size of 0.8×5 µm² and f_T/f_{MAX} of 280/300 GHz. In order to keep power consumption as low as possible and to achieve the maximum oscillation frequency, the sub-circuit is designed as single transistor structure, with the HBT operated in common base configuration.

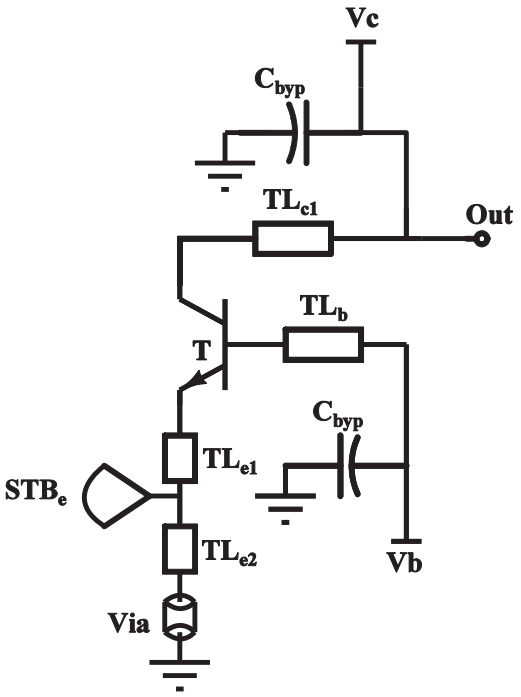


Fig. 4.16. Schematic of the sub oscillator.

A transmission-line section TL_b is used to boost the negative impedance seen when looking into the emitter and collector of the transistor (T). (see Fig. 4.16) The transmission lines are all realized as thin-film microstrip geometries. The impedances formed by the lines TL_{c1} on the collector and the line TL_e on the emitter side cause the transistor (T) to become more unstable and define the steepness of the phase. To fulfill the oscillation condition, the phase of the reflection coefficient at the emitter port is set to zero by optimizing TL_{c1} and adding a resonator using a radial stub and a transmission line with a ground via. In this manner, one sub-oscillator configuration is completed. In general, there are three possible

ways to extract the second harmonic push-push output of the HBTs. It can be taken either from the base, emitter, or collector. The largest signal swing can be obtained at the collector by directly shorting the differential output, similar to the drain-connected HEMT push-push oscillators proposed in [67]. A further advantage of directly shorting the fundamental output at the collector is that the large-signal swing at this node is reduced, enabling more robust operation in terms of base collector breakdown [66]. The circuit diagram of the whole oscillator including its bias network is drawn in Fig. 4.17. The collector lines TL_{c2} and TL_{c3} are used for impedance matching and to maximize the output power. A harmonic balance analysis was performed to ensure the push-push oscillator functionality. The transmission lines were optimized using Agilent ADS, assisted by a 2.5D planar EM-simulator.

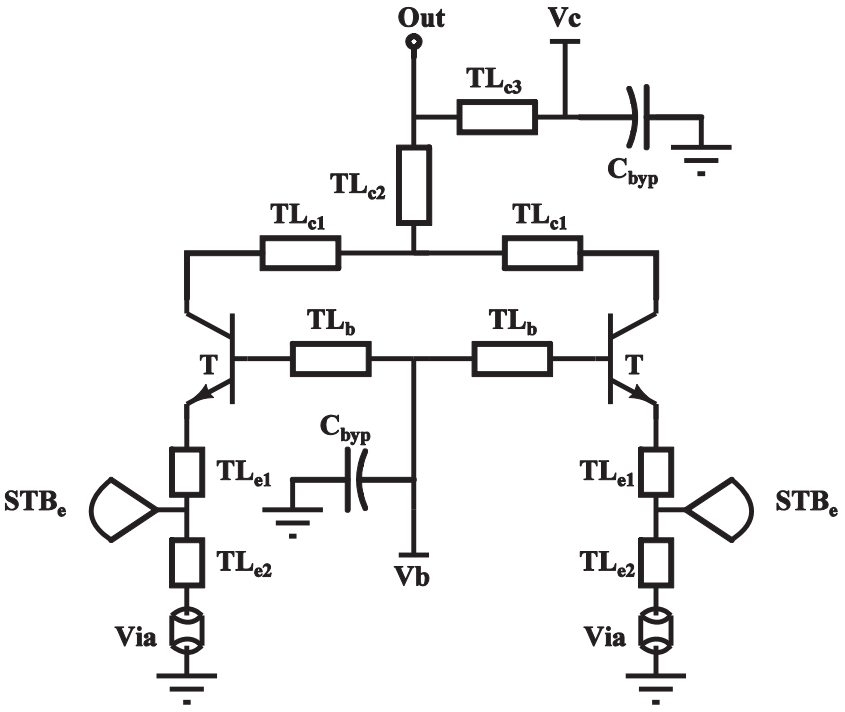


Fig. 4.17. Schematic of the push push Oscillator.

4.3.1.2 162 GHz Push Push Oscillator Characterization

Fig. 18 shows a chip photograph of the realized oscillator circuit. The chip area is 0.9x0.9 mm². The circuits were characterized on-wafer with the setup shown in Fig. 4.7. For RF, a ground-signal-ground (GSG) 220-GSG-50-BT WR-5 wave-guide probe with a WR-5 sub harmonic mixer (SHM) was used to extract the output signal and a 4-channel precision voltage source was employed for DC supply. The measurement steps of the oscillator are explained in Section 3.3.4.

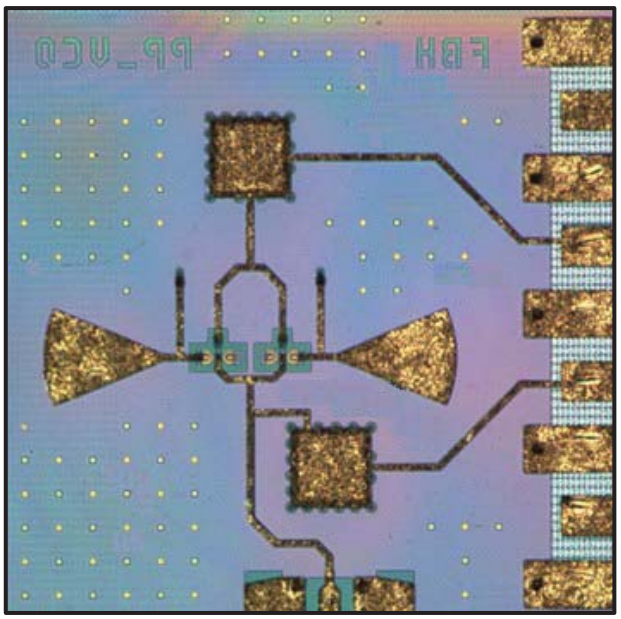


Fig. 4.18. Chip photo of the 162 GHz push push oscillator.

Fig. 4.19 shows the deembedded measured spectrum. Special care has to be taken in order to ensure that the correct spectral component is evaluated. This has been verified using the spectral position of individual harmonics and sideband signals.

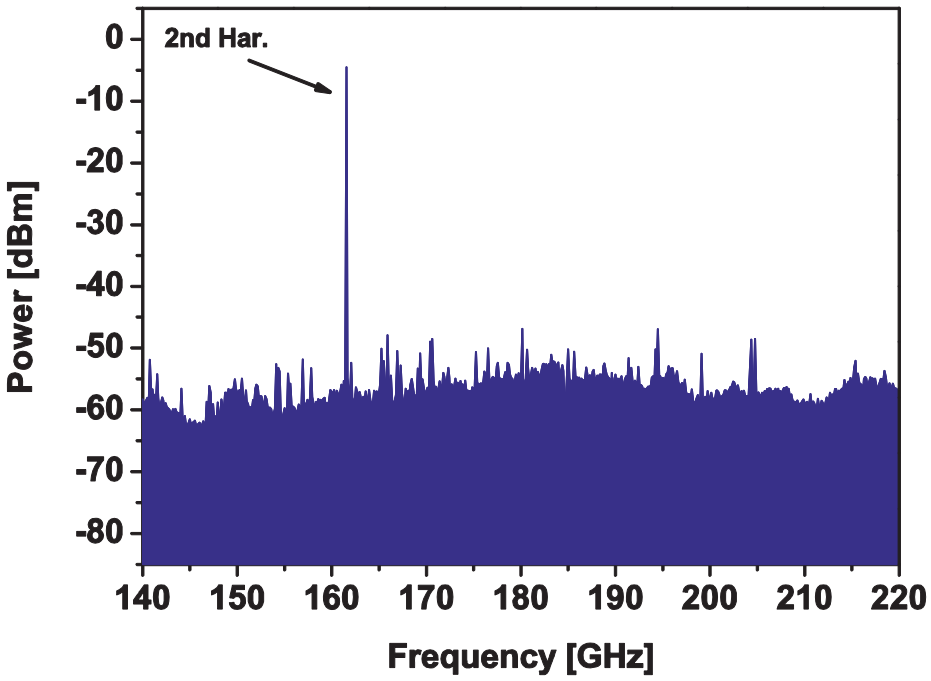


Fig. 4.19. Measured output frequency spectrum of the 162 GHz push push oscillator (cable and prober loss deembedded).

In order to extract accurate output power, the insertion loss of the output probe and the waveguide bend and tapers have to be considered. The losses are estimated to contribute 5.5 dB in the 160 GHz band. As a result, the measured output power values need to be corrected by +5.5 dB to account for the losses of probe, waveguide extension, and tapers. Thus, one arrives at an actual output power of -4.5 dBm. Here we have assumed that interface losses at the flanges etc. are negligible. The DC power consumption is only 23 mW from 1.6 volts power supply, which corresponds to 1.5 % DC-to-RF efficiency. Table 4.4 shows the performance comparison of silicon and III-V push push oscillator around 150 GHz. As can be seen, the realized oscillator attains good power efficiency.

Table 4.4
Performance comparison of silicon and III-V push push oscillator around 150 GHz

Reference	**This work**	[68]
F_{OSC} [GHz]	**162**	150
P_{DC} [mW]	**23**	170
P_{OUT} [dBm]	**-4.5**	-5
DC-to-RF efficiency [%]	**1.5**	0.2
Chip area [mm²]	**0.8**	0.5
Technology	**0.8 µm InP D-HBT**	0.13 µm SiGe HBT

4.3.1.3 270 GHz Push Push Oscillator Characterization

Fig. 4.20 shows a chip photograph of the realized oscillator circuit. The chip area is 0.9x0.7 mm². The circuits were characterized on-wafer with the setup shown in Fig. 4.7. For RF, a ground-signal-ground (GSG) i325-S-GSG-50-BT from Cascade WR3.4 wave-guide probe with a WR-3.4 SHM from RPG was used to extract the output signal. The measurement method of the oscillator is described in Section 3.3.4.

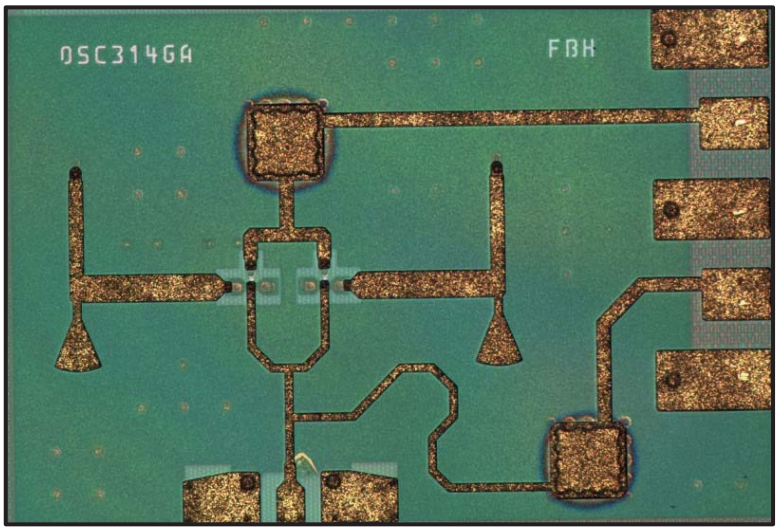


Fig. 4.20. Chip photo of the 270 GHz push push oscillator.

Fig. 4.21 shows deembedded measured spectrum. Special care has to be taken in order to ensure that the correct spectral component is evaluated. An accurate phase noise measurement using a spectrum analyzer at such high frequencies is very difficult, due to the impact of the down-conversion mixer and local oscillator purity.

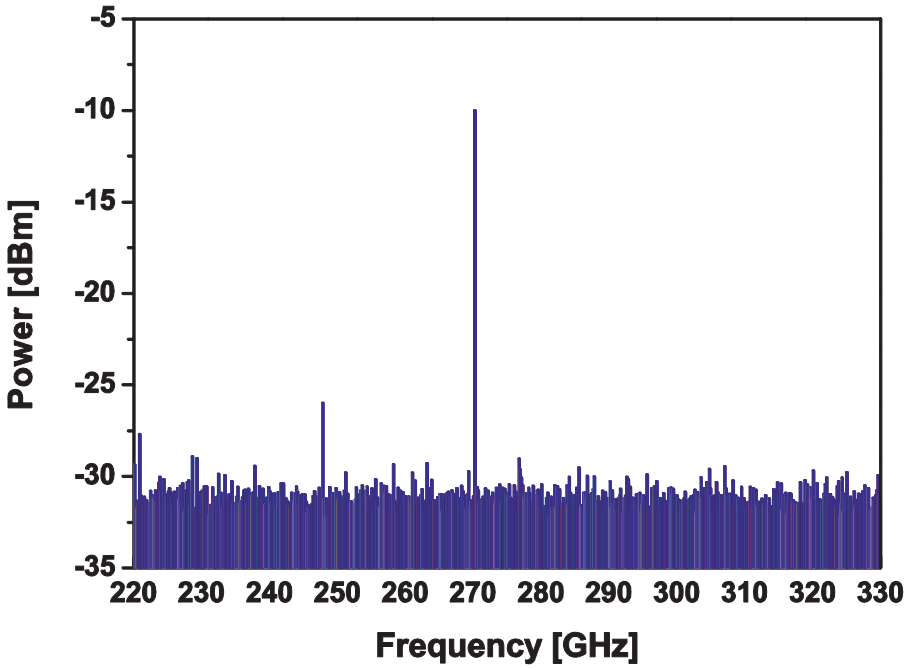


Fig. 4.21. Measured output frequency spectrum of the 270 GHz push push oscillator (cable and prober loss deembedded).

To detect accurate peak power level of the circuit, total waveguide losses need to be known. The insertion loss of the output probe is 5 dB as given by the vendor and the waveguide bend and tapers are estimated to contribute 3 dB insertion losses in the 270 GHz

band. Therefore, the measured output power values need to be corrected by +8 dB based on total losses. Thus, one arrives at an actual output power of -9.5 dBm. The DC power consumption is only 31 mW from 1.8 volts power supply, which corresponds to 0.4 % DC-to-RF efficiency. Here it was assumed that interface losses at the flanges etc are negligible. Table 4.5 benchmarks the performance of the implemented oscillator against other published push-push mm-waves sources beyond 250 GHz frequency on silicon and III-V technologies. As can be seen, the presented oscillator offers good output power at low DC power consumption and, again, record efficiency. It has been published in [65].

Table 4.5
State-of-the-art comparison of silicon and III-V push-push sources beyond 250 GHz

Ref./ Year	Technology	f_T/f_{MAX} [GHz]	Circuit Topology	f_{OSC} [GHz]	P_{OUT} [dBm]	P_{DC} [mW]	**DC-to-RF Efficiency [%]**
[66] 2007	500nm InP DHBT	405/335	Colpitts	285	-4	45	**0.8**
[69] 2007	130nm SiGe	200/275	Hartley	278	-20	132	**0.0076**
[70] 2013	130nm SiGe	300/400	Colpitts	309-330	-13.3	63	**0.07**
This work	800nm InP D-HBT (on BiCMOS)	280/300	Reflection	270	-9.5	31	**0.4**

5 Sub-THz and THz Active Frequency Multipliers

This chapter is concerned with the design of mm-wave and sub-THz active frequency multipliers, which is a very important building block in high frequency applications. Performance targets include broad bandwidth as well as high conversion gain. In this chapter, first, the active frequency multiplier design principle and topology will be discussed. And then design and characterization of active frequency multipliers (doubler, tripler and quadrupler) with passive wideband balun and filter realized on TS InP HBT technologies will be described.

5.1 Design Principle and Topology

5.1.1 Purpose of Active Frequency Multipliers

The frequency range between 100 GHz and 1 THz offers large bandwidth for high-speed communications as well as improved spatial resolution for radar sensors and imaging systems due to the short wavelength. For all these applications, the frequency source is a key component requiring specific features such as high output power within a broad frequency range and low dc power consumption. With increasing operation frequencies into the millimeter-wave range and beyond, the realization of such signal generators, possibly including a phased locked loop (PLL), are a quite challenging task. Fundamental frequency signal sources are difficult to realize, as they require high device cut-off frequencies. Frequency multiplication offers an attractive alternative, allowing for lower cut-off frequencies and standard PLL techniques with good phase-noise performance [71]. The main purpose to use active frequency multiplier is to simplify the low phase-noise signal generation by using commercially available sources with excellent phase noise performance.

Active frequency multipliers have a significant advantage over passive resistive diode or varactor based multipliers in terms of DC-to-RF efficiency and bandwidth [72]. Low DC power consumption is one of the vital issues for high frequency applications. For example, one needs to generate a 300 GHz signal with an output power of 10 dBm for a mixer's local oscillator by multiplying a 100 GHz signal. Basically, there are two ways to generate such a signal. One is using a passive multiplier chain and the other one is an active multiplier chain. The chain using passive multiplier stages needs several amplifiers to compensate for the high

losses of the multiplier chain, as a result it uses more DC power which leads to a decrease in efficiency. On the contrary, the chain using active multiplier has unity gain of each stage, so that no additional amplifier stages are required. Thus, it usually consumes less DC power compared to a passive multiplier solution.

5.1.2 Single Device Frequency Multiplier

Fig. 5.1 shows the simplified circuit diagram of a frequency multiplier that uses a common emitter HBT. The output resonator is tuned to the *n*th harmonic of the excitation frequency, so it short-circuits the HBT's collector at all other frequencies, especially the excitation fundamental frequency, f_0 by using λ/4 open stub.

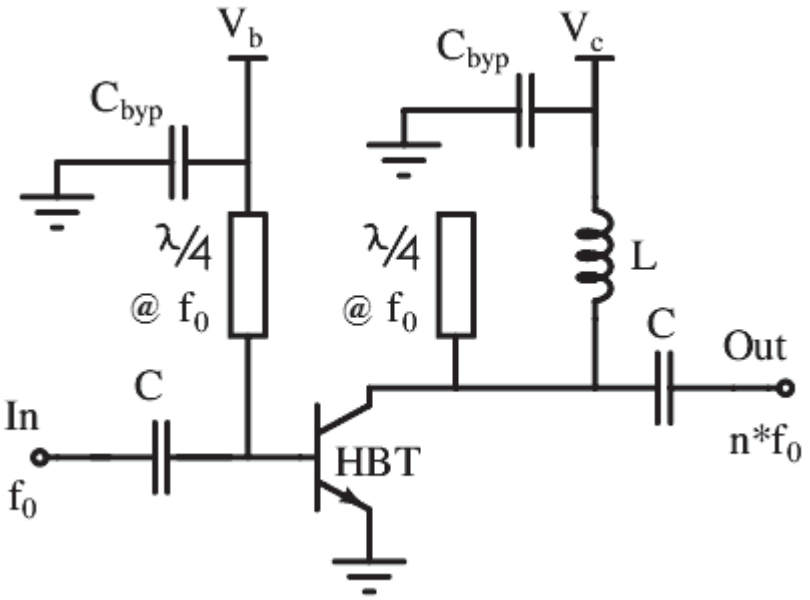


Fig. 5.1. Simplified circuit diagram of an active frequency multiplier using HBT.

In order to design a frequency multiplier, the standard procedure is to determine the appropriate biasing and the best conduction angle for the active device to generate at the output a signal waveform with the desired harmonic. The first approximation is found by calculating the derivative of the specific harmonic current with respect to the conduction angle assuming a constant transconductance. In this case, the collector current is composed of a train of cosine-wave tips that can be expressed by the Fourier series [72] as

$$I_c(t) = I_0 + I_1(\cos\omega_0 t) + I_1(2\cos\omega_0 t) \ldots\ldots I_n(n\cos\omega_0 t) \quad (5.1)$$

for $n \geq 1$

$$I_n = I_{max}\frac{4}{\pi}\frac{t_0}{T}\frac{\cos(n.\pi.\frac{t_n}{T})}{1-(2.n.\frac{t_0}{T})^2} \quad (5.2)$$

for $n = 0$

$$I_0 = \frac{2I_{max}}{\pi}(\frac{t_0}{T}) \quad (5.3)$$

If $n = \frac{T}{2}.t_0$, $n \neq 0$ then

$$I_n = I_{max}\frac{t_0}{T} \quad (5.4)$$

I_{max} is the peak collector current, and the ratio of the conduction time over the period of the input signal defines the conduction angle

$$\theta_t = 2\pi\frac{t_0}{T} \quad (5.5)$$

Fig. 5.2 shows a plot of the normalized harmonic currents as a function of t_0/T for n from n=2 to n=4. From this figure, to generate a current waveform reaching the desired harmonic is by biasing the device in class C with an optimum t_0/T (conduction angle) [73]. In general, higher order harmonic current is smaller than fundamental current (see Fig. 5.2). Therefore, difficulties may arise when choosing a low value of t_0/T. Fig. 5.2 shows that this value of t_0/T is nearly optimum for a doubler (2nd harmonic), and is also not too far from the optimum value for a tripler (3rd harmonic). But, for a quadrupler (4th harmonic) the optimum value of t_0/T is close to the zero of I_4, so a 4th harmonic multiplier having this value of t_0/T would have very low output power and efficiency. Thus, it is necessary in most cases (especially in a multiplier having an output harmonic greater than the second) to use a value of t_0/T that is larger than the optimum. Selecting t_0/T to achieve an acceptable trade-off between gain and output power is an important part of the design flow [72]. Moreover, for an efficient operation of a multiplier, short circuits are required across the transistor's output at all unwanted harmonics except for the desired one [74]. From a practical point of view, short-circuit terminations for unwanted harmonics are optimum design consideration [72].

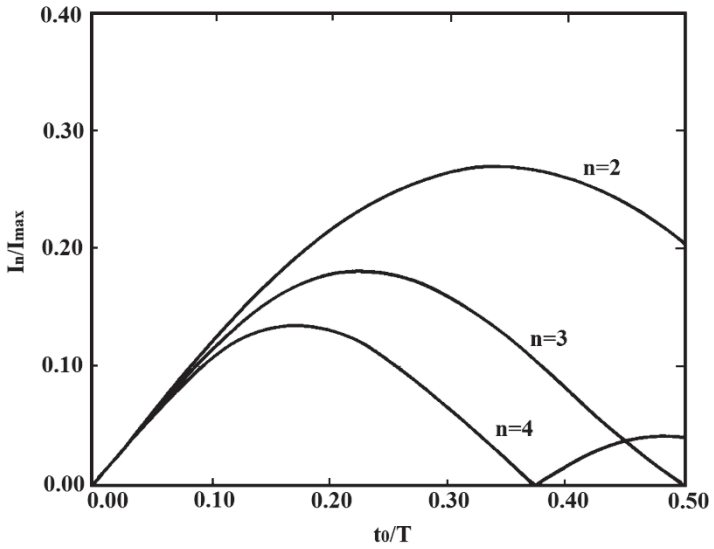


Fig. 5.2. Harmonic current components as a function of t_0/T when the current waveform is a half-sinusoidal pulse train [71].

For an odd-order multiplier design especially in a tripler design, there is another approach which consists of biasing the device in class A condition and overdriving it until there is a clipping due to pinch off on the negative swing. In this case, the collector current waveform tends to be a square waveform, for which only odd harmonics exist. A theoretical analysis of this mode of operation has been presented by [74].

Another way is to obtain a third harmonic based multiplier on the generation of a distorted collector voltage waveform. It is obtained by biasing the device in class A and presenting short circuits at the even harmonics and open circuits at the odd harmonics, except for the output third harmonic, which is matched for maximum output power. The voltage distortion approach provides higher odd harmonic current, compared to the previous approaches, as described by [73].

5.1.3 Balanced Frequency Multiplier

One of the most commonly and practically used version of an even harmonic multiplier is the balanced multiplier. This topology is also known as “push-push” multiplier. The push-push topology uses antiseries devices and exists since the days of vacuum tubes [72]. Due to an antiseries property, the connection between the two collectors forms a virtual ground; it therefore eliminates the problem of achieving a broadband fundamental-frequency short circuit at the collectors. Fig. 5.3 shows the simplified balanced or push-push active frequency multiplier circuit. The collectors of two transistors (T_1, T_2) are connected, by individual input matching networks (IMN). The collectors of the two transistors (T_1, T_2) are driven by signals having a 180-degree phase difference either by using a hybrid or a balun;

therefore, the fundamental-frequency components of the drain currents are out of phase, so each transistor effectively short-circuits the other at the fundamental frequency at all odd harmonics, creating a virtual ground (VG) at the collector. The even harmonics of the collector currents in the two transistors (T_1, T_2) have no phase difference, however, so the collector-current components at those frequencies combine in phase at the output.

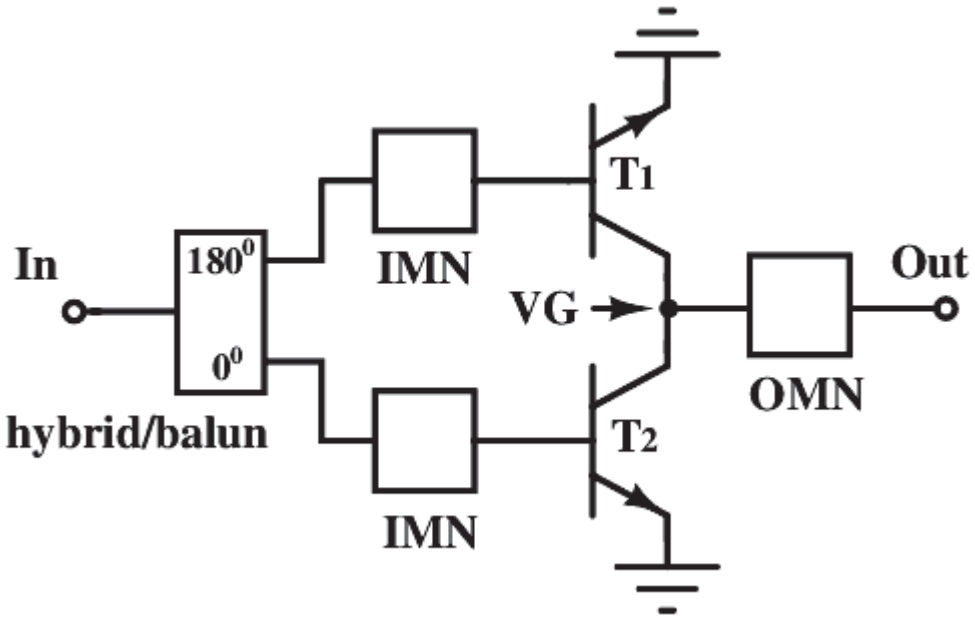


Fig. 5.3. Balanced or "push-push" active frequency multiplier.

This configuration has several advantages over a single-device circuit. First, the output matching circuit can be located close to the collector of the transistors; it need not be separated from them, as in the single-device multiplier, by the using filter. Thus, the balanced multiplier will have greater bandwidth than a single-device multiplier. Second, like other balanced circuits, a balanced multiplier has 3-dB greater output power than an equivalent single-device circuit. This can be a significant advantage when used at high frequencies, with small devices, which have low output power. Third, it is often easier to realize the load impedance of a balanced multiplier than that of a single device multiplier [72]. Also, it offers good isolation between the multiplier stages.

5.2 Design and Characterization

5.2.1 W-band Marchand Balun

Nowadays, a variety of commercial and security applications have emerged that demand for THz and sub-THz integrated systems. Wide bandwidth and high harmonic suppression are important parameters in the design of such a system. In order to achieve these targets, a differential design approach is always preferable. But differential circuits or systems require differential interconnects, which are not readily available at these frequencies. Therefore, a balun offers an attractive solution for realizing differential to single-ended transitions. Moreover, baluns are key components in design of balanced multipliers, push-pull amplifiers and mixers. Baluns can be realized as either active or passive types. Active baluns utilize transistors to overcome losses found in passive baluns and allow for compact circuits in MMIC processes. The main drawback of active baluns is that they exhibit limited bandwidth and power operation. Passive baluns can be realized using either lumped components, like capacitors and inductors or distributed elements such as transmission lines.

In recent years, different balun approaches have been proposed. Frequently, passive baluns have been realized based on spiral structures limited to low frequencies, which are large in size as well as limited bandwidth [75]-[78]. In this work, a compact broadband frequency range from 70 to 110 GHz Marchand balun is realized, using indium phosphide (InP) transferred substrate (TS) MMIC technology, according to Section 2.2. In general, the conventional Marchand balun is attractive due to its wideband performance, employing two quarter-wave length coupled line sections. But the main disadvantage is that it is larger in size. For this reason, a modified version of the conventional topology of the Marchand balun is implemented.

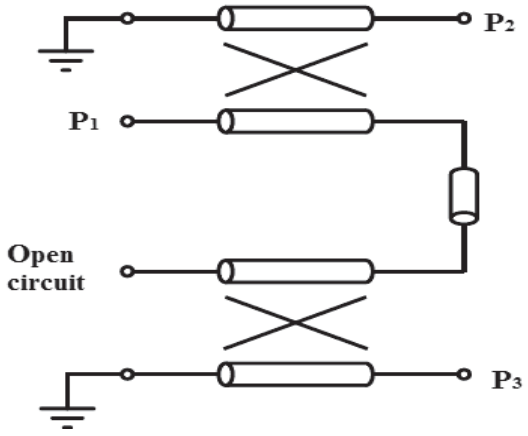


Fig. 5.4. Simplified schematic of the modified Marchand balun.

Fig. 5.4 shows the simplified schematic diagram of the improved Marchand balun. It provides balanced signals to 50 Ω load impedances at the two output ports (P_2 and P_3) when driven from an unbalanced signal at the input port (P_1). In general, the load impedances are different from 50 Ω, however. To obtain optimum performance, the balun is realized on the first thick metal layer. The bottom layer is used as common ground through ground vias. The Marchand balun was designed to fulfill the S-parameter conditions and verified with the multi substrate design tool in Keysight Technology ADS 2009. Finally, it was optimized using a 3D EM-simulator (Ansys HFSS).

The layout of the modified Marchand balun employs two different metal layers folded in a manner that reduces the size of the balun and facilitates the interconnect to a balanced design. Fig. 5.5 shows the chip photograph of the Marchand balun. The total area of the Marchand balun is (0.5×0.45) mm² including RF pads and extended lines. But the core area of the balun is only (0.35x0.16) mm². In order to avoid coupling from probe to balun, extended transmission lines have been used on both sides of the balun. To characterize the Marchand balun, two separate layouts were fabricated, connecting one output to a contact pad and the other to ground, because differential probes were not available in this frequency range. In the top layout in Fig. 5.5a, P_2 is grounded and P_3 is connected to the RF pad, the right picture in Fig. 5.5 presents the opposite case.

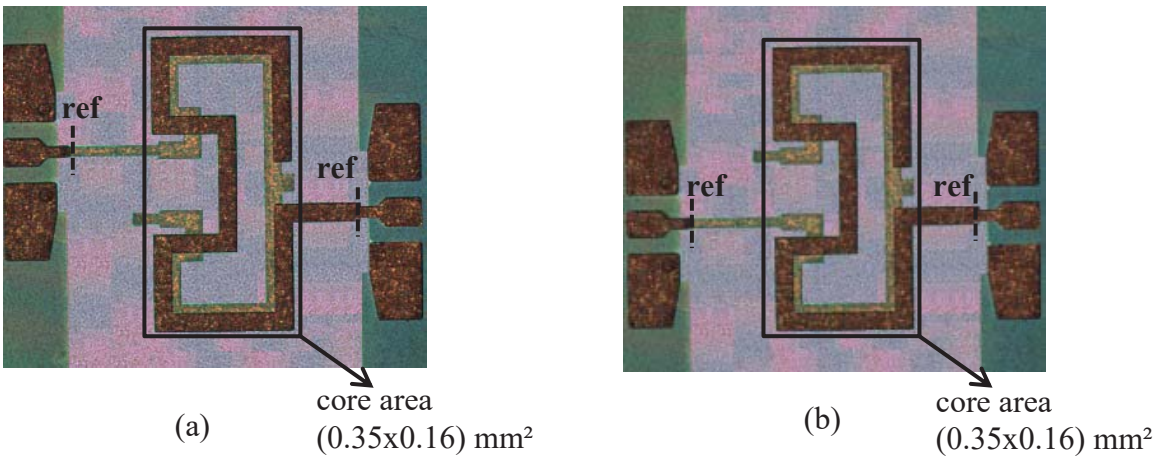


Fig. 5.5. Chip photo graph of the Marchand balun. (a) The output port P_2 is grounded (b) The output port P_3 is grounded.

The Marchand balun was characterized on-wafer by using a ground-signal-ground (120-GSG- 100-BT) WR-10 waveguide probe. The system was calibrated with the multi-line TRL (mTRL) calibration method placing the reference plane at the RF pads (see Fig. 5.5).

Characterization of the balun was performed in two steps: First, the input and output return loss as well as insertion loss of the balun in Fig. 5.5 (a) was determined. Second, same kind of losses of the balun in Fig. 5.5 (b) was measured with the same calibration and test setup. Fig. 5.6 presents the measured and EM simulated input and output return loss results as well as the insertion loss of the balun. Simulation and measurement data for the respective structures are in good agreement. The curves indicate broadband operation with less than 5 dB insertion loss and more than 10 dB return loss over at least 30 GHz. One should note that the amplitude imbalance does not exceed 2 dB in the frequency band between 70 to 110 GHz.

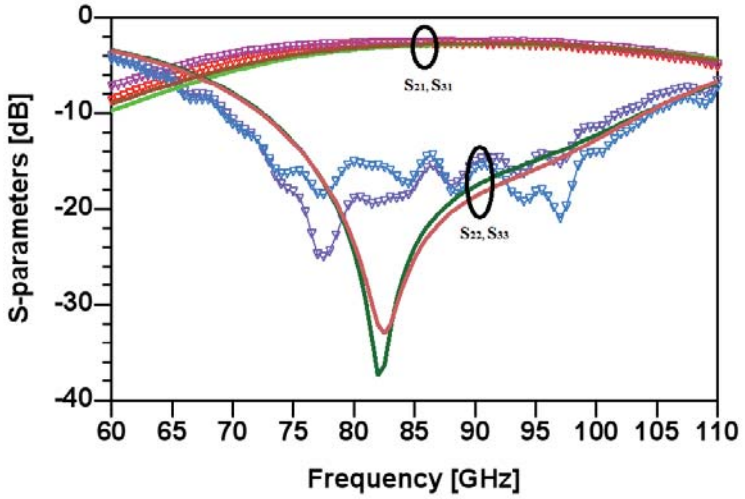


Fig. 5.6. S-parameters as a function of frequency (magnitudes): Measured (symbols) and simulated (w/o symbols) data.

Fig. 5.7 shows the phase behavior of the balun S-parameters. The simulation and experimental results are in good agreement. A phase imbalance of less than 2.5 degrees over a bandwidth of 40 GHz is achieved.

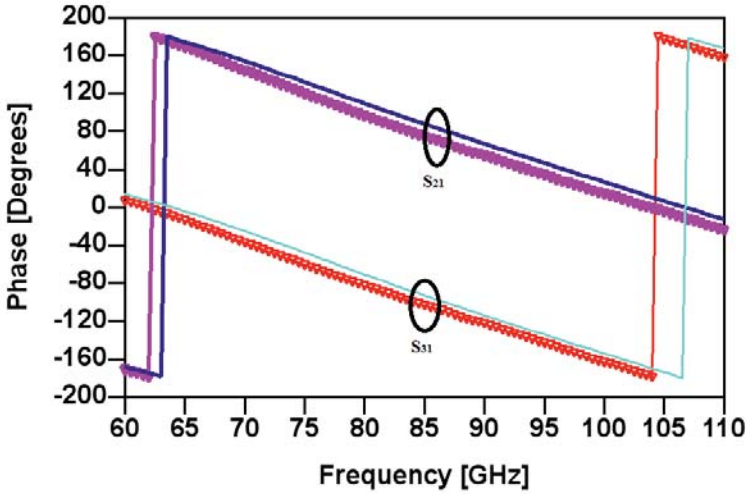


Fig. 5.7. S-parameters as a function of frequency (phases): Measured (symbols) and simulated (w/o symbols) data.

Table 5.1 compares the performance of the realized Marchand balun with other published data. As can be seen, the new balun stands out with regard to center frequency and bandwidth. Also, the core area is very small. The characteristics of the balun presented here make it an ideal candidate to be integrated with mixers and multipliers for building transmit and receive systems at W-band and also for THz frequencies, when using balanced topology for frequency multipliers and mixers. This has already been implemented and verified (see Sec. 5.2.2).

Table 5.1
Performance comparison of baluns on different technologies

Reference	[77]*	[78]	[79]	[80]	[81]	**This work**
Technology	SiGe	SiGe	CMOS	CMOS	SiGe	**InP**
Center frequency [GHz]	22.8	9.4	55	23.6	72	**90**
BW [GHz]	15	4	10	24.5	76	**40**
IL [dB]	4	6	4.2	5.6	<8	**<5**
RL [dB]	>15	>15	>15	<15	10	**>10**
Phase/mag. balance [°/dB]	6/1	0/0.3	0.9/1.2	10/1.5	7/1.5	**2.5/2**
Core area [mm²]	0.16	<0.6	0.07	0.06	0.11	**0.06**

*EM simulated results

5.2.2 140-220 GHz Frequency Doubler

A 140-220 GHz frequency doubler is realized based on a common emitter, balanced topology. It uses a 1-finger HBT with an emitter size of 0.8 × 5 μm² each and an ft/fmax of 280/300 GHz, according to the process Section 2.2. Fig. 5.8 presents the simplified schematic diagram of the balanced frequency doubler. An advantage of the balanced topology is its inherent rejection of the fundamental signal at the output. In addition, the output signal can be easily combined to obtain higher output powers, if the output is well matched. At the input, a W-band Marchand balun was used, which converts the un-balanced GSG input signal into a balanced signal.

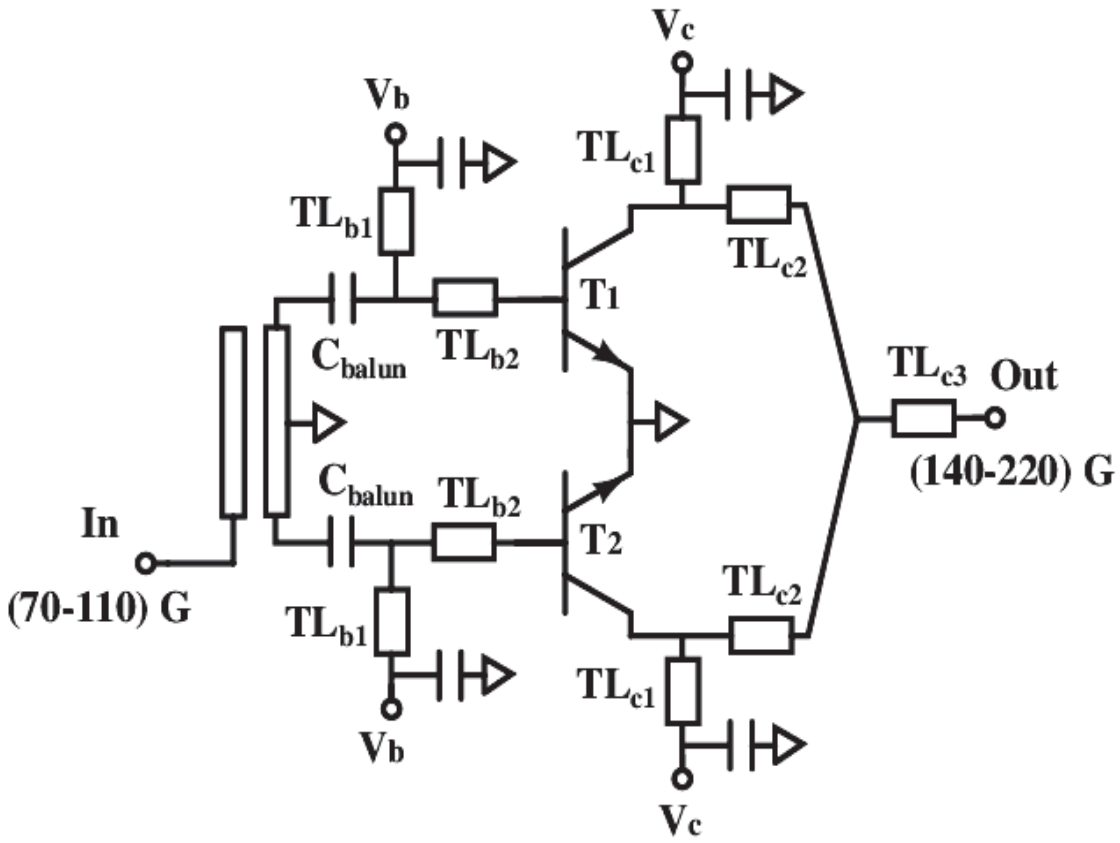


Fig. 5.8. Simplified schematic of the balanced frequency doubler.

Then, the transmissions lines TL_{b1} and TL_{b2} are used to optimize the impedance mismatch between the Marchand balun and the input of the transistors (T_1, T_2). DC blocking capacitors C_{balun} are used to facilitate base biasing with voltage V_b, without being affected by the ground plane of the Marchand balun (see Fig. 5.8). The collector lines TL_{c1}, TL_{c2} and TL_{c3} are used for impedance matching and thus to maximize the output power. All transmission lines are realized as thin-film microstrip geometries. The thin-film microstrip line layout including the Marchand balun was optimized using a 2.5D EM-simulator. Fig. 5.9 shows the chip photograph of the frequency doubler circuit. In order to avoid complex layout routing, DC bias is used through DC pads on top and bottom of the chip. The chip area of the balanced frequency doubler circuit is 1.2×0.9 mm² including RF and DC pads. The input and output RF GSG pad are designed to fit both 100 µm and 50 µm pitch GSG on wafer probing as well as suitable for flip chip bonding in further step.

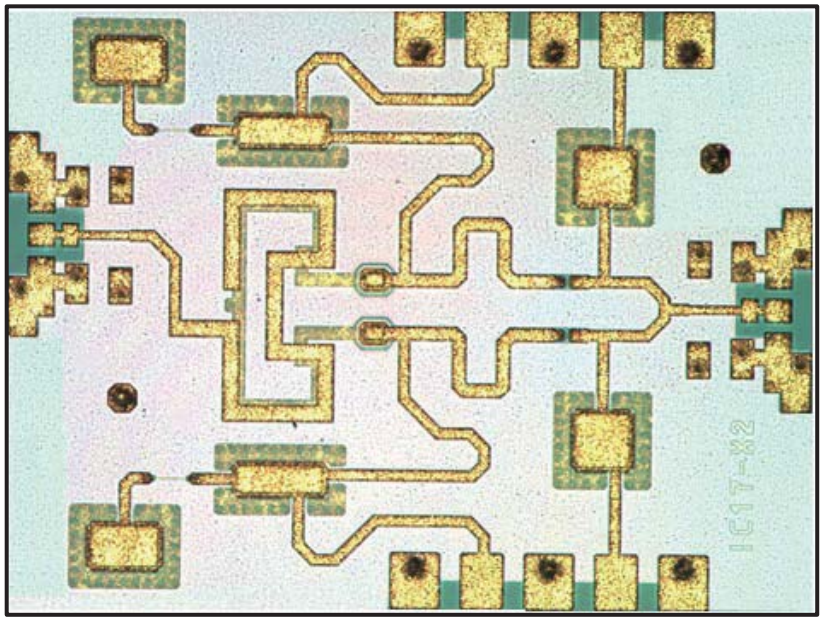


Fig. 5.9. Chip photo of the balanced frequency doubler.

The circuits were characterized on-wafer with the setup shown in Fig. 5.10. Characterization of the doubler was performed in few steps, which is discussed in Section 3.3.5. To determine output spectrum and bandwidth, a ground-signal-ground WR-5 waveguide probe from GGB with a dedicated WR-5 sub-harmonic mixer (SHM) from RPG was connected to the output of the circuit. The measured output spectrums are presented in Fig. 5.11 and Fig. 5.12.

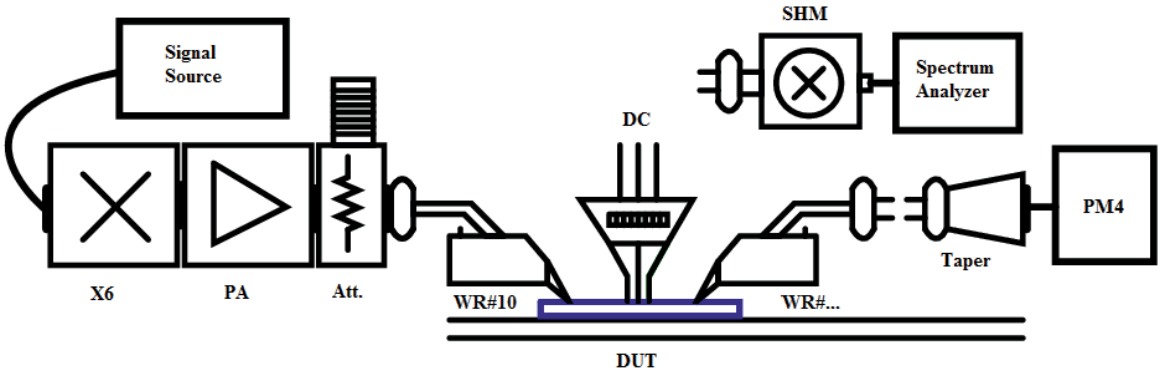


Fig. 5.10. Measurement setup of the multiplier.

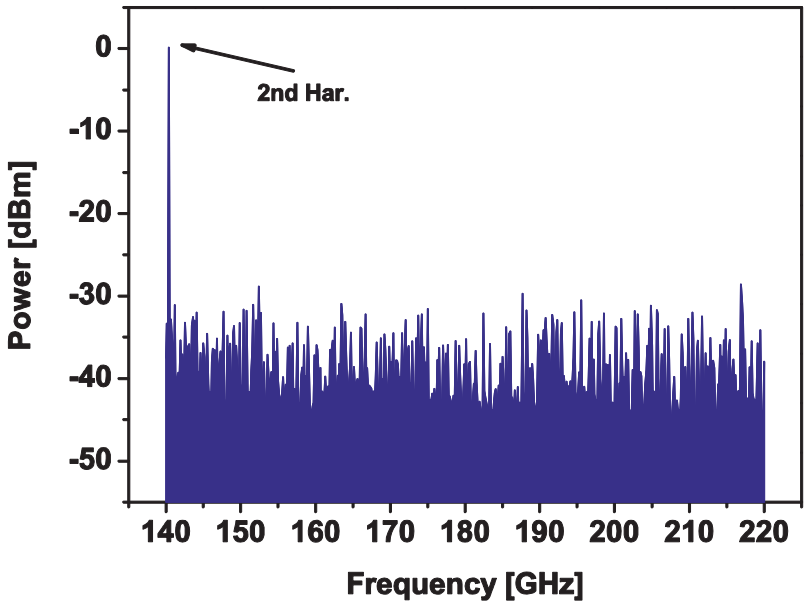


Fig. 5.11. Measured output frequency spectrum of the doubler: input frequency 70 GHz (probe loss is deembedded).

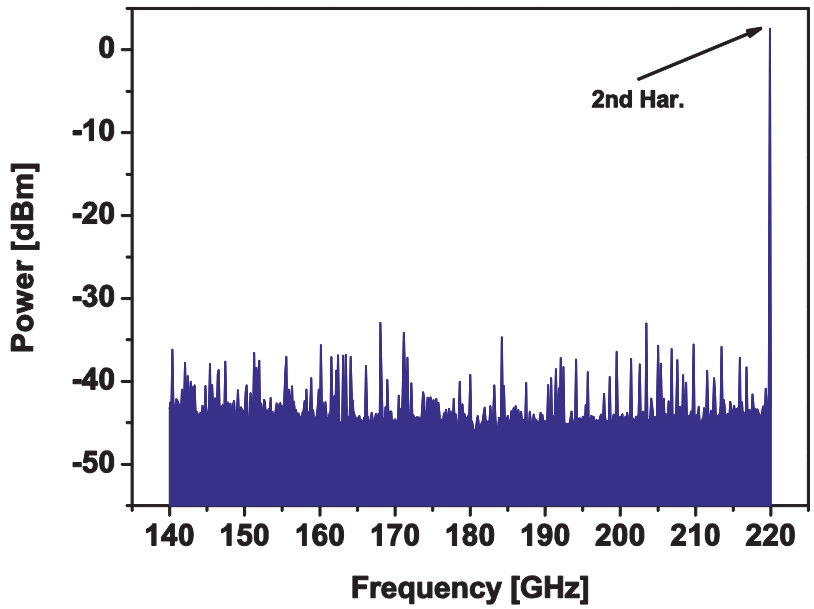


Fig. 5.12. Measured output frequency spectrum of the doubler: input frequency 110 GHz (probe loss is deembedded).

In order to evaluate the accurate input and output power of the doubler, the loss of both probes needs to be corrected. For input, the input power at the probe tips is estimated by deembedding the probe losses of 1.35 dB (data provided by the vendor). A sweep of the input frequency with a constant attenuation is shown in Fig. 5.10. The average insertion loss of the output probe is 4 dB and waveguide bend and tapers are estimated to contribute 1.5 dB insertion losses in the full G-band. Taking into account the waveguide system and probe loss,

one obtains an actual output power of +8.2 dBm at the circuit output, at a frequency of 180 GHz. In Fig. 5.13 the measured output power of the doubler circuit is plotted. As can be seen, it delivers 5 dBm ± 3 dBm in the range 140-220 GHz. The DC consumption is only 41 mW from 1.6 volts power supply. Fig. 5.13 also includes the simulated input and output power as a function of frequency. One can see that the range of values agrees quite well but peak simulated output power is shifted to higher frequencies; this can be explained by to the Marchand balun, the frequency response of which deviates from the simulated behavior.

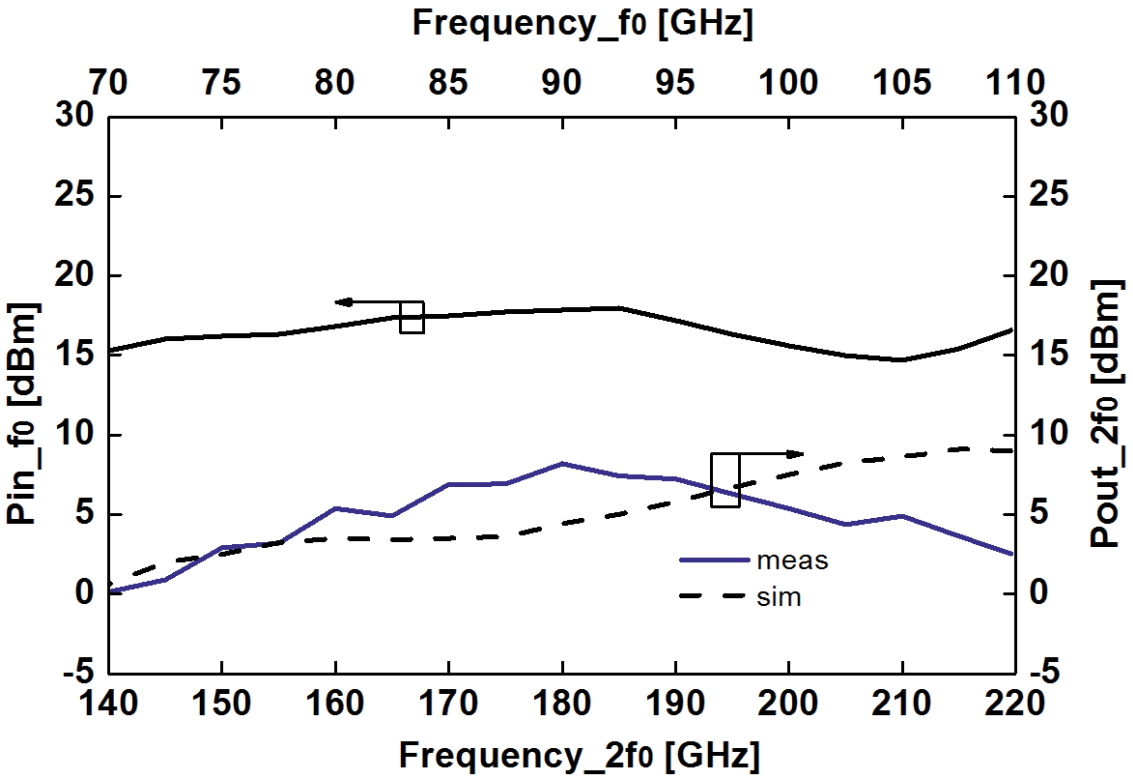


Fig. 5.13. Measured input and output power as a function of frequency of the doubler (waveguide system and prober loss deembedded).

Evaluating the decline in output power below 160 GHz we observed that the input power level varies by 2 dB over the 70-110 GHz frequency band. This variation originates from the X6 multiplier and the power amplifier in the test setup. It is important to note that the X6 multiplier is below 75 GHz out of the band specified by the vendor. Therefore, the lower output power in the frequency range below 150 GHz can be attributed to a decline in input power. The input power level to the doubler should be well above 15 dBm in order to achieve optimum conversion gain, which results in an input level at the transistors of the order of < 10 dBm. This is due to the Marchand balun at the input, which introduces more than 4 dB losses,

as can be seen in section 5.2.1. This can certainly be improved by employing a low-loss Marchand balun, which will be implemented in a future design.

Table 5.2 benchmarks the performance of our doubler with other published G-band sources on different technologies. As can be seen, the realized doubler offers the highest output powers in the G-band frequency range and achieves broadband performance. To the best knowledge, this is the highest reported output power of an transistor based active frequency doubler with wideband frequency range. The doubler circuit exhibits also the best power efficiency of 16% in this frequency range. It has been published in [71].

Table 5.2
State of art comparison of different technologies G-band sources

[Ref.]/ Year	Technology [nm]	f_T/f_{MAX} [GHz]	Circuit Topology	Frequency [GHz]	Pdc [mW]	Peak Pout [dBm]	Power Efficiency [%]
This work	**800nm TS InP HBT**	**280/300**	**Balanced X2***	**140-220**	**41**	**+8.2**	**16**
[82]/2014	130nm SiGe HBT	300/450	Oscillator+buffer	154	68	+7	7.4
[83]/2014	45nm CMOS	-/-	Balanced X2*	135-160	25	+3.5	9
[47]/2014	800nm TS InP HBT	370/370	Fundamental Osc.	200	22	0	4.6
[84]/2013	90nm SiGe	300/310	Balanced X2*	200-245	35	+2	4.5
[85]/2013	45nm CMOS	-/-	PA-multiplier array	163-180	-	+5	-
[86]/2013	800nm TS InP HBT	370/380	Single ended X2*	160-220	36	+7	14
[87]/2013	800nm InP-on-BiCMOS	360/345	VCO+X2*+PA	164	-	0	-
[88]/2012	GaAs MMIC Schottky	-/-	Schottky X2*	140-220	-	-5	-
[89]/2012	350nm SiGe HBT	170/250	VCO+ X2*	144	410	+3	0.5
[90]/2012	45nm CMOS	-/-	Balanced X2*	170-200	39	0	2.6
[91]/2012	130nm SiGe HBT	250/380	Balanced X2*	215-240	630	-3	0.1
[92]/2012	250nm InP HBT	350/600	VCO+ X4*	212-228	-	-4	-
[93]/2012	35nm InGaAs mHEMT	515/-	Balanced X2*	128-220	12.5	+1.8	12

*X2 and X4 denote, doubler and quadrupler respectively.

5.2.3 Band Pass Filter Beyond 200 GHz

Wide bandwidth, unwanted harmonic suppression and receiver noise figure are important in the design of mm-wave and sub-mm-wave transceivers, especially for the multipliers or mixers. To fulfil these targets, the band pass filter (BPF) is one of the key components. Band pass filters can be realized either as active or passive types. Active filters use active devices to overcome losses found in passive filters and allow for compact circuits in MMIC processes. The main drawback of active filters is that they have limited dynamic range, which reduces the bandwidth of the design significantly. Not only that but also it is a quite challenging task to realize in mm-waves and THz frequency ranges. Passive filters can be realized using either lumped components, like capacitors and inductors or distributed elements such as transmission lines.

So far, different band pass filter approaches have been proposed. Mostly, these band pass filters have been realized on printed circuit board (PCB), and they are relatively low frequency range, higher insertion loss, larger in size as well as offers less bandwidth [94]-[96]. In this work, a wide band miniature band pass filter is realized, using the InP transferred substrate (TS) process. It gives low insertion loss and good input and output return losses in wide frequency range from 206 to 246 GHz. The proposed distributed band pass filter realized is based on open-short-circuit resonator topology. The passive filters using lumped components such capacitor and inductor is the most attractive topology due to its wideband performance and compact in size. But the main disadvantage of this type of passive filter is that the quality factor of capacitors and inductors in this high frequency is very low. Fig. 5.14 shows the simplified schematic diagram of the band pass filter. The input and output of the filter are matched with 50 ohm load impedance. In general, the load impedances can be different from the 50 ohm. In this design top 4.5 µm thick metal layer is used. The transmission lines TL_1 and TL_2 are used as short and open circuits respectively. The transmission line TL_1 is short-circuited through a ground via. Two open-short circuit resonators are cascaded by using transmission line TL_3 (see Fig. 5.14). The band pass filter has been designed to fulfill the S-parameter condition and verified with a design tool in ADS 2009. Finally, the band pass filter has been optimized using a 2.5D EM-simulator.

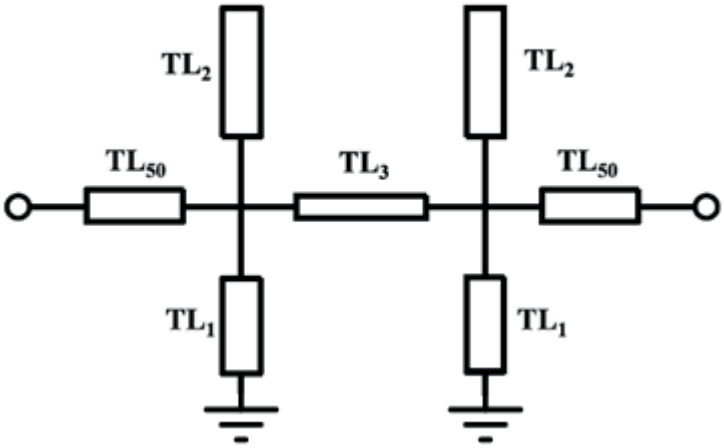


Fig.5.14. Schematic of the band pass filter.

The layout of the proposed band pass filter employs TL_3 transmission line folded in a manner that reduces the size of the filter without any coupling effect to the transmission lines TL_2. Fig. 5.15 shows the chip photograph of the band pass filter. The total area of the band pass filter is (0.8×0.6) mm² including RF pads and extended ground. But the core area of the filter is only (0.22x0.19) mm². In order to avoid coupling from probe to filter structure, extended 50 Ohm transmission lines have been introduced in both sides of the filter. The S-parameters of the band pass filter was characterized on-wafer by using Vector Network Analyzer (VNA) with R&S frequency extension modules and ground-signal-ground (GSG) waveguide probe from GGB and Cascade Microtech. The VNA was calibrated with multi line thru-reflection (mTRL) to place the reference plan at inside the circuit (see Fig. 5.15). In order to obtain comprehensive results on upper and lower side band of the filter, three different bands (W, G, and J) have been measured. This was performed by using WR-10, WR-5 and WR-3 waveguide probes separately.

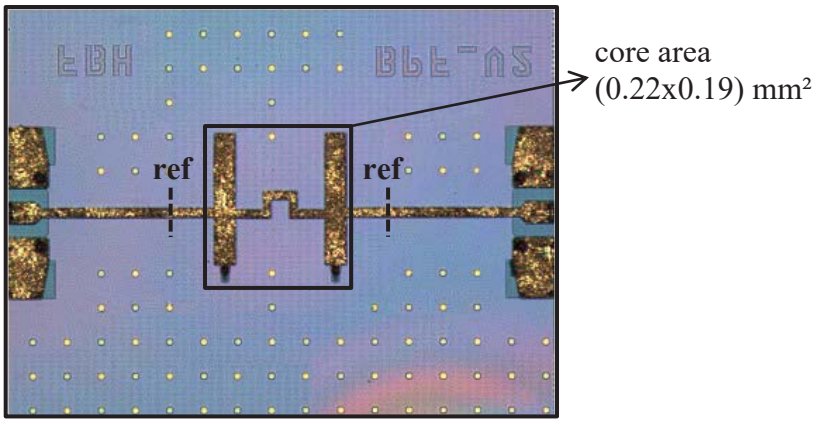


Fig.5.15. Chip photo of the band pass filter

Fig. 5.16 provides the measured (w/symbol) input and output return losses as well as insertion losses of the band pass filter up to 325 GHz, together with the 2.5D EM simulation data (w/o symbol). One could observe that simulation and measurement are in good agreement. The curves indicate broad band behavior with less than 2 dB insertion loss and more than 10 dB return losses at 225 GHz center frequency. One should note that the measured transmission co-efficient (S_{21}) in the upper side band is different than simulated. This is due to calibration uncertainties at high frequencies from the test setup. Moreover, one can expect 5-10 % of frequency shift at such high frequencies. Nevertheless, measured results achieve 18 % fractional band width (FBW) at the frequency band from 206 to 246 GHz. One should note also that there is no measured data between 110 to 140 GHz due to limitations in the bands available at the measurement set-up. However, Fig. 5.16 shows the accuracy of these measurements of three different bands using three different probes and the behavior of the transmission lines.

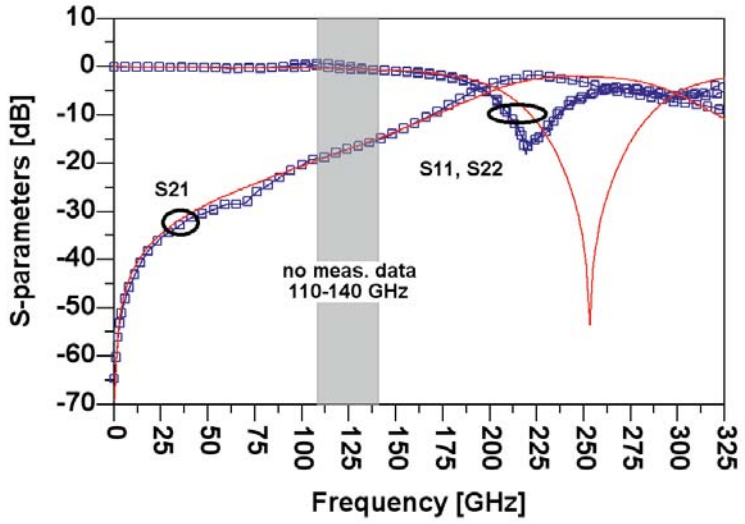


Fig. 5.16. Measured (w/symbol) and simulated (w/o symbol) S-parameters.

It is important to note that one might add more zeros to the side bands, which gives a sharper side band cut-off of the BPF. This characteristic will be implemented in a future design. Table 5.3 compares the proposed band pass filter with other published filters on different technologies. As can be seen, the realized band pass filter represents reasonable insertion loss beyond 100 GHz frequency and achieves broadband performance. Also, the core area is smaller than others. The characteristics of the band pass filter (BPF) presented here confirm that it can be easily integrated with mixers and multipliers for building transmit and receive systems at mm-waves and THz frequencies. This has already been implemented and shows the potentiality of the band pass filter in section 5.2.4.

Table 5.3
Performance comparison of band pass filter on different technologies

Reference	[97]	[98]	[99]*	[100]	**This work**
Center Frequency [GHz]	100	95	120	180	**225**
Bandwidth [GHz]	~ 10	10	20	80	**40**
Insertion Loss (S_{21}) [dB]	<3.5	<1.5	6.9	1.8	**1.8**
Return Loss (S_{11}, S_{22}) [dB]	>10	>20	>15	>20	**>10**
Technology	GaAs	GaAs	Si	CMOS	**InP**
Core area [mm²]	0.5	0.2	0.08	-	**0.04**

*EM simulated results

5.2.4 250 GHz Frequency Tripler

A single ended 250 GHz frequency tripler is realized, based on a common emitter, single-ended topology. It uses a 2-finger HBT with an emitter size of 0.8 × 5 μm² each, using the TS InP process of Section 2.2. The single HBT device is biased under class-A conditions and driven into saturation. In this condition, the HBT amplifier generates an output waveform with higher odd-order harmonics. The unwanted spurious and the fundamental and the second harmonics are suppressed by a high-pass type output matching network, followed by an open-short type band-pass filter. The input of the transistor (T) is matched using TRL_{b1} and TRL_{b2} to 50 Ω at the input frequency f_0, while the output matching network provides conjugate matching at the third harmonic $3f_0$. Moreover, to reduce the losses at the desired harmonic, λ/4 transmission lines are used to short-circuit the fundamental f_0 and the second harmonic $2f_0$ of the tripler, respectively. At the input, a resistor R_{osc} is employed to increase the K factor, thus ensuring stability. A DC blocking C_{blk} capacitor is included at the input and output to facilitate future integration with buffers or mixers.

At the output, a bandpass filter (BPF) is used to suppress all unwanted harmonics at the output of the circuit. The transmission lines and the implemented open-short band pass filter (see sec.5.2.3) were optimized in ADS, assisted by a 2.5D planar EM-simulator (Momentum). The input of the BPF is matched for the third-harmonic impedance and the output of the BPF is matched to 50 Ω.

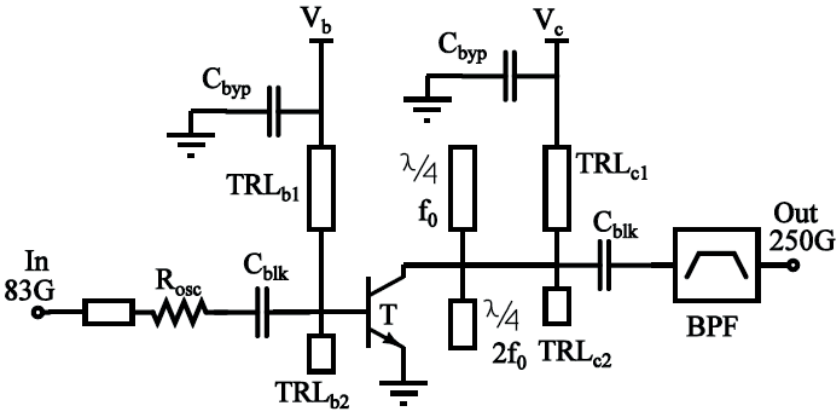


Fig. 5.17. Simplified schematic of the single ended frequency tripler.

Fig. 5.18 shows the chip photograph of the tripler circuit. The chip area of the hetero-integrated circuit is 1.5×0.9 mm². In Fig. 5.10 shows the test setup of the circuit. The measurement procedure was elaborated in Section 3.3.5. To explore the output behavior of the tripler, a ground-signal-ground WR-5 waveguide probe from GGB with a dedicated WR-5 sub-harmonic mixer (SHM) was connected to the output of the circuit. The measured output spectrum is presented in Fig. 5.19. A bandwidth more than 50 GHz is achieved.

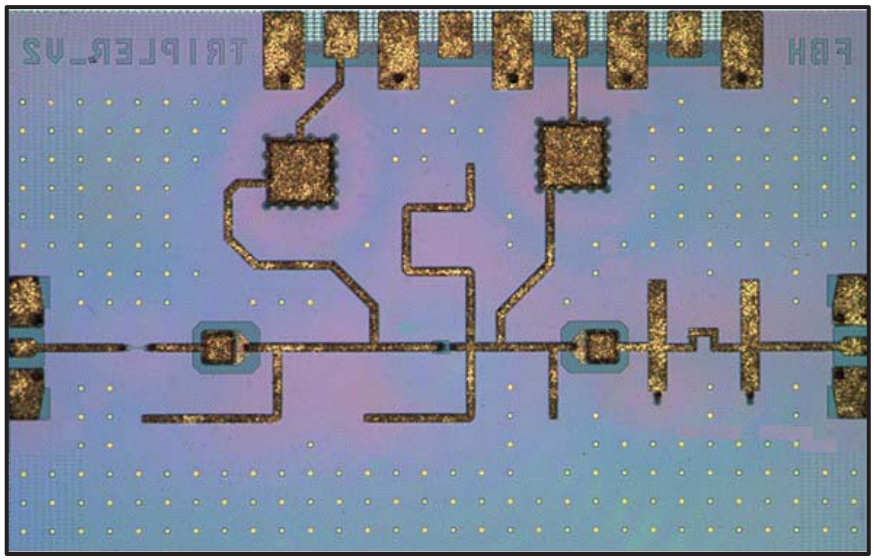


Fig. 5.18. Chip photo of the single ended frequency tripler.

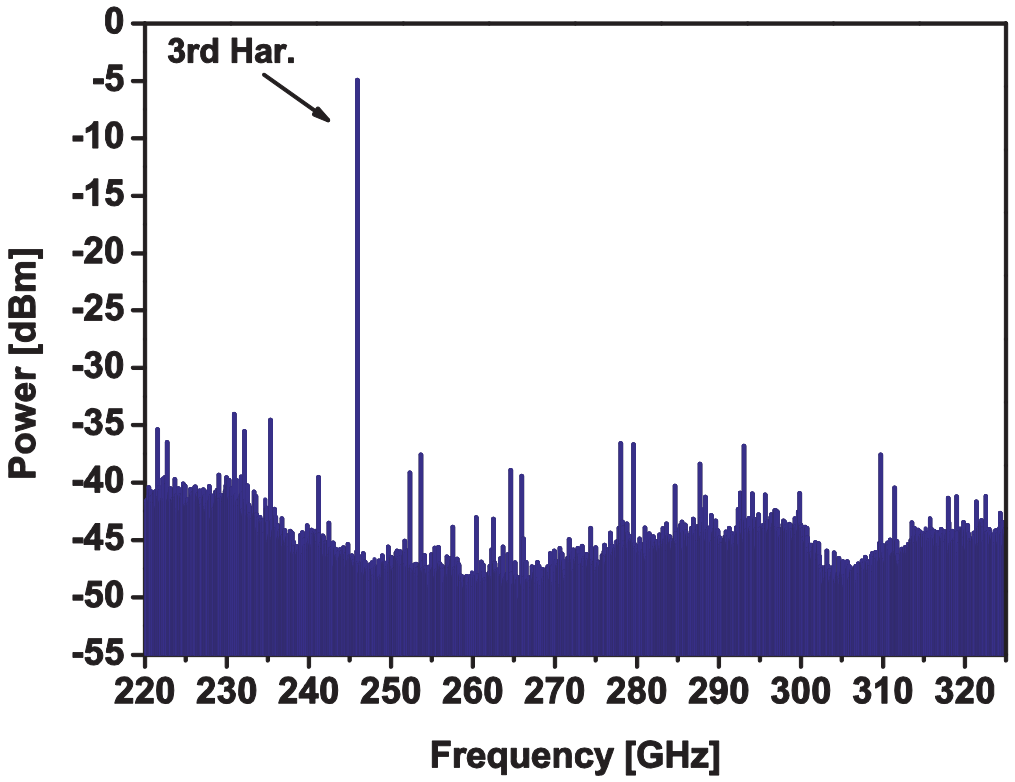


Fig. 5.19. Measured output frequency spectrum of the tripler: input frequency 82 GHz (probe loss is deembedded).

In order to extract the output power, waveguide losses have to be deembedded. The insertion loss of the output probe is 4.5 dB and the waveguide bend and taper are estimated to contribute 3 dB insertion losses in the 247 GHz band. All measurement data presented in the following are corrected by the average resulting losses of 7.5 dB. Taking into account the waveguide system and probe loss, one obtains an actual output power of -4.4 dBm at the circuit output, at a frequency of 247 GHz. The DC consumption is only 12 mW from a 1 volts power supply, which corresponds to 3 % DC-to-RF efficiency. It is interesting to see that the spurious level in the frequency range between 220-325 GHz is below - 30 dBc, which demonstrates the high spectral purity of the tripler circuit. In Fig. 5.20, the measured input and output power in the three corner frequencies (e.g. 225 GHz, 247 GHz and 261 GHz) of the tripler are plotted. Table 5.4 summarizes the main features of the realized tripler.

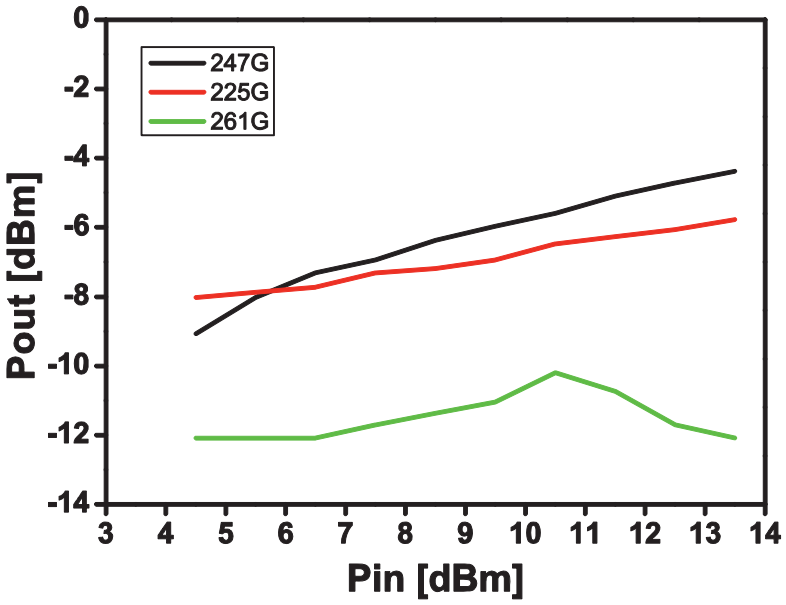


Fig. 5.20. Measured input and output power of the tripler: input frequency at 225 GHz, 247 GHz and 261 GHz (waveguide system and prober loss deembedded).

Table 5.4
Performance summary of the tripler

Frequency [GHz]	**247**
Bandwidth [GHz]	**50**
Pdc [mW]	**12**
Pout [dBm]	**-4.4**
DC-to-RF efficiency [%]	**3**
Chip area [mm²]	**1.5**

5.2.5 330 GHz Frequency Quadrupler

A 330 GHz balanced frequency quadrupler has been realized using the TS InP-DHBT process, according to Section 2.2. It consists of a Marchand balun, buffers, and a frequency multiplier. Fig. 5. 21 presents the block diagram together with simplified schematic diagram of the quadrupler. First, an 82 GHz Marchand balun was designed, which converts the un-balanced output signal from the source to a balanced signal. Then two parallel single-ended 82 GHz buffers T_1 and T_2 are realized based on common emitter (emitter area 0.8 × 5 μm²) topology, followed by a balanced quadrupler (T_3, T_4) with equal emitter size.

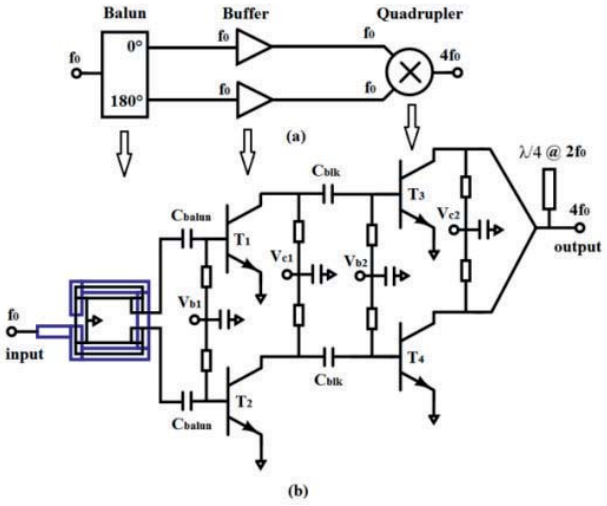


Fig. 5.21. (a) Block diagram and (b) simplified circuits schematics of the quadrupler.

In order to maintain appropriate operation of the quadrupler and the buffer stages, separate dc biasing was implemented by using V_b and V_c supply voltages. DC blocking capacitors C_{balun} are used to facilitate dc bias voltage V_{b1}, without affecting by the ground plane of the balun (see Fig. 5.21.b). At the output, the odd-order harmonics are suppressed by shunting the collectors. The unwanted 2nd harmonic is short-circuited by a λ/4 thin-film MS-line. The thin-film microstrip line layout including the Marchand balun was optimized using a 2.5 D EM simulator. Simulation results show that all unwanted harmonics are 19 dB lower than the 4th harmonic, given an input power of 17dBm at 82 GHz (see Fig. 5. 22). Fig. 5.23 shows the chip photograph of the quadrupler circuit. The chip area of the hetero-integrated circuit is 1.5×1 mm². Due to complex layout routing, DC bias is used through DC pads on top and bottom of the chip.

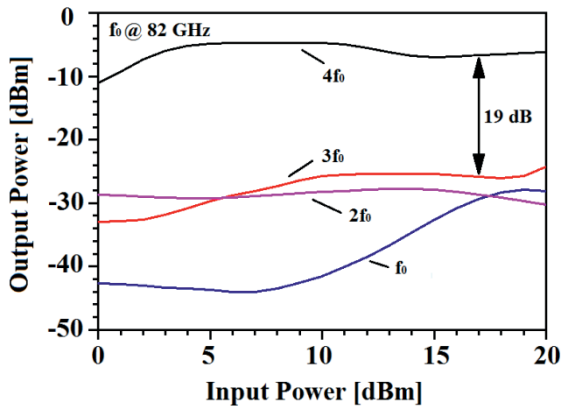


Fig. 5.22. Simulated harmonics versus input power at 82 GHz.

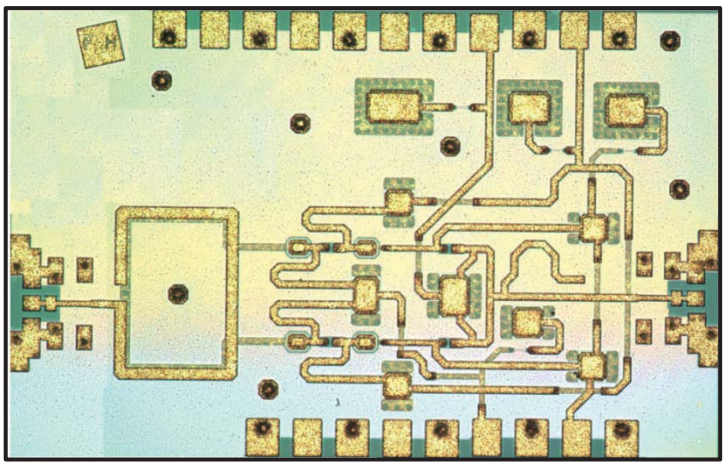


Fig. 5.23. Chip photo of the single ended frequency quadrupler.

The circuits were characterized on-wafer with the setup shown in Fig. 5.10. In Section 3.3.5, the measurement procedure of the circuit is described. The output of the quadrupler was realized using ground-signal-ground (i325-S-GSG-50-BT) WR-3.4 waveguide probes and a sub-harmonic mixer WR-3.4. Fig. 5.24 presents the measured output spectrum. During spectrum measurement 90 GHz bandwidth was achieved.

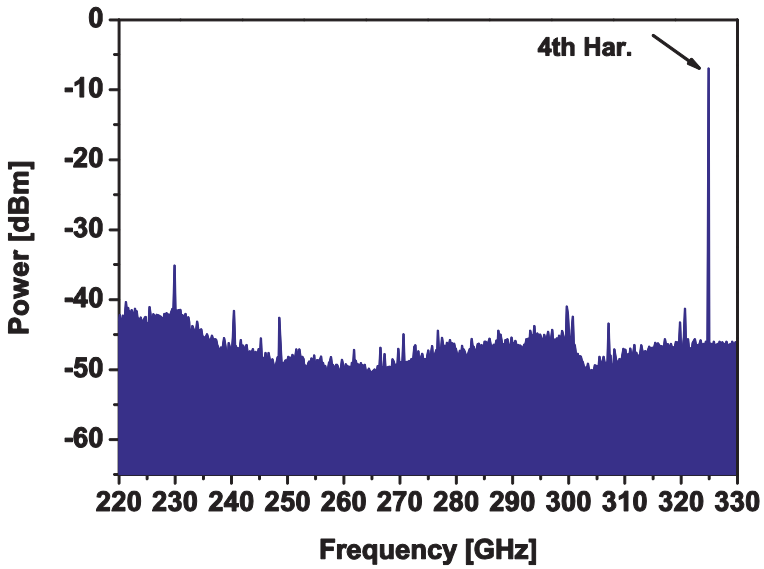


Fig. 5.24. Measured output frequency spectrum of the quadrupler: input frequency 81.5 GHz (probe loss is deembedded).

The accurate output power of the circuit was determined by correcting the losses from the waveguide system. The insertion loss of the output probe is 6.5 dB at 325 GHz as given by the vendor, waveguide bend and taper s are estimated to contribute 3 dB insertion loss in the 325 GHz band. All measurement data presented in the following is corrected by the resulting

attenuation of 9.5 dB (waveguide system and probe loss as given by vendor). Taking into account the waveguide system and probe loss, one obtains an actual output power of -7 dBm at the circuit output, at a frequency of 325 GHz, at an input power of 17 dBm with 24 dB conversion loss. The measured output power is 2-3 dB lower than simulated, which still demonstrates a good agreement at these frequencies. The total DC consumption including buffer is only 40 mW from 1.6 volts power supply. In Fig. 5.25.a the measured output power of the circuit is plotted.

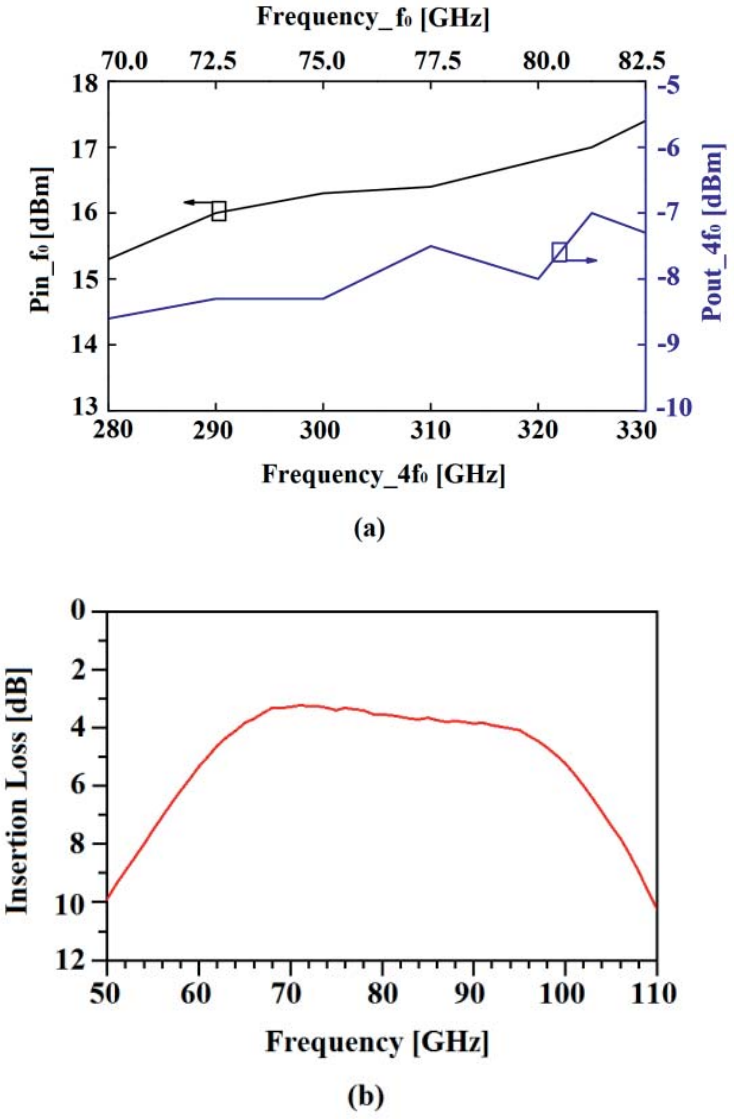


Fig. 5.25. (a) Measured input and output power as a function of frequency of the quadrupler (waveguide system and prober loss deembedded) and (b) Measured insertion loss of the Marchand balun.

During measurement, we observed that the input power level variation and test setup limitation over the 75-110 GHz frequency band (see Sec. 5.2.2). Therefore, the decrease in

output power in the frequency range between 280 to 300 GHz can probably be associated to a reduction in input power. Moreover, due to limitations of test setup, measurements below 280 GHz and beyond 330 GHz could not be performed. The Marchand balun at the input is employed for matching and input power optimization purposes. It introduces more than 4 dB loss at the input, as can be depicted in Fig. 5.25.b for the measured insertion loss of the Marchand balun. Table 5.5 benchmarks the performance with other recently published active multiplier based THz sources around 300 GHz in different technologies. As can be seen, the realized multiplier based source achieves the best power efficiency, at relatively high output power. It has been published in [124]. A few sources [112], [115], [123] deliver higher output power, but in those case buffer stages were used to increase input power level of the multiplier. It is also important to note that those sources were designed by using either second ($2f_0$) or third ($3f_0$) order harmonic extraction, but the presented source in this work is based on fourth ($4f_0$) harmonic. In general, the most dominant harmonic components are the lower order harmonics (see Sec. 5.2.1).

Table 5.5
Multiplier based THz sources around 300 GHz on different technologies

Reference	[122]	[116]	[123]	[112]	[115]	**This work**
Technology	45nm SOI CMOS	35nm mHEMT	35nm mHEMT	130nm SiGe HBT	120nm SiGe HBT	**800nm TS InP-DHBT**
Circuit Topology	VCO+ Tripler	Tripler	Multiplier chain	Multiplier chain	VCO+Buffer +Doubler	**Quadrupler**
Frequency [GHz]	285	324	320	325	290	**325**
Pdc [mW]	561	650	-	430	167	**40**
Peak Pout [dBm]	-7	-8.8*	-5	-3	-1.7	**-7**
Efficiency [%]	0.04	0.02	-	0.12	0.4	**0.5**

*average power

6 Hetero-Integrated Sources

This chapter will deal with the design of sub-THz and THz hetero-integrated signal sources, which is very important building block for such high frequency system. First, the goal of the hetero-integration and design consideration of an optimum transition will be discussed. And then design and characterization of hetero-integrated signal sources based on heterogeneous process will be described.

6.1 BiCMOS-to-InP Transition

In the hetero-integrated circuit design, the transitions between BiCMOS and InP part represent one of the most important features. The main issues are to optimize them with regards to misalignment between the BiCMOS and InP wafers and to parasitic effects. Optimization is performed by electromagnetic (EM) simulations employing the 3D solver CST Microwave Studio. The parameters available are via diameter, landing pad and ground opening sizes. The influence of the latter one is rather strong due to the capacitance between the landing pad of the signal line on the TM2 level and the ground (M1 GND). To avoid the capacitance to M1 GND a square opening is realized with an optimum width of 25 µm (see Fig. 6.1).

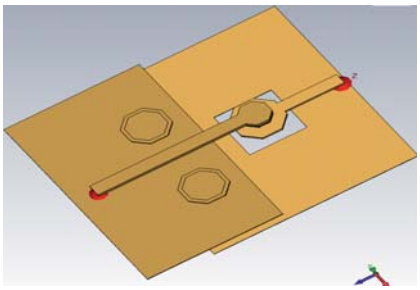


Fig. 6.1. Transition region of the GND opening in M1.

Another major problem in the design is the possible shift of the layers in the InP process relative to the structures of the BiCMOS process, caused by misalignment during wafer bonding. But even if one considers a maximum of 15 µm shift in any direction, the resulting changes remain negligible (see Fig. 6.2). More details of the transition can be seen in [101], [107].

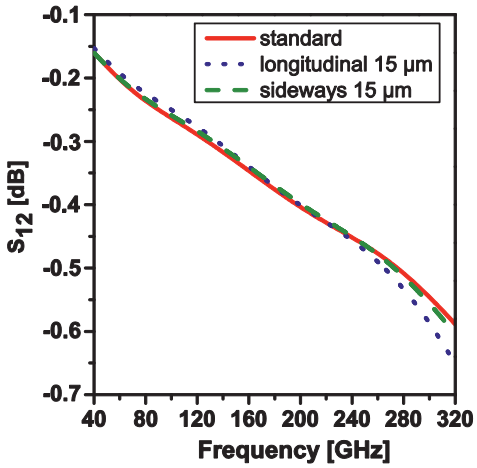


Fig. 6.2. Insertion loss for shifted sideways and longitudinally by 15 µm as well as standard version against frequency.

The resulting interconnects performance is excellent: EM simulation data and experimental verification show that a back-to-back structure with two interconnects including a line of 1250 µm length in BiCMOS exhibits a return loss RL above 12 dB from DC to 220 GHz and an insertion loss IL below 1 dB up to 220 GHz [100]. In a more-in-depth investigation, the fabrication of the transitions has been verified for potential misalignment and connection errors using a test structure with a chain of 10 transitions, as illustrated Fig. 6.3. For comparison, a further structure with a 1250 µm long transmission line length is included. The structures were characterized from 220 GHz to 325 GHz. Fig. 6.3 presents the measured and simulated insertion loss (S_{21}) data of the test structure (transition chain with ten transitions) and the 1250 µm long line (G_2) on the InP part. One observes that simulation and measurement for the respective structures are in good agreement. Fig. 6.3 shows also the measured insertion loss (S_{21}) of three samples across the wafer. In order to obtain the insertion loss (IL) per transition, it is necessary to subtract the losses of the 1250 µm transmission line and to divide by the number of transitions. This leads to an estimated IL of less than 0.5 dB per transition from 220 GHz to 325 GHz.

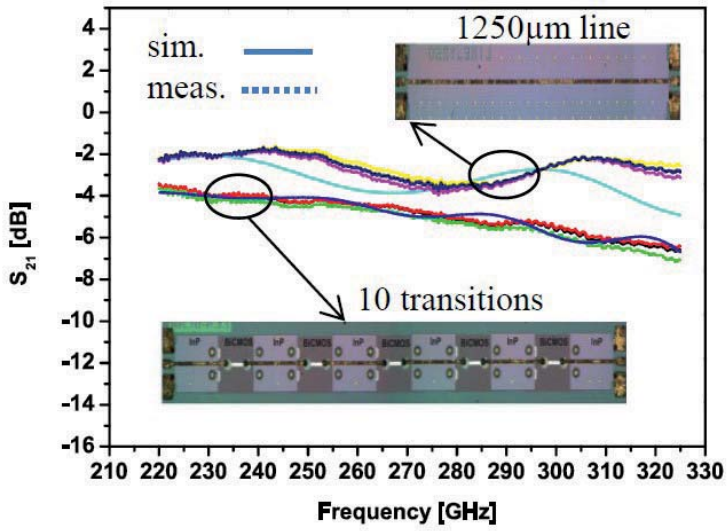


Fig. 6.3. Simulated and measured insertion loss (S_{21}) of the test structure with ten concatenated transitions between the InP microstrip layer (G_2) and the metal layer (TM2) in the BiCMOS process. The vias close to the InP microstrip line ensure that a common ground is shared between the InP and BiCMOS circuit parts. Also shown are simulated and measured insertion loss data of a 1250 µm line length on the InP part.

6.2 Design and Characterization

6.2.1 250 GHz Hetero-Integrated Source

The 250 GHz hetero-integrated source consists of a Voltage Controlled Oscillator (VCO) in 0.25 µm BiCMOS technology and a frequency multiplier in 0.8 µm transferred-substrate (TS) InP-HBT technology. Fig. 6.4 (bottom) shows the block diagram and entire schematic diagram of the hetero-integrated circuit. The VCO circuit can be seen on the left, in the center the BiCMOS-InP transition, and the tripler circuit on the right. The BiCMOS VCO features a differential Colpitts topology and is described in [101]. The VCO is followed by a single-stage buffer in cascode topology. The purpose of the buffer is to isolate the VCO core from the rest of the circuit. Cascode topology offers good isolation and matching. Single-ended output is taken from one port of the differential buffer.

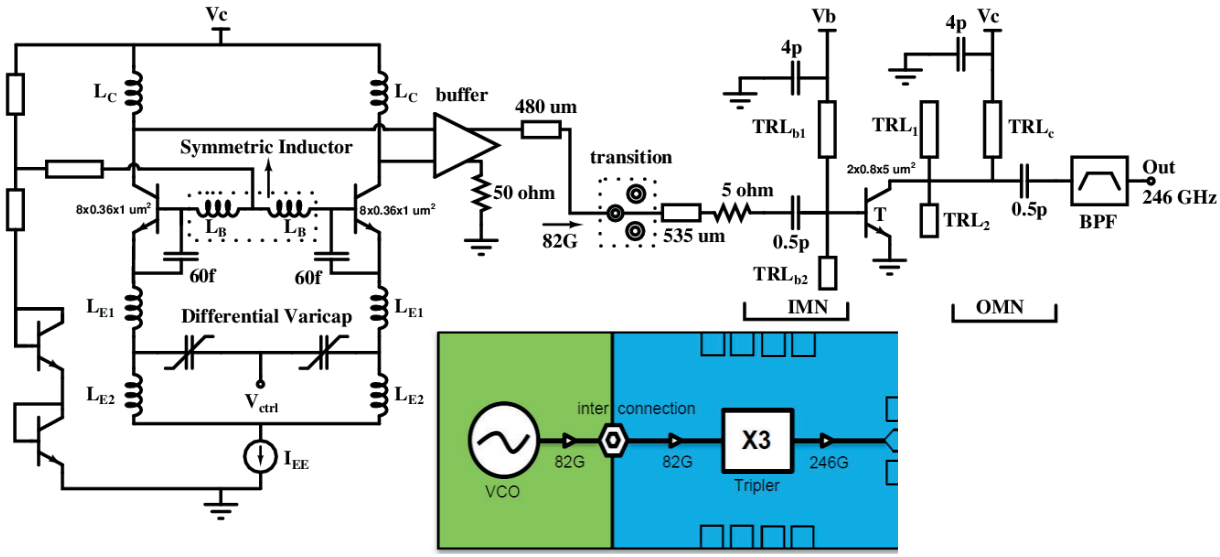


Fig. 6.4. Schematic diagram of the 250 GHz hetero-integrated source with block diagram.

The TS InP-DHBT part consists of a 246 GHz single-transistor tripler. The frequency tripler is based on a common emitter, single-ended topology. It uses a 2-finger HBT with an emitter size of 0.8 × 5 µm² each. The single HBT device is biased under class-A conditions and driven into saturation. In this condition, the HBT amplifier generates an output waveform with higher odd-order harmonics. The unwanted spurious and the fundamental and the second harmonics are suppressed by a high-pass type output matching network, followed by an open-short type band-pass filter. The input of the transistor (T) is matched (IMN) using TRL_{b1} and TRL_{b2} to 50 Ω at the input frequency f_0, while the output matching network (OMN) provides conjugate matching at the third harmonic $3f_0$. Moreover, to reduce the losses at the desired harmonic, λ/4 transmission lines TRL_1 and TRL_2 are used to short-circuit the fundamental f_0 and the second harmonic $2f_0$ of the tripler, respectively [103]. At the input, a 5 ohm resistor is employed to increase the K factor, thus ensuring stability. A DC blocking 0.5 pF capacitor is included at the input and output to facilitate future integration with buffers or mixers.

At the output, a bandpass filter (BPF) is used to suppress all unwanted harmonics at the output of the circuit. The transmission lines and the implemented open-short band pass filter (BPF) were optimized in ADS, assisted by a 2.5D planar EM-simulator (Momentum). The input of the BPF is matched for the third-harmonic impedance and the output of the BPF is matched to 50 Ω.

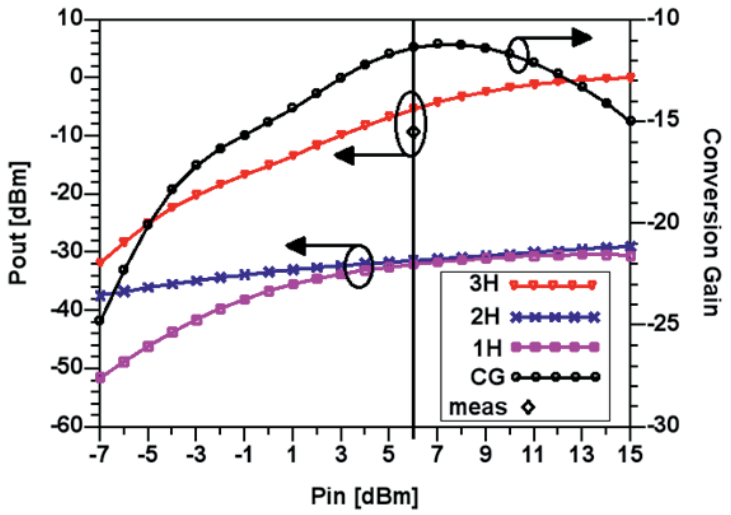


Fig. 6.5. Tripler circuit of Fig. 6.4: Simulated conversion gain (CG) and output power of the first (1H), second harmonic (2H) and the desired third harmonic (3H) as a function of input power for 82 GHz fundamental frequency. Actual input power was measured to be about 6 dBm, as indicated by the vertical bar. Also included is the measured output power at 3rd harmonic (diamond).

In Fig. 6.5, the simulated conversion gain (CG) and output powers of the first (1H), second (2H) and the desired third harmonic (3H) are plotted against input power. One can see that the power level of the fundamental and second harmonic stays -20 dB below the third harmonic according to simulations. Measured output power of the hetero-integrated source is -9 dBm (see Fig. 6.12), which is not far from the expected value from the simulation.

In the circuit realized here, a version of the tripler without the band pass filter (BPF) was implemented. After fine tuning the input and output matching network, the tripler without the band pass (BPF) filter in simulation predicts -3.2 dBm and +2.1 dBm single ended output power, for an input power of 6 dBm and 14 dBm, respectively. The tripler collector bias voltage and base current were set to 1.6 volts 10 mA and 0.27 mA, respectively. According to simulations, the fundamental (f_0) and the second harmonics ($2f_0$) were suppressed by approximately -10 dB and -19 dB compared to the third harmonic ($3f_0$). It is obvious that the filter involves a trade-off between harmonics suppression and insertion loss and thus output power for the wanted harmonic. The latter could be compensated by adding an extra buffer stage at the output of the tripler. Regarding power, one should note also that the circuit involves a 535 µm long interconnect line between the VCO and the tripler (see Fig. 6.4), which could be significantly shortened in a redesign thus improving output power further.

Fig. 6.6 shows the chip photograph of the hetero-integrated circuit. The chip area of the source reaches 3×1 mm². DC biasing of the VCO on BiCMOS as well as the tripler on InP DHBTs is both provided through DC pads on top of the chip, i.e., on the upmost InP metallization layer. RF output has to be taken from the ground–signal–ground (GSG) probe

pads on the right-hand side of Fig. 6.6. A continuous ground plane is located between the TS InP on the right-hand side and the BiCMOS circuit area below. This ensures a low loss thin-film microstrip wiring environment in the TS InP part, which is not affected by the BiCMOS circuitry below. The BiCMOS filler structure is implemented only in the BiCMOS circuit part while the InP circuit part is kept filler-free.

The hetero-integrated source was measured on-wafer using the setup shown in Fig.6.7. Three major steps were performed to characterize the hetero-integrated source. In a first setup, the output spectrum of the complete hetero-integrated circuit was investigated. The goal here was to identify and measure the output frequency and to guarantee that the spectrum is clean, i.e., the amplitudes of the spurious lines are small enough, which is important for the accuracy of the power measurement. To estimate suppression of unwanted harmonics over the full frequency range, different frequency bands of the output spectrum were measured applying the suitable waveguide probes and sub-harmonic mixers with the same setup.

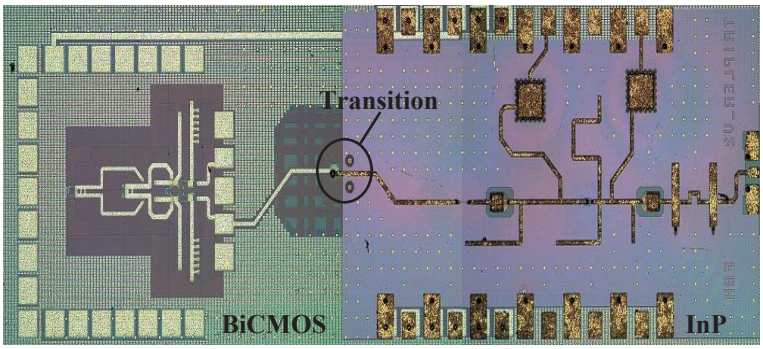


Fig. 6.6. Chip photograph of the 250 GHz hetero-integrated circuit.

In a second setup, the output power of the circuit was determined with a waveguide probe and a waveguide system connected to the input of an Erickson PM4 power meter. Since, the power meter is not frequency-selective any spurious line will degrade measurement accuracy of the component at the wanted output frequency. In a third setup, the output reflection coefficient of the circuit was measured with a waveguide probe and an R&S ZVA-Z325 frequency extender connected to the input of a vector network analyzer.

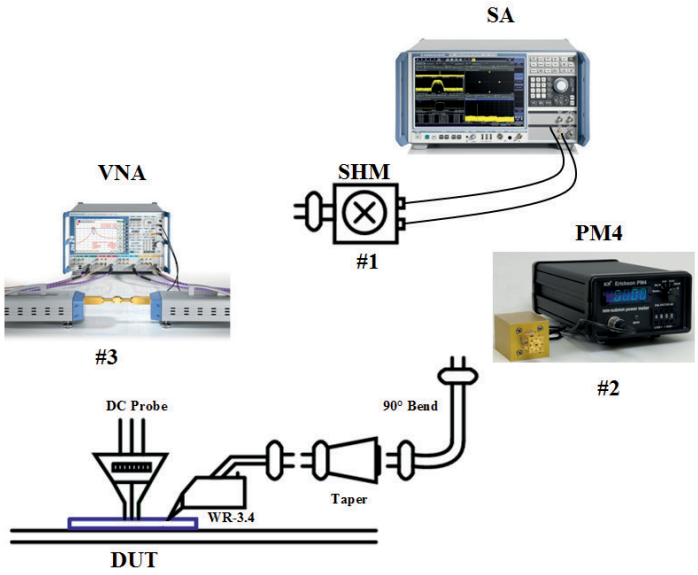


Fig. 6.7. Measurement setup for characterization of the signal source (meas. setup #1 for output spectrum, meas. setup #2 for power measurement, meas. setup #3 for S parameters).

In order to determine the behavior of the BiCMOS VCO itself and the possible changes due to wafer bonding and the additional layers on top of the CMOS stack, a version without tripler was fabricated where the InP circuit part consists of a simple thru-line (see Fig. 6.8). This allows on-wafer probing. In this case, the frequency of oscillation was measured using an FSUP signal source analyzer. In order to ensure linear operation of the SHM, a variable attenuator was placed right after the RF probe, with attenuation fixed to 20 dB during measurement of the VCO spectrum.

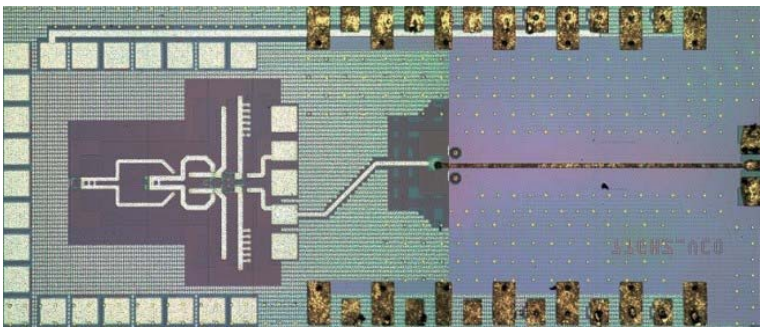


Fig. 6.8. Chip photograph of the 82 GHz VCO without InP tripler (the InP part consists of a simple through-line).

The output power of the circuit was measured with a 90° bend and WR10 taper connected to the input of an Erickson PM4 power meter. Fig. 6.9 shows the VCO output spectrum. The VCO was fed by 5 volts DC supply and the current consumption was 134mA.

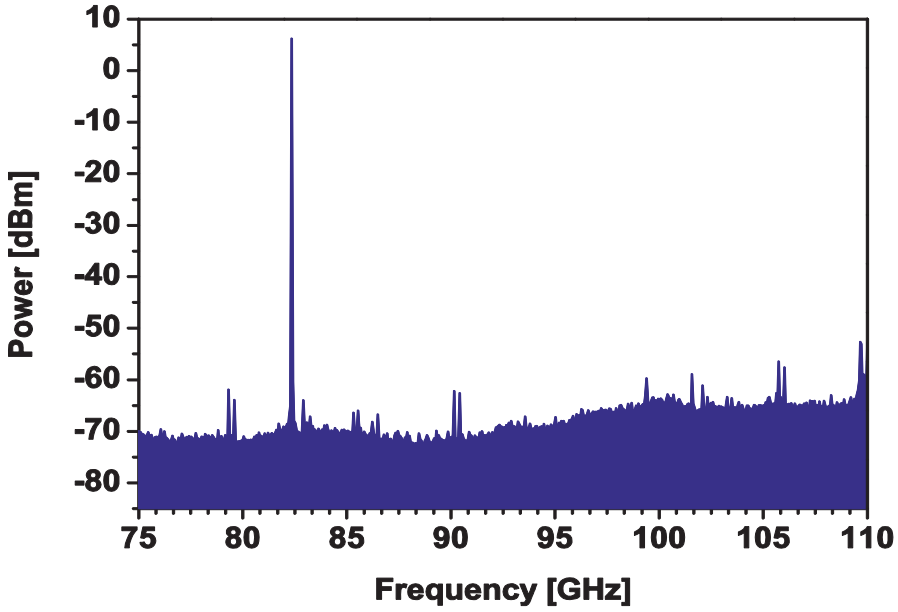


Fig. 6.9. Measured output frequency spectrum of the VCO version without tripler according to Fig. 6.9. (tuning voltage: 0 volt losses of cable, prober, 20 dB attenuator and of the 1mm long microstrip line on the chip deembedded).

The measured output power of the VCO was approximately 5 dBm, with around 1 GHz of tuning range and a corresponding output power variation of less than 0.3 dB. Correcting the output power by the loss of the 1mm long microstrip line at the output (see Fig. 6.8), one achieves approximately 6 dBm of actual input power delivered to the tripler in the final circuit (see following subsection). Fig.6.10 shows the output power and frequency of oscillation as a function of the tuning voltage. Note that the data in Fig.6.9 takes into account all the losses, the output power measured on spectrum analyzer is in good agreement with the measured actual output power shown in Fig. 6.10.

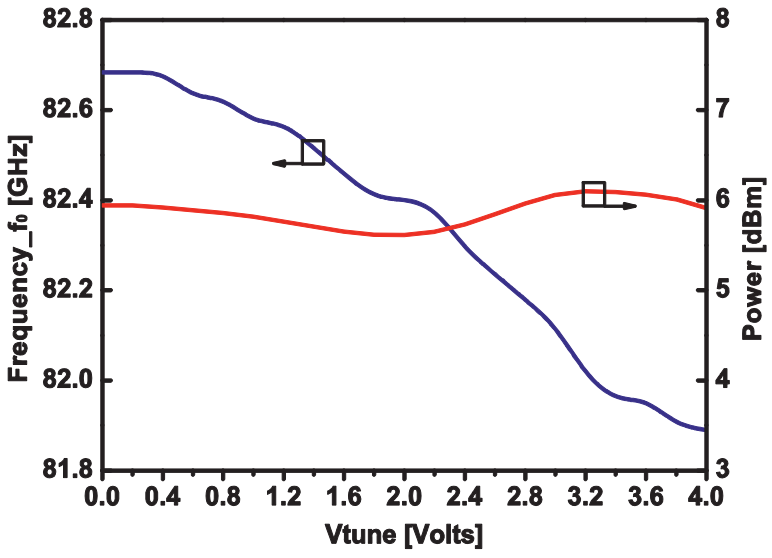


Fig. 6.10. Measured output power and frequency of the VCO (see Fig.8) as a function of tuning voltage (waveguide system and prober loss deembedded).

A Cascade ground-signal-ground (i325-S-GSG-50-BT) WR3.4 waveguide probe was used to probe the output signal of the source in the band from 220 to 325 GHz. The insertion loss of the output probe is 4.5 dB as given by the vendor; waveguide bend and taper are estimated to contribute 3 dB insertion losses in the 245 GHz band. All measurement data presented in the following are corrected by the resulting attenuation of 7.5 dB. The output spectrum was detected by means of a sub-harmonic spectrum analyzer mixer WR3.4, which has a conversion loss of approximately 35 dB at 245 GHz, and an FSUP signal source analyzer. Fig. 6.11 presents the measured output spectrum.

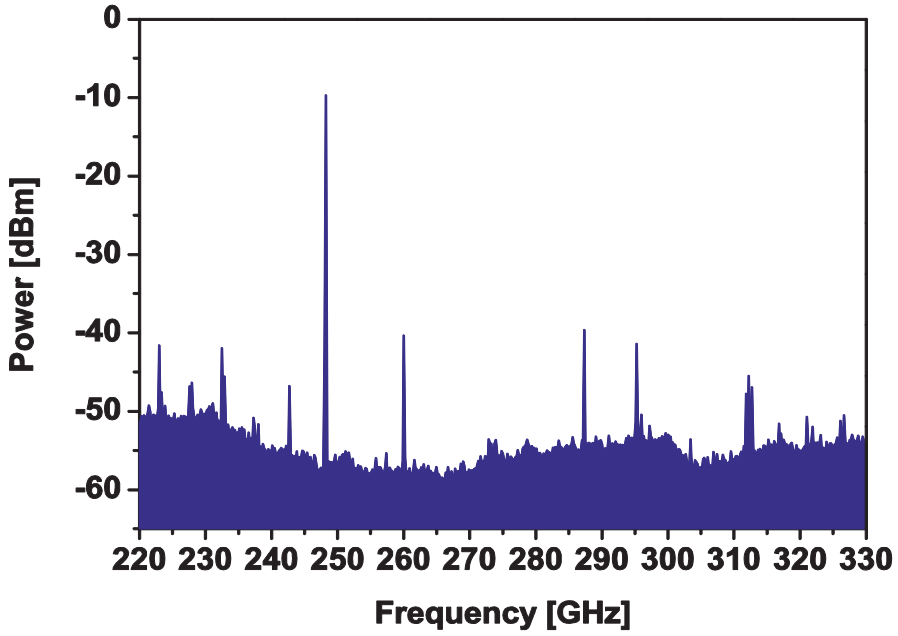


Fig. 6.11. Measured output frequency spectrum of the hetero-integrated source (tuning voltage: 0 volts, cable and prober loss deembedded).

In a next step, the output power of the circuit was determined with a 90° bend and a WR3.4-WR10 taper connected to the input of an Erickson PM4 power meter. Taking in to account the waveguide system and probe loss, one obtains an actual output power of -9 dBm at the circuit output, at a frequency of 248 GHz. In Fig. 6.12, the output frequency of the hetero-integrated source and the output power are plotted as a function of the tuning voltage. A tuning range around 3 GHz is achieved. One should note that the deembedded power data for the spectrum and the power meter measurements in Figs. 6.11 and 6.12 agree well, although measurements set-ups differ (see Fig. 6.7, setup #1 and #2). This proves repeatability of our measurements and supports validity of the deembedding approach. The frequency tuning characteristics plotted in Fig. 6.10 and the corresponding fundamental Fig. 6.12 differ slightly by 200 MHz because they refer to different circuits on the wafer. The standard

deviation of the BiCMOS VCO frequency across the 3" hetero-integrated wafer is 0.08 % [104], i.e., 66 MHz.

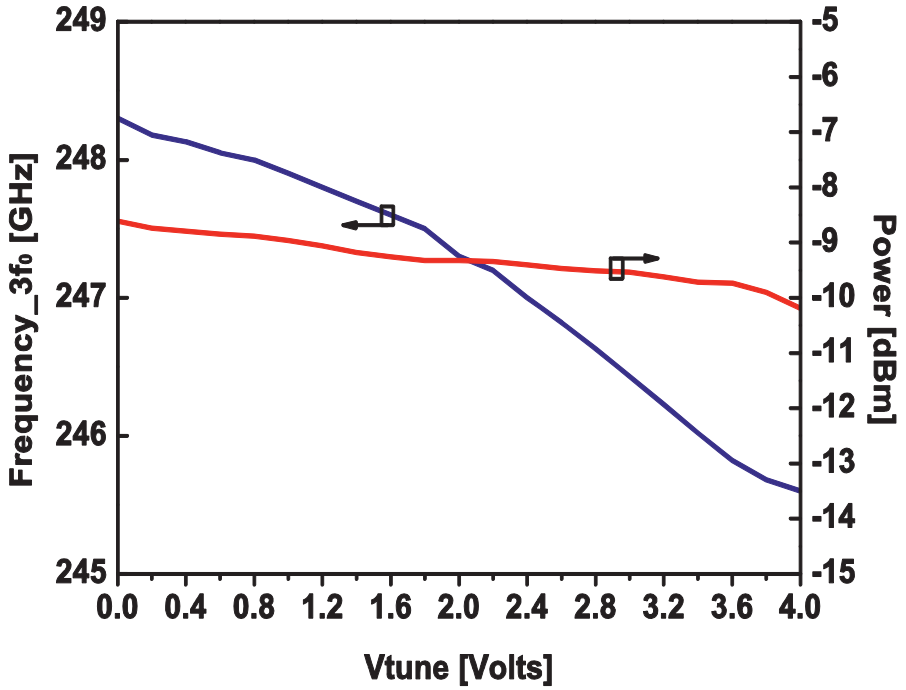


Fig. 6.12. Measured output frequency and power of the hetero-integrated source as a function of the tuning voltage (waveguide and prober loss deembedded).

The band pass-filter at the output introduces approximately 4 dB losses (estimated by EM simulation), therefore, the tripler circuit alone is expected to deliver about -5 dBm. On the other hand, the band pass filter improves suppression of fundamental (f_0) and second ($2f_0$) harmonics by more than 25 dB (estimated by EM simulation), which is advantageous from the system point of view.

In order to obtain comprehensive results on spectral purity and unwanted harmonics suppression, three different bands (W, G, and J) have to be measured. This was performed by using a WR-10 waveguide system (probe and SHM), a WR-5 waveguide system (probe and SHM) and a WR-3.4 waveguide system (probe and SHM) separately. Fig. 6.13 provides the measured output spectrum at W-band, G-band, and J-band. Due to the presence of spurious signals caused by the mixers etc. interpretation of the data is not always straightforward. In J-band and W-band, however, all unwanted or spurious signals are much weaker than the 3rd and 1st harmonics, respectively. Thus, measuring the total power in these bands with the power meter should give reliable values for the harmonic lines.

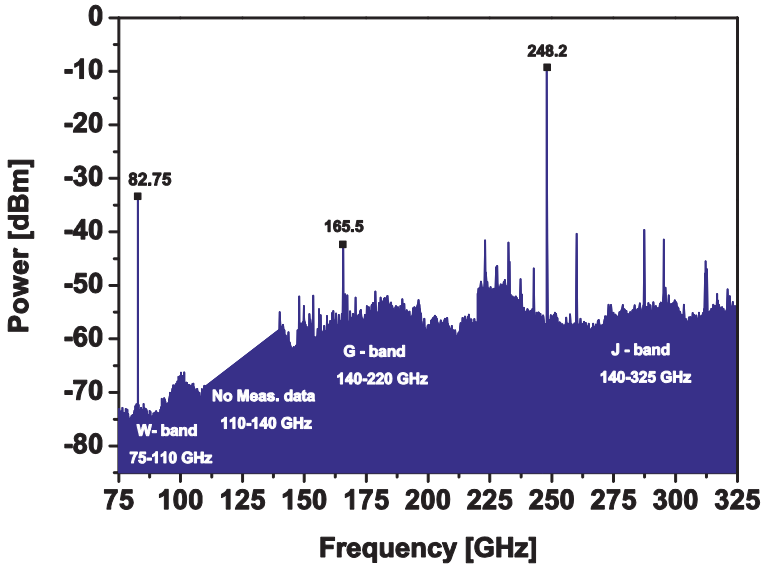


Fig. 6.13. Measured W-band, G-band and J-band output frequency spectrum of the hetero integrated source (tuning voltage: 0 volt, cable and prober losses deembedded; no measured data in the frequency range between 110GHz and 140 GHz).

One can easily observe that the fundamental (f_0), second harmonic ($2f_0$) and unwanted signals all are below -30 dB with respect to the desired third harmonic ($3f_0$) signal. Note that in Fig. 6.14 the back ground noise of the spectrum increases in the higher frequency bands. This is due to the noise contribution from the sub-harmonic mixer used for the G and J bands. The measured phase-noise characteristics are presented in Fig. 6.14. Values of -85 and -106 dBc/Hz at offsets of 1 MHz and 10 MHz are obtained, respectively. These are excellent results for this frequency range and a free-running VCO.

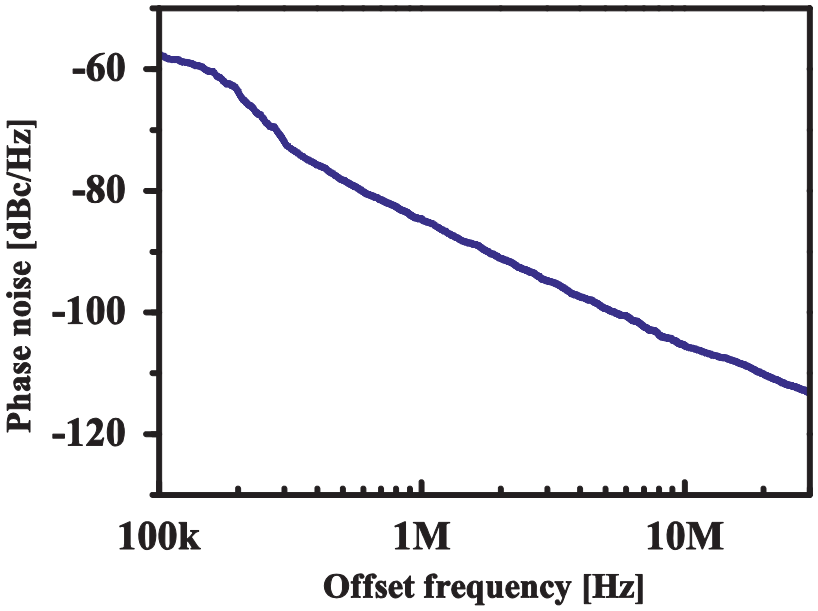


Fig. 6.14. Measured phase noise performance of the hetero integrated source.

The output return loss of the hetero-integrated circuit was measured using a vector network analyzer. The system was calibrated with thru-reflection-match (TRM) to place the reference plan at the probe tips. Note that in this measurement the bias supply of the BiCMOS VCO was switched off so that the InP tripler was operating as a non-autonomous circuit. Fig. 6.15 shows the measured output return losses of three samples. The curves indicate broad-band behavior with more than 12 dB return loss over at least 20 GHz. This is a promising result at this frequency range. It also shows that all unwanted harmonics (f_0, $2f_0$) and spurious signals are well suppressed by the integrated band pass filter at the output.

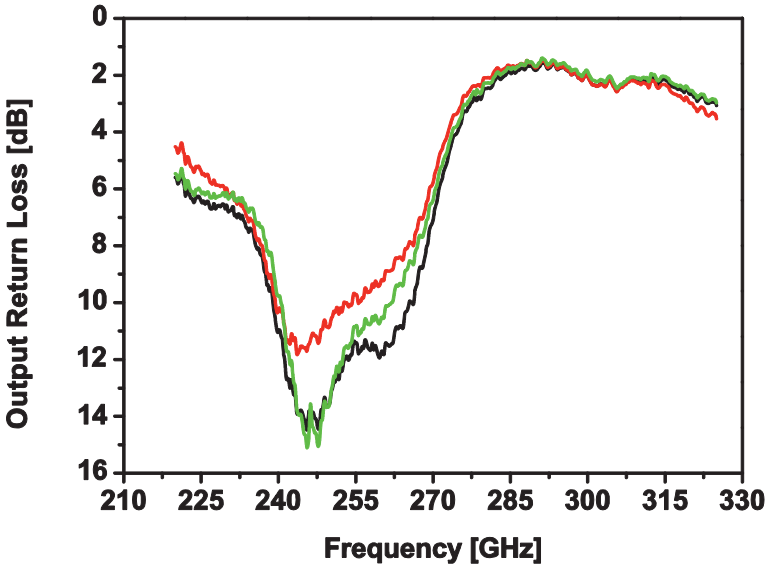


Fig. 6.15. Measured output return losses of the hetero integrated source (3 samples).

As mentioned before the circuit suffered from a relatively low output power of -9 dBm. (see Table 6.1 [106]). In order to achieve higher tuning range and output power, the new tripler has been optimized by redesigning the input and output matching networks and the output band pass filter. Also, the layout was realized in a more compact way reducing interconnection loss between the VCO and the tripler subcircuits. After redesigning, the circuit significant performance improvements have been achieved such as a 5-fold higher tuning range and more than 7 dB increase in output power. The measured output power of the redesigned hetero-integrated source reached -1.6 dBm (0.7 mW) output power at 250 GHz with around 5 GHz tuning range. In Fig. 6.16, the output frequency of the new version hetero-integrated source and the output power are plotted as a function of the tuning voltage.

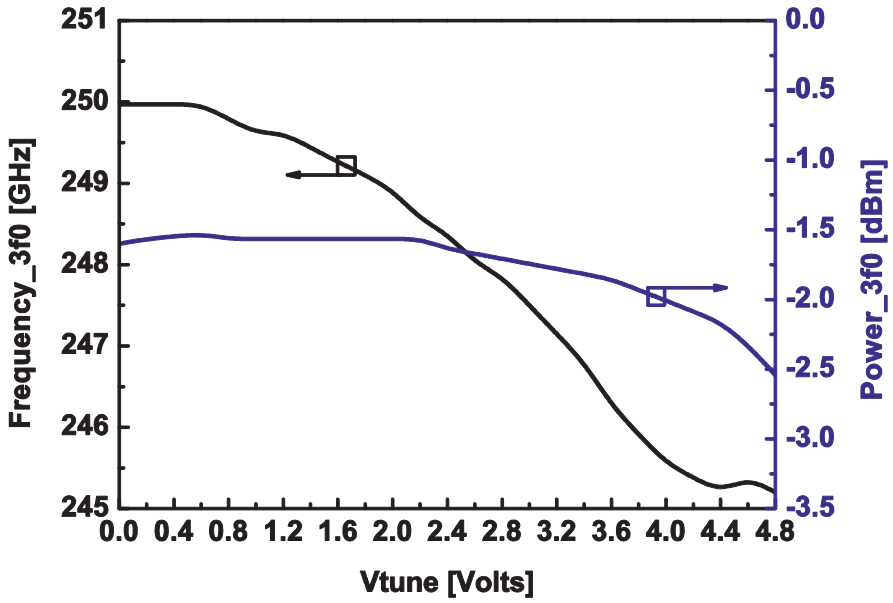


Fig. 6.16. Measured output frequency and power of the redesigned hetero-integrated source as a function of the tuning voltage (waveguide and prober loss deembedded).

Table 6.1 benchmarks the performance of the hetero-integrated source against other published mm-waves sources beyond 200 GHz in different technologies. As can be seen, the hetero-integrated source belongs to the ones with the highest output powers among the published results. A few sources [47], [102], [108] exhibit higher output power, but those are in lower frequency bands. The circuit according to [109] delivers higher output power at 250 GHz, but in this case 2 PA stages were used to increase input power level of the doubler. To the best knowledge, this was the first hetero-integrated signal source beyond 200 GHz frequency reported so far. It has been published in [105].

Table 6.1
State-of-the-art comparison of mm-wave sources on different technologies

Reference	Technology	ft/fmax [GHz]	Source Topology	Frequency [GHz]	Pdc [W]	Pout [dBm]*
This work	**BiCMOS+TS InP HBT (250nm + 800nm)**	**>350/350 180/200**	**VCO + Tripler (Hetero-integrated)**	**245-250**	**~ 0.700 (0.68+ 0.013)**	**-1.6**
[106]	BiCMOS+ TS InP HBT (250nm + 800nm)	360/345 180/200	VCO + Tripler (Hetero-integrated)	246-247	0.700	-9
[110]	50nm InGaAs mHEMT	380/500	Tripler + Buffer	285-315	0.064	-1.9
[111]	250nm InP DHBT	375/>650	Fundamental VCO	287	~0.115	-3.9
[112]	130nm BiCMOS HBT	250/380	3 stage PA + Doubler	215-240	0.430	-3
[113]	250nm InP DHBT	350/600	VCO + Quadrupler	212-228	-	-4
[114]	65nm CMOS	-/175	3rd Harmonic Generation VCO	285	0.070	-19
[47]	800nm TS InP HBT	370/370	Fundamental Oscillator	200	0.022	0
[102]	35nm InGaAs mHEMT	515/-	Balanced Doubler	128-220	0.013	+1.8**
[108]	90nm SiGe	300/310	Balanced Doubler	224-228	0.035	+2
[109]	130nm BiCMOS HBT	300/500	VCO + 2 stage PA + Doubler	245	0.290	+1.4

*peak output power, **power at 154 GHz

6.2.2 330 GHz Hetero-Integrated Source

The 330 GHz hetero-integrated signal source is based on a fundamental BiCMOS voltage controlled oscillator (VCO) followed by InP frequency multiplier. The detail of the BiCMOS VCO has already been discussed in section 6.3.1. Fig.6.17 presents the entire block diagram of the hetero-integrated signal source.

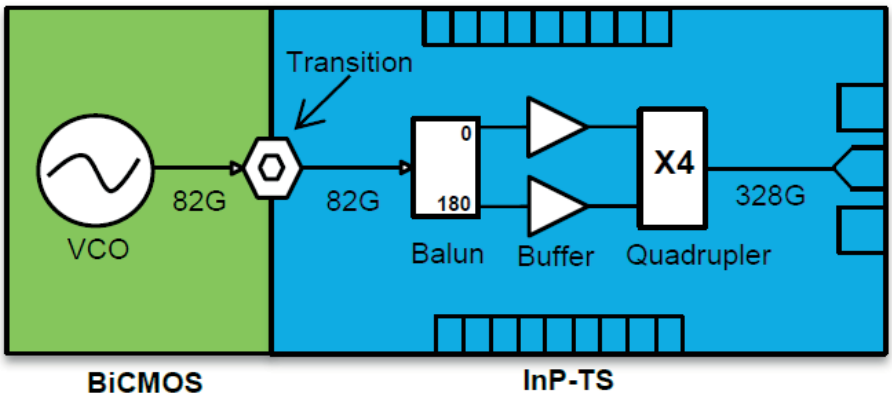


Fig. 6.17. Block diagram of the 330 GHz hetero-integrated source.

The TS InP-DHBT part contains a Marchand balun, buffers, and a frequency multiplier. Fig. 6.18 presents the simplified schematic diagram of the quadrupler. First, a 82 GHz Marchand balun was designed, which converts the un-balanced output signal from the BiCMOS VCO to a balanced signal. Then two parallel single-ended 82 GHz buffers T_1 and T_2 are realized based on common emitter (emitter area 0.8 × 5 μm²) topology, followed by a balanced quadrupler T_3 and T_4 having equal emitter size same as T_1 and T_2. In order to maintain appropriate operation of the quadrupler and the buffer stages, separate dc biasing was implemented by using V_b and V_c supply voltages. DC blocking capacitors C_{balun} are used to facilitate dc bias voltage V_{b1}, without affecting by the ground plane of the balun (see Fig. 6.18). At the output, the odd-order harmonics are suppressed by shunting the collectors. The unwanted 2nd harmonic is short-circuited by a λ/4 thin-film MS-line. The thin-film microstrip line layout including the Marchand balun was optimized using a 2.5 D EM simulator.

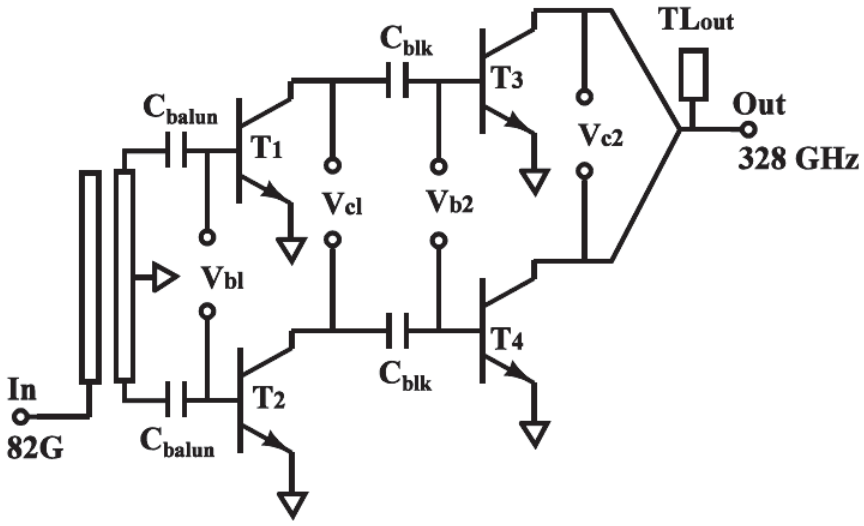


Fig.6.18. Simplified circuit diagram of the InP quadrupler with balun and input buffer.

Fig. 6.19 shows the chip photograph of the entire hetero-integrated circuit. The VCO circuit can be seen on the left, in the center the low-loss BiCMOS-InP transition (see Sec. 6.1), and the quadrupler circuit on the right. The chip area of the hetero-integrated circuit is 2.5×1 mm². DC biasing of the VCO in BiCMOS as well as the quadrupler in InP DHBT technology is provided through DC pads on top of the chip. RF output has to be taken from the ground–signal–ground (GSG) probe pads on the right-hand side of Fig. 6.19. A continuous ground plane is located between the InP circuitry on the right-hand side and the

BiCMOS circuit area below. This ensures a low loss thin-film microstrip wiring environment in the InP part, which is not affected by the BiCMOS structures below.

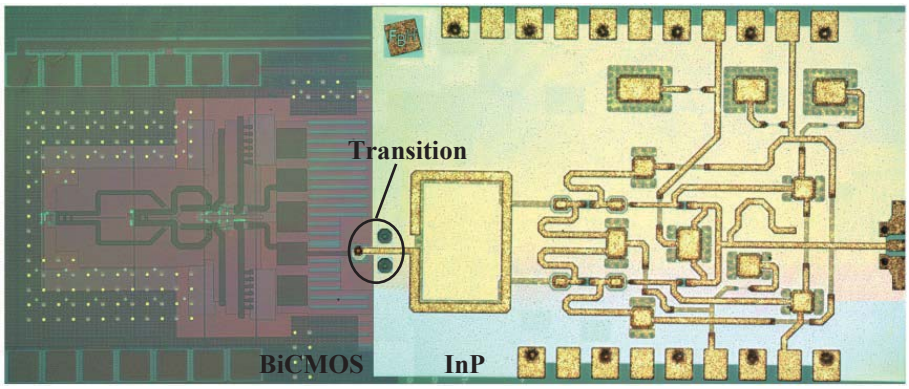


Fig. 6.19. Chip photograph of the 330 GHz hetero-integrated circuit.

The hetero-integrated source was characterized on-wafer using the setup shown in Fig.6.7. The output spectrum was measured by a ground-signal-ground (i325-S-GSG-50-BT) WR3.4 waveguide probes, a sub-harmonic mixer, and a FSV3Q spectrum analyzer (see Fig.6.7 meas. setup # 1). Fig. 6.20 presents the measured output spectrum. One can easily observe that the third harmonic of the VCO fundamental ($3f_0$) is below -30dBc. The output power of the circuit was determined through a WR3.4 taper, a 90° bend and a WR3.4-WR10 taper connected to the input of an Erickson PM4 power meter (see Fig.6.7 meas. setup#2). The insertion loss of the output probe is 6.5 dB at 325 GHz as given by the vendor, waveguide bend and tapers are estimated to contribute 3 dB insertion loss in the 327 GHz band. All measurement data presented in the following are corrected by the resulting attenuation of 9.5 dB. Taking into account the waveguide system and probe loss, one obtains an actual output power of -12 dBm at the circuit output, at a frequency of 327.2 GHz. One should note that the deembedded power data for the spectrum and the power meter measurements agree well, which confirms measurement repeatability.

It is important to mention that the used WR3.4 waveguide probe is specified for a frequency range from 220 to 325 GHz, while the quadrupler circuit operates around 327 GHz. This introduces additional losses to those specified by the vendor and thus actual power may be higher than the value given above. The frequency limitations of the probe also were the reason why tuning characteristics of the source could not be measured to their full extent. Nevertheless, during measurement it was observed that one could achieve more than 1.53 % tuning range, limited by the VCO.

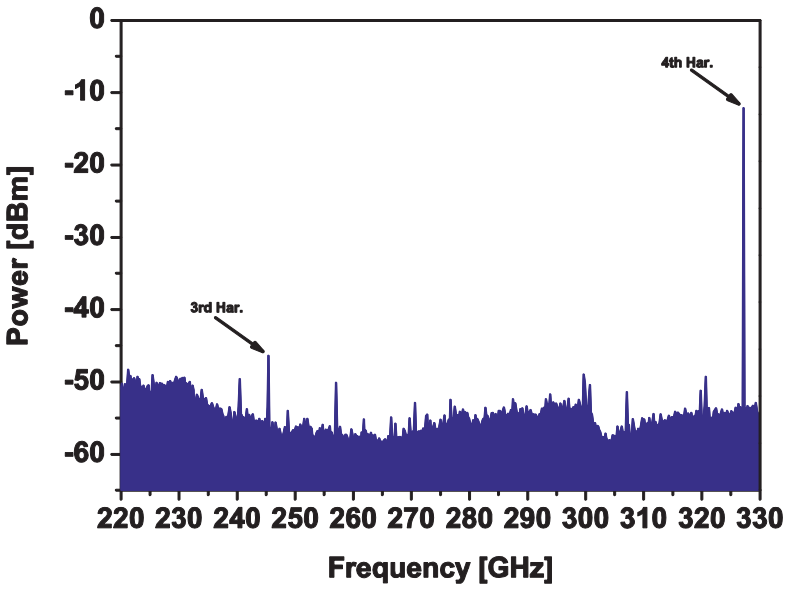


Fig. 6.20. Measured output power spectrum of the hetero-integrated source. (BiCMOS VCO oscillation frequency: 81.8 GHz at 4.8 volts tuning voltage, prober loss is deembedded).

Table 6.2 benchmarks the performance with other recently published THz sources around 330 GHz in different technologies [114]–[117]. As can be seen, our signal source represents the first hetero-integrated source in this frequency range. The output power is at the lower end of the data but this is not surprising since the present circuit is based on a more relaxed geometry (250nm-BiCMOS and 800nm-InP). To the best knowledge, this was the first THz hetero-integrated signal source reported so far. It has been published in [121].

Table 6.2
Comparison THz sources around 330 GHz on different technologies

Ref./ [Year]	[114]/ 2013	[115]/ 2012	[116]/ 2012	[111]/ 2011	[117]/ 2008	**This work**
Technology	120nm SiGe HBT	35nm mHEMT	65nm CMOS	130nm SiGe HBT	35nm InP HEMT	**800nm/250nm Heterointegrated InP-on-BiCMOS HBT**
ft/fmax [GHz]	300/400	515/-	-/~200	250/380	-/600	**320/320 180/200**
Circuit Topology	PP VCO	Tripler	4 coupled VCO	Multiplier chain	Oscillator	**VCO+ Quadrupler**
Frequency [GHz]	320	324	320	325	330	**328**
Pdc [W]	0.063	0.65	0.34	0.43	0.016	**0.045 (InP) 0.700 (BiCMOS)**
Pout [dBm]	-13.3	-8.8*	-3.3	-3	-5.7	**-12****

*average power, ** probe loss data calculated at 325 GHz

7 Conclusions

This thesis presents mm-wave MMIC fundamental and harmonic signal sources using 0.8 µm Transferred Substrate InP DHBT technology as well as wafer-level integration of InP-on-BiCMOS (250nm-BiCMOS and 800nm-InP) technology. The frequency range around 100 GHz and beyond offers large bandwidth and short wavelengths, which enable high-speed communications as well as improved performance of sensors and imaging systems. All of these systems require an efficient signal source, which includes particularly a combination of high output power, low phase noise and high DC-to-RF efficiency. The main contributions of this research are summarized below.

The first part covers highly efficient fundamental and harmonics oscillators, from 96 GHz to 290 GHz, based on the FBH 0.8 µm TS InP-DHBT MMIC process. The 96 GHz oscillator delivers 8.7 dBm output power, the 197 GHz oscillator delivers 0 dBm output power at 24.7% and 4.6% overall DC-to-RF efficiency, respectively. A 290 GHz harmonic oscillator reaches -8.5 dBm output power at 0.5% overall DC-to-RF efficiency. These are the highest reported efficiencies for fundamental and harmonic oscillators, at the time of publication [47, 56].

Beyond this, 162 GHz and 270 GHz reflection-type push-push oscillators with low power consumption were demonstrated, based on an InP HBT MMIC process on BiCMOS technology. The circuits achieve -4.5 dBm output power with 1.5% overall DC-to-RF efficiency and -9.5 dBm output power with 0.4% overall DC-to-RF efficiency [65], respectively.

As a key element in the realization of more complex source and multiplier circuits, several passive components with remarkable performance were developed. This comprises a compact 0.06 mm² broadband Marchand balun and a wideband tiny 0.04 mm² band pass filter. The balun exhibits an insertion loss of less than 5 dB and return losses of more than 10 dB within a wide frequency range from 70 to 110 GHz. The band pass filter exhibits an insertion loss less than 2 dB and a return loss of more than 10 dB at 225 GHz center frequency and achieves 40 GHz 3 dB bandwidth.

A second major contribution of this work is broadband active frequency multipliers. A full G-band (140-220 GHz) high output power frequency doubler, based on the balanced topology is presented. It delivers 5 dBm ± 3 dB output power across the full band. The doubler circuit exhibits a power efficiency of 16% in this frequency range. High order active frequency multipliers, i.e., tripler and quadrupler have been shown as well. The tripler (x3)

circuit delivers -4.4 dBm output power at 247 GHz with 3% DC-to-RF efficiency and 50 GHz bandwidth. The quadrupler (x4) circuit performs well within 90 GHz of bandwidth and delivers -7 dBm output power at 325 GHz with 0.5% DC-to-RF efficiency [124].

There are Schottky diode based multipliers which achieve higher output power [e.g. 117, 118]. However, the advantage of MMIC approach is that the circuit can be integrated on the same chip with the other components such as PA, VCO and mixer and thus lends itself to system integration. System integration is crucial at these frequencies, because any transition off chip leads to losses in excess of 1 dB, which limits the system performance. An additional important aspect is the good return loss of MMIC solutions. Finally, it has been considered to apply on-chip power combining and cascode operation to increase the output power by at least 3 dB and conversion gain by 5 dB. This is not possible for Schottky diodes and difficult with BiCMOS or CMOS technologies due to limited breakdown voltage capabilities. Overall, the results on the InP oscillators and multipliers show the capabilities of the 0.8 μm InP DHBT transferred-substrate process to realize efficient signal generation, with a geometry node which is quite relaxed compared to the corresponding III-V and Si-based processes.

The third important contribution of this work is that it has demonstrated the potential of sources towards THz frequencies with heterogeneous InP-on-BiCMOS integration the first time. A 250 GHz voltage controlled hetero-integrated source using InP-on-BiCMOS technology has been developed, which consists of an 84 GHz Voltage Controlled Oscillator (VCO) in 0.25 μm BiCMOS technology and a 250 GHz frequency tripler in 0.8 μm transferred-substrate InP-HBT technology. The source delivers 0.7 mW (-1.6 dBm) output power with a 2% tuning range. Excellent phase noise behavior with values at -85 and -106 dBc/Hz at offsets of 1 MHz and 10 MHz, respectively are reached. The InP tripler sub-circuit consumes only 13 mW DC power and exhibits a conversion loss of approximately 5 dB. At even higher frequencies, a 330 GHz hetero-integrated source using the heterogeneous process has been realized. It uses a fundamental BiCMOS Voltage Controlled Oscillator (VCO) and a frequency quadrupler including Marchand balun and input buffer in TS InP-HBT technology. The source delivers -12 dBm output powers with -30dBc third harmonic ($3f_0$) of the fundamental VCO. These were the first hetero-integrated signal source in sub-THz and THz frequency range reported, at the time of publications [105, 106, 107, 121]. These results demonstrate that hetero-integrated technology employed here (250nm-BiCMOS and 800nm-InP), despite its relaxed geometry, outperforms the high-end Si-based processes in terms of output power and efficiency in the sub-mm-wave range. On the other hand, it offers the full

Si-typical complexity at lower frequencies, thus offering a distinct advantage over the pure InP processes.

Summarizing the results obtained in the course of this work, Fig. 7.1 depicts the output power of the realized signal sources as a function of frequency. It reveals the well-known trend for output power characteristics against frequency. While the values achieved and the numbers of circuits realized are an excellent first step in demonstrating the potential of the new hetero integration process, the output power level obtained can certainly be increased, either by using larger transistor in the circuit design or additional output buffers of the oscillators and input/output buffer stages in the multiplier circuits. This should be explored as the next step.

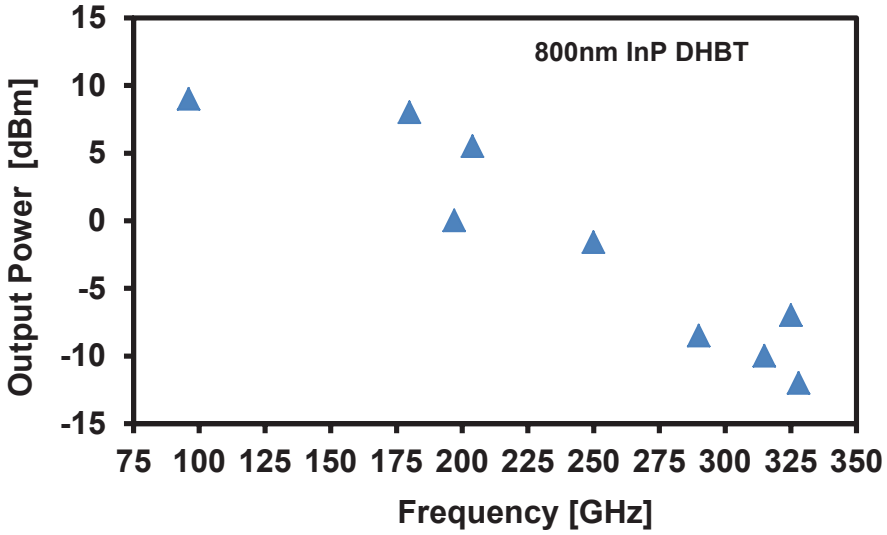


Fig. 7.1. Realized output power of the signal sources as a function of frequency.

Packaging is one of the further important directions of this research work. In order to achieve complete systems, the mm-wave and THz components such as PA, oscillator, multiplier and mixer, need to be integrated into package. This can be implemented in a future step. The advantage with this technology is that a maximum number of circuits can be integrated on the same chip thus reducing mm-wave interconnects to a minimum.

There are some other future aspects of this work. The sources presented in this work are fixed frequency source; but can be turned into a VCO in a simple way employing a varactor.

Regarding hetero-integration, the available on-chip BiCMOS module can easily be complemented by a PLL and other digital functions necessary to realize a frequency source as required in practical system applications. This will be a further issue for a future design.

Appendix

A. Abbreviations

AlN	Aluminium Nitride
Au	Gold
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BCB	Benzocyclobutene
BPF	Band Pass Filter
CB	Common Base
CMOS	Silicon Complementary Metal Oxide Semiconductor
CG	Conversion Gain
DHBT	Double Hetero Bipolar Transistor
DUT	Device Under Test
DC	Direct Current
dB	Decibel
dBm	Decibel Miliwatt
dBc	Decibels Relative to the
EM	Electromagnetic
E-field	Electromagnetic Field
FOM	Figure Of Merits
GSG	Ground Signal Ground
G	Conductance
G2	Top InP Metal Layer
GD	InP Ground Metal Layer
GND	Ground
GSG	Ground-Signal-Ground
GHz	Gigahertz
HEMT	High Electron Mobility Transistor

HFSS	High Frequency Structural Simulator
InP	Indium Phosphide
InP-on-BiCMOS	Heterogeneous
IF	Intermediate Frequency
IL	Insertion Loss
IMN	Input Matching Network
K-factor	Stability Factor
LO	Local Oscillator
MIM	Metal Insulate Metal
mm-wave	Millimeter Wave
MMIC	Monolithic Microwave Integrated Circuit
mTRL	multiline Thru-Reflect-Line
meas	Measurement
MS	Microstrip
N-well	N-type Well
PLL	Phase Locked Loop
PM4	Power Meter 4
PA	Power Amplifier
Pout	Output Power
Pdc	DC Power Consumption
OMN	Output Matching Network
Q-factor	Quality factor
T	Period of the signal
R	Resistance
RF	Radio Frequency
RL	Return Loss
RPG	Radiometer Physics Gmbh

R&S	Rohde & Schwarz
SiGe	Silicon Germanium
SiNx	Silicon Nitride
S-parameters	Scattering Parameters
SHM	Sub Harmonic Mixer
STMIC	Sub-THz Monolithic Microwave Integrated Circuit
STB	Radial stub
SA	Spectrum analyzer
Sim	Simulation
TL	Transmission Line
T	Transistor
TM2	Top BiCMOS Metal Layer
TS	Transferred Substrate
THz	Terahertz
TRM	Thru-Reflection-Match
VG	Virtual Ground
VNA	Vector Network Analyzer
VCO	Voltage Control Oscillator
WR-##	Waveguide Rectangular Number

B. Symbols

α	Attenuation Constant
β	Phase Constant
θ_t	Conduction Angle
t_0	Conduction Time
e	Wave Propagation
f_{MAX}	Maximum Oscillation Frequency
f_T	Unity Current Gain
f_0	Fundamental Frequency
$2f_0$	Second Harmonic Frequency
$4f_0$	Fourth Harmonic Frequency
γ	Complex Propagation Constant
I_c	Collector Current
I_{cq}	Quiescent Current
I_{max}	Maximum Current
I_n	n^{th} harmonic Current
$\lambda/4$	Quarter Wavelength
I_{max}	Peak Collector Current
r_P	Passive Real Part
r_E	Emitter Real Part
ω_0	Angular Frequency
x3	Multiplication Factor Three
x4	Multiplication Factor Four
Z_0	Characteristic Impedance
Z_E	Emitter Impedance
Z_B	Base Impedance
Z_C	Collector Impedance
S_{21}	Forward Voltage Gain

S_V	Open Loop Gain
V_b	Base DC Bias Voltage
V_c	Collector DC Bias Voltage
V_{ce}	Collector Emitter Voltage
C_{balun}	Balun Blocking Capacitor
mW	Miliwatt
µm	Micrometer
1H	1^{st} Harmonic
2H	2^{nd} Harmonic
3H	3^{rd} Harmonic

C. Figures

D. Tables

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Curriculum Vitae

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2012 – 7/2016	Technical University Berlin, Germany. Doctor of Engineering.
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3/2008 - 2/2011	Researcher at 'IHP-microelectronics GmbH', Frankfurt (Oder), Germany. The work responsibilities were to design and investigate RF analog circuits using 250nm BiCMOS technology.
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