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Innovationen mit Mikrowellen & Licht

Development of Sub-mm Wave Flip-Chip Interconnect

Sirinpa Monayakul

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Innovations with Microwaves and Light

**Research Reports from the Ferdinand-Braun-Institut,
Leibniz-Institut für Höchstfrequenztechnik**

Preface of the Editors

Research-based ideas, developments, and concepts are the basis of scientific progress and competitiveness, expanding human knowledge and being expressed technologically as inventions. The resulting innovative products and services eventually find their way into public life.

Accordingly, the *"Research Reports from the Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik"* series compile the institute's latest research and developments. We would like to make our results broadly accessible and to stimulate further discussions, not least to enable as many of our developments as possible to enhance everyday life.

With the emerging availability of electronic solid-state circuits operating in the sub-mm-wave to THz region (above 300 GHz), the need for manufacturable cost-effective packaging solutions in this frequency range arises. Traditional packaging concepts rely on precision-machined hollow waveguide housings of individual high-frequency semi-conductor chips, which are then interconnected via bulky metal flanges. This report details the development of flip-chip assembly techniques suitable for frequencies up to 500 GHz, representing the highest reported flip-chip connection bandwidth at the time of this writing. Assemblies of several semiconductor chips performing individual functions can be realized by flip-chip mounting on the here presented low-loss carrier substrates, greatly reducing the size, weight, and cost of typical sub-THz RF frontend sub-systems.

We wish you an informative and inspiring reading

Prof. Dr. Günther Tränkle
Director

Prof. Dr.-Ing. Wolfgang Heinrich
Deputy Director

The Ferdinand-Braun-Institut

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Development of Sub-mm Wave Flip-Chip Interconnect

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Abstract

This research focuses on the design, fabrication and RF characterization of AuSn flip-chip bump interconnects for sub-mm wave chip package applications. Flip-chip bonding is the most suitable interconnect scheme for the high-frequency range due to its low inductance. In this study, several experimental models have been designed by using coplanar waveguides (CPW) and stripline structures together with miniaturized eutectic AuSn bumps to investigate the mechanical and electrical characteristics of flip-chip interconnect in the high-frequency area. The first flip-chip module started from a simplified CPW-to-CPW structure, operating at frequencies up to 220 GHz. The second interconnect module was fabricated using a stripline-to-CPW structure, leading to the operating frequency of more than 250 GHz. The third flip-chip module was developed in form of a stripline-to-stripline interconnect, adding an optimum shielding system, which allowed operation at frequencies up to 500 GHz. All of the transmission lines (CPW, microstrip and stripline) were designed based on the optimum electromagnetic results obtained from the simulated 3D model. The 10 μm AuSn microbumps were fabricated using the evaporation technique and subsequent lift-off. After mounting the chip on the substrate using a flip-chip bonder, scattering parameter measurements were performed, characterizing the interconnect quality, using the on-wafer multi-line Thru-Reflect-Line (TRL) method. Finally, the novel flip-chip technology was implemented as a first demonstration of a packaging concept for MMICs using InP double-heterojunction bipolar transistors (DHBT).

Zusammenfassung

AuSn Bumps basierend auf der sogenannten Flip-Chip Technologie bieten aufgrund ihrer elektromagnetischen Eigenschaften vor allem im hohen Frequenzbereich eine interessante Möglichkeit als Verbindungsstruktur zwischen MMICs untereinander sowie zwischen MMIC und Trägersubstrat.

Diese Arbeit beschäftigt sich mit Design, Herstellung und der elektrisch-mechanischen Charakterisierung dreier Modellstrukturen, in denen Kombinationen aus koplanaren Wellenleitern und Stripline Strukturen mit eutektischen AuSn Bumps Anwendung fanden. Die Designs der Leitungen sind Resultat einer Optimierung in vorher durchgeführten 3D Simulationen. Die Fertigung der 10um AuSn Microbumps erfolgte mittels Elektronenstrahl-Evaporationsmethode und anschließendem Liftoff. Nach der Montierung der Bauteile auf einem AlN Trägersubstrat mit Hilfe eines Flip-Chip Bonders wurde die Qualität der Verbindung mit Hilfe der Streuparameter kontrolliert, die nach der TRL Methode (multi-line thru reflect line) auf Waferlevel gemessen wurden.

Das erste auf diese Art hergestellte Flip-Chip Modul basierte auf einer vereinfachten CPW-zu-CPW Struktur und erreichte eine Frequenz von bis zu 220 GHz. Das zweite Modell wurde als Stripline-zu-CPW gefertigt und konnte bis 250 GHz betrieben werden. Bei der dritten Teststruktur im Stripline-zu-Stripline Design wurde besonderes Augenmerk auf die Minimierung von Abstrahlverlusten sowie von Verlusten bedingt durch die Anregung höherer Feldmoden gelegt. Diese erlaubte schließlich den Betrieb bis zu einer Frequenz von 500 GHz.

In einer ersten Machbarkeitsuntersuchung wurden Flip-Chip-Module mit InP-MMICs realisiert.

Contents

Chapter 1

Introduction

1.1 Motivation

Recently, the demand for high frequency electronics has been increasing rapidly, particularly in the so far mostly unexploited terahertz (THz) region. THz commonly denominates the frequency range between 300 GHz and 3 THz, corresponding to a wavelength of 1 mm down to 0.1 mm. The THz range offers the possibility of a wide range of applications, such as in medical imaging or security scanning, radar systems, spectroscopy, as well as broadband wireless communications [1–7].

Regarding the development of THz electronics, besides optoelectronic devices, particularly THz transistors have been receiving a lot of attention. Several research groups are adding their efforts to increase the operation frequency of their monolithic microwave integrated circuits (MMICs) such as high-electron-mobility transistors (HEMT) or heterojunction bipolar transistors (HBT). These THz transistors are the main components supporting those ultimate-frequency applications. Without these transistors, frequency conversion systems using multiple circuits up to mm-wave range would be required, leading to drawbacks in bigger circuits, increasing losses, and yields.

But to develop high-speed chips is only one part of the story. These chips also need their connection to the outside world. Therefore, apart from the interconnects of these high-frequency transistors, the packaging, which is the outermost boundary to restrict operation

frequencies of a system also need to be developed in parallel. In practice, ideal zero-loss transitions cannot be fabricated, and special care has to be taken in the development to reduce parasitic losses to a minimum extent.

Principally, there are two important factors to be considered in order to create a proper sub-mm wave interconnect. These considerations are 1) selecting suitable chip connection methods and 2) choosing appropriate planar transmission lines. In general, there are two well-known interconnect technologies for chip connections. These are wire bond and flip-chip. With increasing frequencies, the wire bond technology suffers from intrinsic parasitic effects which are essentially self-made due to its wire length. For flip-chip technology, in contrast, the interconnect path through bumps is much shorter, yielding a significant reduction of parasitic inductances. This has turned flip-chip interconnects into a promising technology for sub-mm wave applications and justifies its use in the present thesis.

Apart from choosing the suitable chip-connection technology, to select an appropriate planar transmission line is also one of the key tasks in the design of devices with increased system bandwidth. The choice of a suitable transmission line should based on the desired target frequency as well as the feasibility to be successfully integrated into the system. Among several line systems, microstrip (MS), coplanar waveguide (CPW) and stripline are potential candidates to fulfill these conditions.

Besides the criteria mentioned above, there are other substantial details which need to be considered during the development of high-frequency packaging at this level. These parameters are for example substrate materials, bump dimensions, bump pads, distance between chip and substrates and transmission line geometry. They need to be adjusted according to the application of the transition.

1.2 Scope and Outline

The goal of this research was to develop flip-chip interconnects for sub-millimeter wave frequencies and to implement them as a first-level packaging concept for InP heterojunction bipolar transistors (HBTs). Hence the operating frequency of interest is somewhere beyond 220 GHz. The major part of this work focuses on the fabrication of passive flip-chip interconnect modules using different planar transmission line concepts: coplanar waveguide (CPW)

and stripline designs in combination with eutectic AuSn bumps, leading to the development of three passive flip-chip modules suitable to the respective frequency bands up to 220, 325 and 500 GHz. In addition, a diamond layer is integrated to the construction. Due to its high thermal conductivity properties, the latter is considered as a heat sinking layer for the target InP HBTs.

A previous study [8] shows that keeping the transition areas as well as the bump dimension as small as possible helps to increase the frequency. Based on this knowledge, 10 µm AuSn microbumps have been developed for all of the experiments described in this thesis, including the AlN submounts for InP HBT chips [9].

Illustrated in Figure 1.1 is the project's development road map, providing different cross-sectional structures of four flip-chip experiments for the study timeline. Beginning in April 2012, the study started with the development of 220-GHz flip-chip module. Then the operating frequency has been increased to 325 GHz and further to 500-GHz. At the final stage of the study, which took place in December 2015, the flip-chip technology was implemented to the active HBTs. The details about each development phase will be provided in the following sections.

The thesis consists of seven chapters in total.

- The next chapter, chapter 2, reviews the background and state of the art of sub mm-wave packaging. Additionally, an overview of the planar transmission lines used in this work and details of flip-chip technology are given. The chapter closes with a small introduction to the FC150 bonder, as it was routinely used for this thesis.

- Chapter 3 presents the first flip-chip iteration up to 220 GHz utilizing CPW-to-CPW lines, including the fabrication details of the miniaturized AuSn bumps.

- Chapter 4 reports the second flip-chip development using a stripline-to-CPW structure, aiming at the frequencies beyond 250 GHz. The measurement results of the fabricated samples are discussed and compared to the values predicted by the simulations.

- Chapter 5 presents the third experiment using the stripline-to-stripline interconnect, extending the frequency up to 500 GHz. This exceeds the frequency values reported in the literature until now. Furthermore, the influence of process tolerances such as misalignment of bump positions, variation in line geometries, and dielectric thicknesses will be analyzed using 3D EM simulations.

- In chapter 6, the results of InP HBT flip-chip are discussed.

- Finally, chapter 7 gives an overall summary and provides an outlook for possible future work.
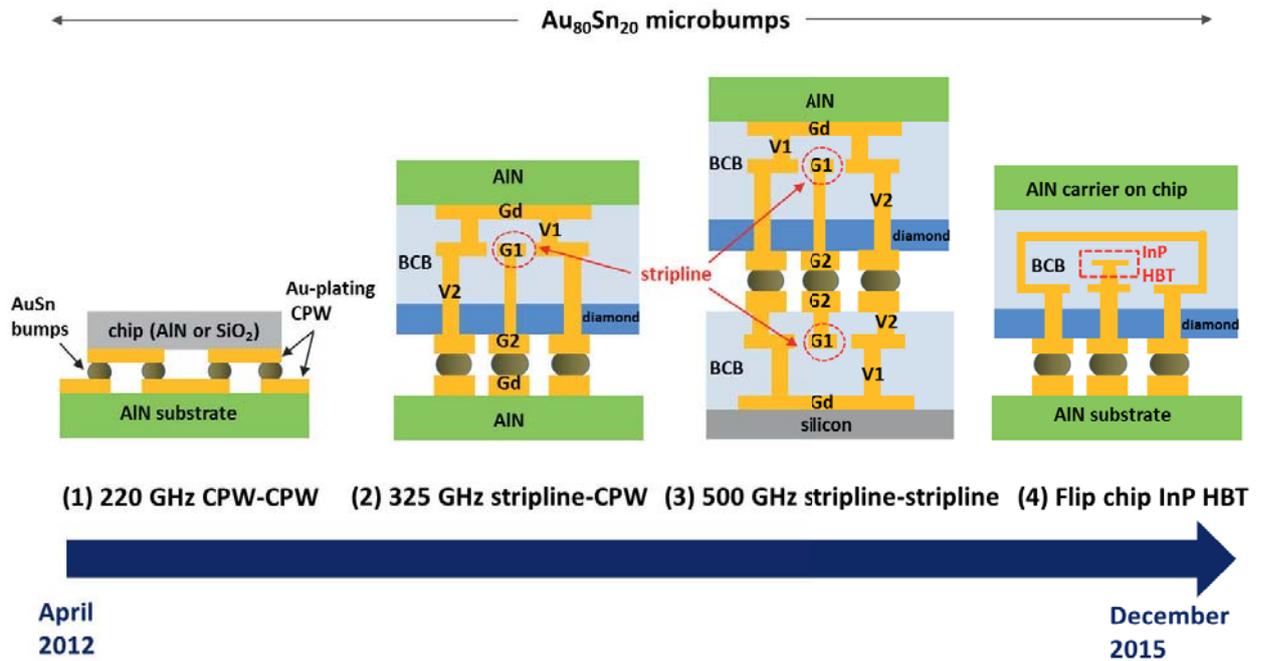

Figure 1.1: Development roadmap of flip-chip for sub-mm wave applications, showing four different cross-sectional structures of chips and substrates connected through AuSn bumps flip-chip. Three passive flip-chip interconnects were developed, using different combinations of planar transmision lines, gaining frequencies of 220 GHz, 325 GHz and 500 GHz (1)-(3). In the last development phase, the flip-chip technogy was implemented to InP HBT (4).

Chapter 2

Sub-mm Wave Flip-Chip Interconnect

2.1 Microwave and mm-Wave Packaging

In general, the packaging system can be classified at least into three levels [10]. The first-level packaging (chip-to-package) relates to the connection of bare dies directly onto their carrier substrates to generate the first possible electrical contact of chips to the outside system. This can be done by several assembly techniques, mostly by wire bonding and flip-chip mounting. The second-level packaging (package-to-board) is the attachment of the first-level packaged chip onto a motherboard or printed circuit board (PCB). The third-level packaging refers to the assembly of several circuit boards into a system.

In a similar way as for low-frequency packaging, in microwave and millimeter-wave areas device packages also have their functions to deliver signal and power of IC circuits to outer systems, to support mechanical stability of chips and to protect the devices from the environment, as well as to dissipate heat from the system [10]. Note, however, that for high-frequency applications, as operating frequencies increase, parts of the packaging themselves can turn to be a source of parasitics, deteriorating signal propagation or provoking resonance in the system [11]. This adds more complications to the design of mm-wave packages as compared to conventional ones. A short review of some concerned topics which need extra considerations for high-frequency packaging is given as follows [12]:

Distributed effects

The point that makes mm-wave packaging totally different from the low-frequency one is that at high frequencies all of the packaging components such as wire bonds and dielectric mold compounds do not just act as a connection or a chassis of the system. At such frequencies, their hidden lumped elements, for example an inductance from wire bond and a capacitance from the dielectric material, behave differently. Depending on the operating frequencies the dielectric capacitance acts no longer as a pure capacitance but also emerges the inductive effect into combination. A wire bond is not solely a metal connection between two points. Instead, the signal starts radiating from the wire and converting the metal wire to an antenna of the system or distinctly presents the inductive effect. This phenomenon is called 'distributed effect', which means that the electrical behaviors change when the operating frequency is increased [12]. This occurs because at mm-wave frequencies, the physical dimensions of the devices become a fraction of a wavelength. As a result, the packaging strongly affects the electrical characteristics of the whole electronic system. Therefore, mm-wave packages have to be carefully designed based on their operating frequencies, taking the distributed effect into account.

Resonances from signal coupling and radiation

At mm-wave frequencies, undesired coupling and radiation can occur wherever in the circuit where metal lines are placed close to each other. Cross talk and radiation are the cause of resonances which degrade signal performances. The resonances not only occur from the coupling between circuits but they also happen from a cavity inside a metal package. It is difficult, however, to detect this problem during the design phase, because the coupling and radiation only appear while the electrical measurement is performed. Nevertheless, with modern EM simulation software these effects can be predicted, and rough distances that metal traces need to be separate from each other should be able to be defined.

Choice of materials

Choosing suitable materials is one of the critical subjects for mm-wave packaging, having in mind that the material properties affect the characteristic impedances, which directly

influence insertion losses. For instance different types of dielectric contribute in dielectric losses by their loss tangents, and metal types impact conductor losses.

Thermal management Another point which needs to be taken care of not only for low-frequency packaging but also for mm-wave packaging is the thermal management [11]. This is because devices generally rise up the heat during operation. Therefore it is important that the packages offer a good thermal management. This can be done by several techniques including the attachment of a heat-sinking material such as CuW, AlSiC and AlN [13–15], drilling thermal vias to connect to the high-thermal conductivity substrate and using flip-chip bumps for thermal dissipation.

The next section starts with the packaging construction concepts. This is to give an overview of mm-wave packaging/housing before further examining the interconnect concept of the first-level packaging, which is the focus of this dissertation.

2.1.1 Types of mm-Wave Packages

In principle, good mm-wave packagings need to fulfill two system requirements which are 1) providing excellent electrical performances and 2) having the potential for low cost production. In reality, to develop a choice of packages, which can combine these two aspects, is a big challenge. Obviously, these two requirements are a trade-off to each other. In the sub-section below, the overview of different mm-wave packagings is presented according to the purpose of their developments.

2.1.1.1 mm-Wave Packages with High Electrical Performance

Metal-housing packages [16]

For an excellent performance, metal housings are one of the best packaging solutions because they offer excellent shielding to the system. But using a metal chassis increases the packaging cost. Depending on the applications, metal packages are made for two types of devices, which are discrete devices and complex modules, as illustrated in Figure 2.1 (right).

Figure 2.1: Development of mm wave packaging as compared to conventional packaging, adapted from [16].
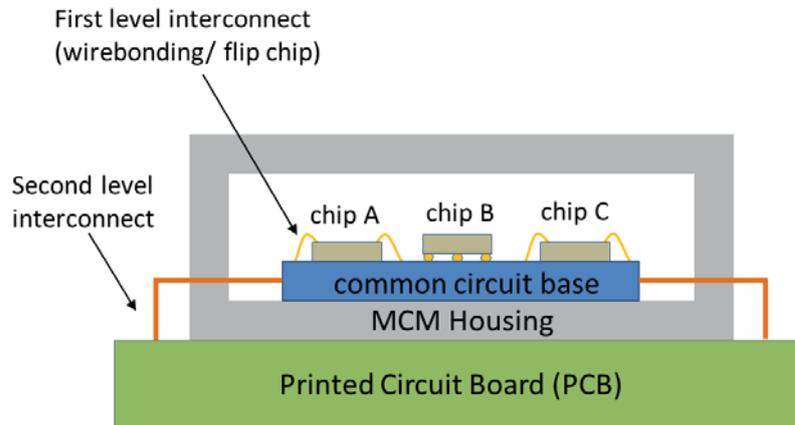
Figure 2.2: Illustration of MCM concept, adapted from [17].

For the discrete device package, it is named split-block package because the package is composed of two metal parts, combined together as an mm-wave housing. The split-block package is normally used for single devices such as MMIC, transistors and waveguide transitions. Unlike the split-block, the complex packaging module combines different device functions together in one metal block. Both of these metal packages are mostly made of aluminum, coated with gold to avoid corrosion. The construction of the packaging is done using a milling technique, most likely with the aid of computer numerical control (CNC). Therefore, these packages can be called 'CNC Milled Metal Housing'.

For both packaging styles, several methods such as wire bonding or flip-chip technology are applied to connect a chip inside the metal body. To provide good RF isolation between the individual units the wave propagation inside the package is suppressed by limiting the width and height of the package less than half of the wavelength at the target operating frequency or by attaching absorbing materials to the packages.

Multichip-module packages (MCM) [16, 17]

Another attempt to increase packaging performances is by using multichip-module packages (MCM). The concept of this packaging is to connect several different chips through the first-level interconnect, and to reduce the second-level packaging or the outer connection as much as possible, as parasitic effects of this packaging level can easily degrade the total system

performance [17]. Additionally, using MCM also leads to the reduction of module size while increasing the degree of integration [18, 19].

Typically, the MCM packages can be classified into three types, depending on their substrate materials. These are are MCM-L for laminated substrates, or PCB (printed circuit board), MCM-C for ceramic substrates and MCM-D for deposition of dielectric substrates. Amongst these three types of MCM, the ceramic MCM offers the best thermal conductivity and also the lowest loss.

2.1.1.2 Low-Cost Packages

Plastic-molding packaging

Plastic-molding packages are widely used as standard packaging technologies at low frequencies. These types of packages are for example DIP (dual in-line package), SOIC (small outline integrated circuit), PLCC (Plastic leaded chip carrier), QFP (Quad Flat Package), QFN (quad-flat no-leads) and BGA (ball grid array), as shown in Figure 2.1. In general, there are two different techniques of mounting the packages on a board. These are 1) through-hole (PTH) technology and 2) surface-mount (SMT or SMD) technology. For the PTH method, the package pins will be inserted into the exact footprint holes on the board. In contrast to the PTH, mounting the SMT can be done by placing and soldering the device on one side of a printed circuit board (PCB) without the package pins penetrating to another side of the PCB. In the group of the packages shown above only DIP represents the through-hole mounting type.

As plastic materials are much cheaper compared to metal packages, they are very attractive for high-frequency packaging in term of cost reduction. However, plastic materials are lossy. This can degrade the overall system performance.

Amongst all the conventional plastic packages used in low-frequency applications the QFN package is the one which is often adapted to mm-wave packaging [20]. In principle, the QFN package is done by attaching the MMIC dies on a lead frame using epoxy. These MMIC dies are connected to the electrical pads through wire-bonding technology before the whole construction is molded using a plastic compound, in the case of fully molded-package. Bessemoulin et al. [21] present the use of plastic QFN to power amplifier MMICs up to 20

GHz. It is shown that at this frequency the conventional mold compounds can be attached directly to MMIC dies. But for 40 GHz applications, an air gap between chip and package is required in order to avoid physical contact, which generates parasitics. Lin et al. [22] reported the use of the full-molded QFN packages up to 50 GHz, but additional via holes and multi wire bond at the ground pads need to be implemented.

Generally, thermal management is a major concern in broadband packaging. Nevertheless, this issue can be solved by attaching the packages to thermal dissipation materials such as AlSiC, AlN, CuW, etc. or by adding thermal vias [11]. But when choosing the heat sinking material, the coefficient of thermal expansion (CTE) also needs to be considered in order to avoid the stress occurring between the heating device and the heat-sinking material [23].

Wire bonding and flip-chip technologies are typical interconnect techniques used to connect the chips inside their packages [24]. This dissertation focuses on the flip-chip technique because it has shown several advantages over wire-bonding method at high frequencies, which are [25–27]:

1. Flip-chip offers a much shorter interconnect path comparing to wire bond, resulting in small parasitic inductances which lead to high bandwidth.

2. Flip-chip offers a good mechanical stability. Unlike wire-bonding technology, bump forms and bump shapes can be predicted.

3. The overall package size is minimized using flip-chip due to its short path of connection.

Although heat dissipation in wire bonding can be done in the larger area through the die attach, the heat dissipation in flip-chip can also be provided through bumps. In order to create a good first-level high frequency interconnect, as already mentioned in chapter 1, there are two major concerns: 1) selecting suitable transmission line types for the desired frequency and 2) choosing a proper interconnect technology with a proper design transition. Details of these two points are described in the following sections.

2.2 Planar Transmission Lines for High-Frequency Applications

There are several types of planar transmission lines which have been investigated until now [28–30]. To select a suitable transmission line structure, its circuit type and operating frequency need to be considered. This is because each line structure interacts with the electric and magnetic fields differently, leading to different modes of propagation. There are three basic modes of propagation in 'guided' structures with homogeneous cross-section. These are the transverse electric (TE) mode, the transverse magnetic (TM) mode and the transverse electromagnetic (TEM) mode [28, 31].

In the TE mode, only the component of magnetic field appears in the direction of propagation but no electric field component in this direction. In contrast, the TM mode has no magnetic field in the direction of propagation but solely the electric field exists. Unlike these two modes, in TEM mode there is no electromagnetic field in the wave propagation direction at all. The existing electric and magnetic fields in this mode are perpendicular to each other and also to the direction of propagation. This is a desired mode of propagation because it is practically dispersion free for the desired frequency range. The TEM mode occurs when transmission lines have at least two conductors and the wave travels in only one medium. A stripline is a good example of a planar transmission line which supports the TEM mode [28]. In comparison to the pure TEM mode, the so-called quasi TEM requires the wave traveling within two or more different media (these are typically a dielectric material and air). This leads to a change in the effective dielectric constant, which accounts for a phase velocity change and hence a signal dispersion. Planar transmission lines, which support the quasi TEM mode are, for instance, microstrip and coplanar (CPW) lines [28, 30].

Besides the above mentioned modes of propagation, there are also hybrid modes (HE and EH modes) [32] the longitudinal electric and magnetic field components of which are non-zero. Both HE and EH modes are found in inhomogeneous-dielectric waveguides [32], for instance.

In this work, the main transmission lines under investigation are microstrip (MS), coplanar waveguide (CPW) and stripline. The concept of these three line types is discussed in the following sub-section in more detail.

2.2.1 Microstrip

Microstrip line is one of the widely used planar transmission lines in microwave integrated circuits because the structure is easy to fabricate, and all the active devices can be directly attached on a surface panel [33]. The cross section of a microstrip line is depicted in Figure 2.3. The structure consists of two metal layers: a thin signal-conducting strip and a metal ground plane. These two conducting layers are separated from each other by a dielectric substrate.
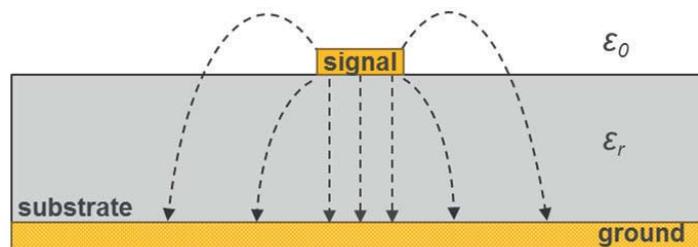

Figure 2.3: Cross section drawing of microstrip (MS).

Although the microstrip looks rather simple the field behavior in the microstrip is more complicated than its structure. This is because the signal strip lies at the interface of two different dielectric materials, which are the substrate with the dielectric relative permittivity ε_r and the air surrounding the upper part of the strip, with the dielectric constant ε_0, respectively. Because of this non-uniform dielectric, the fields spread into two media and change abruptly at the substrate-air interface. The non-uniform dielectric does not allow the microstrip lines to support a pure TEM mode, and result therefore in a quasi-TEM propagation.

Since there are two dielectric materials involved in how the fields behave in the microstrip lines, a parameter called 'effective dielectric constant' ε_{eff} is required to further analyse the characteristics of the microstrip. This effective dielectric constant is a value which, let's say, includes both the quantity of the fields spreading into the dielectric substrate and the one extending in the air. The effective dielectric constant is the representative of the whole dielectric and makes the scenario of the microstrip as if it functions under only one dielectric material.

The characteristic impedance of the microstrip is influenced by three important parameters which are 1) strip width 2) substrate thickness and 3) substrate dielectric constant. If the microstrip line has the same width as the ground plane, the structure will then act as the parallel plate, resulting in the field concentration only inside the metal plates. In the case of narrow strip width (normal microstrip), a high-enough dielectric constant substrate is required to confine the electromagnetic fields inside the dielectric underneath the metal strip, reducing the radiation loss [30]. This radiation loss is one of the disadvantages of the microstrip due to its open structure, spreading the fields out to the environment, and thus, creating undesired electrical response to active devices. Therefore, a shielding system might be required for some applications.

Another drawback of the microstrip is that the line is considered as dispersive transmission line, which means that the phase velocity of signal propagation changes when different frequencies are applied. This is a typical phenomenon in non-TEM mode. An additional difficulty of the microstrip line in terms of fabrication is that in order to access the ground plane physically, via holes need to be provided. This adds more complications to the process.

2.2.2 Coplanar Waveguide

The coplanar waveguide (CPW) is constructed by using only one single metal layer to form a signal strip and ground planes on the same side of the dielectric substrate (see Figure 2.4) [34]. The signal line is placed between the two ground planes, electrically separated by small gaps. In CPW, the ratio of signal width and signal-ground spacing dominantly affects the characteristic impedance of the line [29]. Unlike the case of MS, the substrate thickness of CPW does not influence the line impedance because the ground planes are located in the same layer as the signal strip, making the fields concentrate only between the signal-ground metal slots.

In principle, the CPW line can support two modes of propagation. These are CPW mode (or even mode) and slotline mode (or odd mode). The desired mode of signal propagation in a CPW is line is the CPW mode. Within this CPW mode, both ground planes are at the same potential. Hence, the field starts from the centre strip and and ends at each side of the ground (fields go in opposite direction starting from the middle strip). The CPW mode supports signal propagation in quasi-TEM and gives low radiation loss.
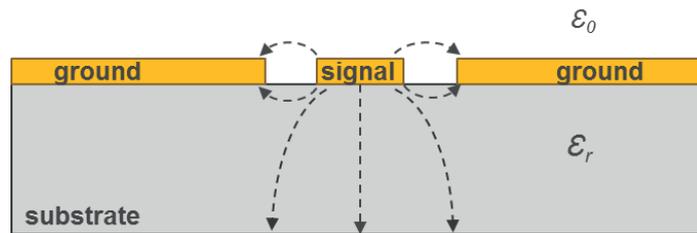
Figure 2.4: Cross-sectional coplanar waveguide (CPW) structure on dielectric substrate, showing CPW mode (even mode).

For the unwanted slotline mode (or odd mode) both ground planes have different potentials, which can be a result of asymmetric line dimensions or discontinuities [35]. In this case, not only the fields start at the middle strip but also at a ground plane as shown in Figure 2.5. One way to suppress the slot line mode is to physically connect two ground planes together using the air bridge in order to keep the potential of ground planes identically [29].
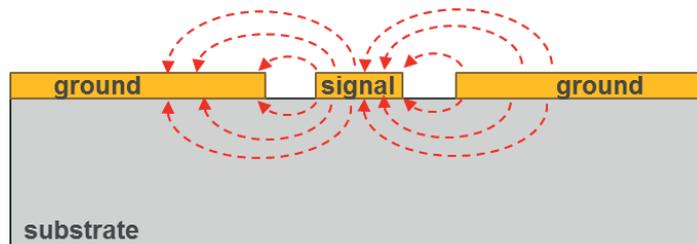
Figure 2.5: Cross-sectional coplanar waveguide (CPW) structure on dielectric substrate, representing slot line mode (odd mode).

One big advantage of the CPW is that the structure can be simply fabricated without a need of any via holes since all the conducting metals are in the same layer. The CPW features can be well-defined using stepper lithography, which makes it possible to minimize dimensions of the signal strip and signal-ground gaps. The smaller these features become, the more fields concentrate in the slot, giving the CPW a great potential of having low radiation and low dispersion, especially when comparing to the microstrip. However, in sub-mm-wave operations, radiation losses in CPW are also increased.

2.2.3 Stripline

In principle the stripline is a flattened form of a coaxial line. The stripline structure contains three metal layers: the space between top and bottom ground planes is filled with homogeneous dielectric material, with the signal conductor embedded within this dielectric as illustrated in Figure 2.6.
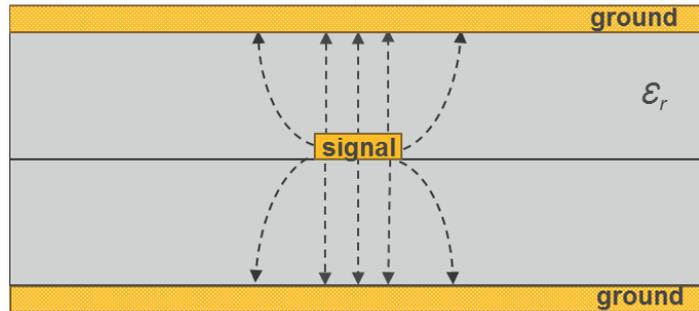
Figure 2.6: Cross-sectional structure of stripline with a signal width in the middle between two ground planes.

The key parameters that determine the characteristic impedance and line loss of a stripline are strip width as well as dielectric constant and loss tangent of the dielectric material involved, the distance from signal to grounds, and the surface resistance of the metal conductor.

As the field propagates in one medium only, the stripline fully supports TEM mode, resulting in no change of phase velocity and characteristic impedances at different frequencies (non-dispersive). This makes the stripline approach suitable even for very high-frequency areas.

The disadvantage of the stripline is, however, that the structures need a via interconnect between two ground layers. Adding via holes lead to a complication in the fabrication steps and the processing time will be longer compared to those of CPW and microstrip line.

Transmission lines	Modes	Dispersion	Radiation
Microstrip	Quasi-TEM	medium	higher than CPW
CPW	Quasi-TEM	low	low (dimensional control)
Stripline	TEM	none	none

Table 2.1: Summarized overview of the planar transmission lines microstrip, CPW and stripline.

2.3 Loss Mechanisms in Transmission Lines

In an ideal transmission line, a sinusoidal signal propagates between two points without any changes. This ideal transmission line is known as a lossless transmission line. But in reality, there is always a difference between an input signal from point one and the output signal at point two. This is a result of various loss mechanisms in the transmission line. In order to understand where these losses come from, we have first to understand the propagation constant, which is an important characteristic of the signal transmission.

The propagation constant γ describes the behavior of electromagnetic fields in a transmission line. As a complex entity, the propagation constant contains a real part α (attenuation constant) and an imaginary part β (phase constant), and can be formally written as

$$\gamma = \alpha + j\beta$$

From the equation, the attenuation constant α indicates a real loss (or amplitude loss) of the sinusoidal signal that occurs during the signal propagation, while the phase constant β expresses the phase of signal at a constant time. There are three main causes of losses. These are conductor losses, dielectric losses and radiation losses [36]. These loss mechanisms are discussed as follow:

2.3.1 Conductor Loss
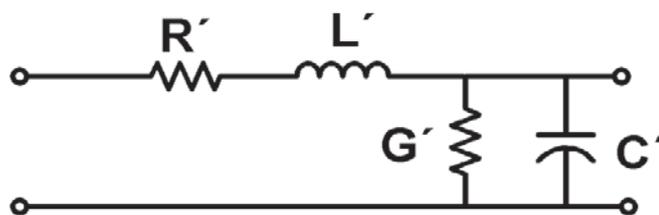
Figure 2.7: Equivalent model of a transmission line.

As described in [37], a transmission line can be schematically drawn as four distributed elements as shown in Figure 2.7. Taking a look inside the transmission line model, the

conductor loss, which clearly relates to the metal used in the transmission line, can be expressed by a normalized resistance R' (resistance per unit length). This resistance is defined by the geometry and the property of the metal materials.

In the case of DC environment, the resistance of the metal is a constant value. But at high frequency the situation of resistance of a metal is different. At this circumstance when frequencies f change, the resistance is increased proportional to $\sqrt{f}$. This is due to the so-called skin-effect [29]. The relation of the surface resistance to the frequency and the material property can be generally demonstrated in the equation below:

$$R_s = \sqrt{\frac{\pi f \mu}{\sigma}} = \frac{1}{\sigma \delta}$$

where

f = frequency

μ = permeability of the conductor (usually $\mu_0 = 4\pi \times 10^{-7}$ H/m)

σ = DC conductivity of the conductor ($\Omega \cdot \text{m}^{-1}$)

As it is presented in the equation, the 'skin depth' δ is the significant parameter, which influences the surface resistance.

δ denotes the field-penetration distance and is measured from the conductor surface. It can be calculated by

$$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}}$$

As can be seen from the above equation, by increasing the frequency, the skin depth δ is decreased. This actually means that at high-frequencies, metals thicker than the skin depth are not required for signal conduction, as the currents travel only at the skin surface of the metal. This is also an interesting aspect in terms of cost reduction. Table 2.2 shows the frequency dependence of skin depths for different conductor materials.

Metal	ρ (μΩ · cm)	500 MHz	1 GHz	2 GHz	5 GHz	10 GHz
Gold	2.44	3.5 μm	2.5 μm	1.8 μm	1.1 μm	0.79 μm
Tungsten	5.49	5.3 μm	3.7 μm	2.6 μm	1.7 μm	1.2 μm
Aluminum	2.62	3.6 μm	2.6 μm	1.8 μm	1.2 μm	0.82 μm
Copper	1.72	3.0 μm	2.1 μm	1.5 μm	0.93 μm	0.66 μm
Silver	1.62	2.9 μm	2.0 μm	1.4 μm	0.91 μm	0.64 μm
Nickel	6.90	5.9 μm	4.2 μm	3.0 μm	1.9 μm	1.3 μm

Table 2.2: Skin depth δ of various conductor materials at different frequencies [38].

2.3.2   Dielectric Loss

Dielectric loss is a loss which comes from the energy loss during the signal transmission through a dielectric material. This loss occurs either because of the presence of free electrons or by dipole relaxation phenomena [36]. When different potentials apply between two points of metal transmission lines, polarization occurs. This results in the movement of charges or molecules with a dipole moment in the dielectric material, as they try to align themselves to the field directions. During this displacement, the charges and molecules collide to each other. As a result, the energy loss occurs in the form of heat dissipation.

The dielectric loss is influenced by the frequency as well as material properties. In general, the dielectric loss is proportional to the frequency: the higher the applied frequency, the greater the loss from energy dissipation. In term of material properties, the dielectric loss can be demonstrated by the material's loss tangent and the dielectric constant. The loss tangent is the value indicating how lossy the dielectric material is, whereas the dielectric constant k is the ratio of permittivity of dielectric material to the free space.

2.3.3   Radiation Loss

Radiation losses are the energy loss occurring when an electromagnetic wave propagates away from the surface of the transmission line conductor [39]. Radiation losses are one of the major concerns for open transmission lines such as microstrip [40]. Parameters involved in radiation loss are dielectric constant as well as distances between metal conductors and transmission line length. The radiation loss can be minimized by implementing a good

shielding technique to a transmission line. One example of an excellent shielding line system is a coaxial cable, which is actually considered as an excellent non-radiated transmission line [28].

2.4 Sub-mm Wave Interconnects

2.4.1 Wire Bond and Flip-Chip

As already discussed in the previous chapter, the two main interconnect methods used in the first-level packaging are wire bond and flip-chip. There are several investigations with particular focus on the use of these two techniques in high-frequency applications. As frequency increases, wire bonding severely suffers from parasitic effects because the length of the wire cannot be scaled down enough [41–47]. Several research groups have investigated the wire-bonding connection on coplanar transmission line. T. Krems et al. analyzed the wire bond between 60-120 GHz using a raised coplanar model [42]. It is clearly stated in this work that increasing the wire length dramatically increases insertion losses. In [48], the attempt of using wire bond itself as a coplanar transmission line was analyzed. It was shown that the height of wire bonding from the substrate and the wire spacing determine the characteristic impedance of this wire-bond coplanar waveguide. Special methods such as low-loop ribbon bonds [49–51] and compensation of bond wire interconnect [52] were attempted to increase the operational frequency, but still without reaching values beyond 100 GHz. Li et al. [53] suggested the approach of reducing interconnect distances with optimization of the pad area, which yielded a wire bonding performance up to 170 GHz. Nicholson et al. could show the importance of wire bond impedance matching associated with the difficulty in controlling the wire shape [54]. As can be seen in these studies, the biggest obstacle to implement wire bond to sub-mm wave band is the wire length itself. Therefore, the idea of using flip-chip to shorten the connection path was emerged, and several groups started the investigation on using wire bond and flip-chip in high-frequency applications [55, 56]. Beer et al. [57] compared the use of flip-chip interconnect to wire bonding using CPW lines, connecting between silicon MMIC to antenna in the frequency range between 110 - 170 GHz. It is clearly indicated in this study that the wire length results in high impedance, and limits the bandwidth of wire bond. On the other hand, the flip-chip interconnects offer a shorter connection path, leading to a lower line impedance and resulting in a broader bandwidth.
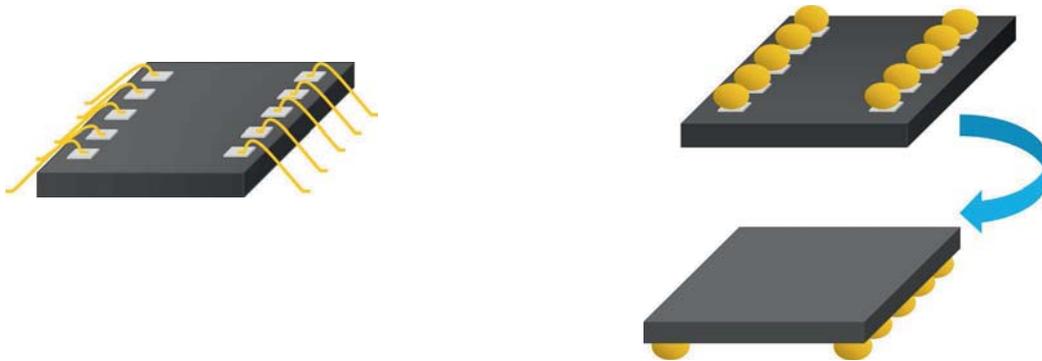
Figure 2.8: Chip interconnect techniques: wire bonding (left), flip-chip (right).

2.4.2 State-of-the-Art Sub-mm Wave Flip-Chip

The first generation of solder-bump flip-chip or so-called Controlled-Collapse Chip Connection (C4) was introduced by IBM in 1964 [10, 58–60]. Since that time the manual wire-bonding led to high expenses, unreliable contacts and low producibility. The need of finding a better interconnection then occurred. The C4 means a method of depositing solder bumps on wettable pads of a chip and at the same time also preparing wettable pads on a substrate which have matching footprints to the chip side. Then the chip will be upside-down placed on to the substrate. The joining is done by soldering reflow. The first version of C4 bumps had typical dimensions between 100 - 150 µm [58]. Since this new interconnection concept was successfully developed that time, several efforts have been dedicated to develop the flip-chip technology until now.

The flip-chip approach with its inherently shorter dimensions appears to be better suited for mm-wave and sub-mm-wave assemblies, but the vast majority of previous work is limited to frequencies up to the W-band [61–69]. Several investigations have been performed to study the RF characteristics of flip-chip, and also to find the best environment for sub-mm wave flip-chip. Although for the flip-chip interconnect, the transition combines both inductive and capacitive behaviors, Ghouz [70] demonstrated an overall capacitive characteristic out of the accurate equivalent flip-chip model. The result of this examination agreed well with Jentzsch
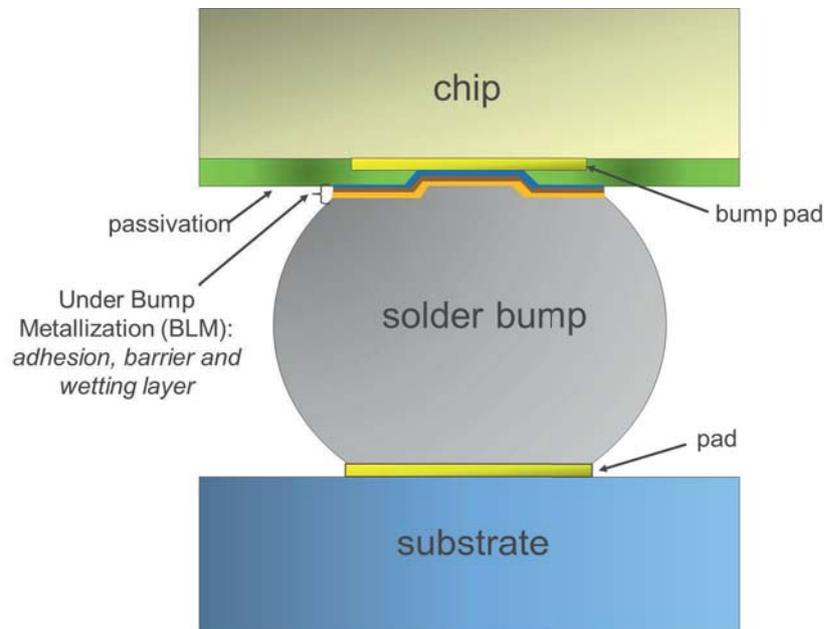
Figure 2.9: The first flip-chip concept 'C4', which was introduced by IBM [59].

[8] who found out that the capacitive effect from the dielectric surroundings overtakes the inductive effect from the current flow through the bumps.

Based on this knowledge, further analysis was conducted to find out methods to compensate this capacitive behavior. Jentzsch et al. [63] suggested two impedance compensation techniques which are 1) implementing staggered bumps and 2) using a high impedance line by adjusting the CPW gaps. Another interesting compensation technique, which is called "locally matching", can be done by increasing the CPW gaps around bump pad area [71]. This results in an increasing of inductance around the transition area and finally compensating the capacitance at that region.

W. Heinrich and A. Jentzch [63] explicitly examined designs and configurations of millimeter wave flip-chip interconnects using coplanar waveguide. From their analysis, it was concluded that small transition areas, small bump pads as well as tiny bump dimensions lead to a better flip-chip performance at mm wave. This is because the smaller geometries result in a small capacitance at the transition regions. Therefore, these dimensions should be kept as small as the technology allows. One more physical configuration affecting the parasitic

capacitance is the dielectric overhang between chip and substrate [8]. However, this effect can only be controlled by the dicing technology.

Another important aspect is the detuning effect or the proximity effect [8, 61, 72, 73], which is caused by the narrow space between chip and substrate after flip-chip mounting. Bringing chip and substrate close to each other can alter the electrical behavior of the devices due to the increasing of the relative dielectric constant ε_r. This effect can be avoided by adjusting the separation distance between chip and substrate, which, in practical can be done by adjusting the bump height. The detuning effect deteriorates the interconnect quality as presented in the study of Nagy et al. [74] in both CPW and MS lines. Apart from the small gap, the detuning effect can also get stronger when there is a metal layer on the submount surface [63]. From the examinations above, there are two straightforward techniques to prevent the detuning effect, which are 1) increasing the bump height in order to create a bigger gap between chip and substrate, and 2) minimizing the use of metallization under the chip side.

The special interconnect-configuration so called 'hot-via' was purposed avoiding the detuning effect using the faced-up bonding of on-chip MS to on-carrier CPW connecting a front-side and back-side metal through via [75, 76]. With this feature, results are reported up to 60 GHz. Bessemoulin et al. [77] have also taken the hot-via concept using CPW-CPW interconnect. Through their work the frequency increases up to 110 GHz.
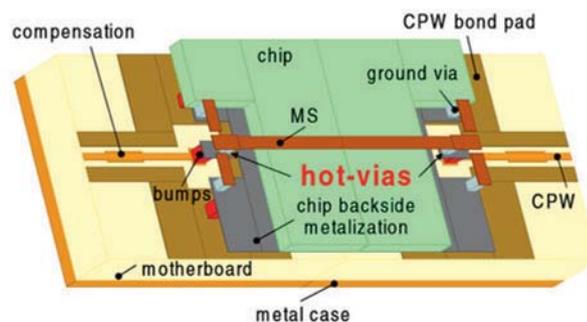
Figure 2.10: Hot-via structure (MS on chip and CPW on carrier) developed by Schmueckle [75].

It is known that the coaxial line is considered as the perfect transmission line. Therefore, various attempts to integrate the coaxial model on the planar transmission lines arised. One novel concept is to create multiple ground bumps around CPW-CPW transitions, forming

pseudo-coaxial shielding structures [78, 79]. Later on, the genuine coaxial CPW-CPW flip-chip was developed using the benefit of its excellent shielding environment [80, 81].
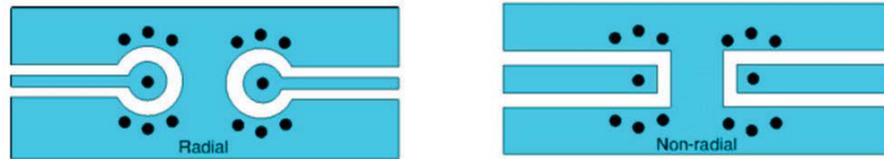
Figure 2.11: Shielding system using multiple ground bumps around the transition areas [78].
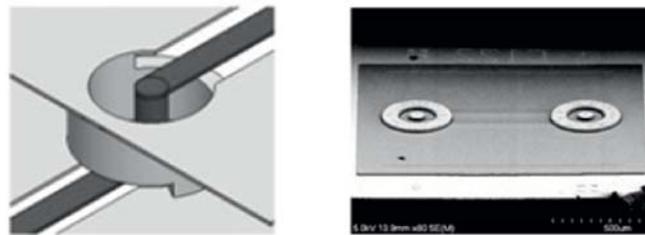
Figure 2.12: Coaxial transition developed by Wu et al. [81].

In 2014, Khan et al. [82] presented the use of high impedance inductive components to compensate excessive parasitic capacitances which occurred from the chip-to-substrate overlap, promoting their flip-chip performance up to 170 GHz.

2.4.3   AuSn Soldering Material

In this framework, the flip-chip bonding technology is implemented as a mounting technique for the InP HBT circuit. In contrast to the use of stud bumps in thermosonic flip-chip process, the flip-chip soldering requires a very low bonding force, which is suitable for bonding fragile chips [83]. However, the temperature of solder material needs to be maintained within the tolerance of the transistors. The eutectic $Au_{80}Sn_{20}$ is, thus, selected as a bump material in this study because of its low melting point (280 °C) compared to any other hard solder materials such as Au-Ge and Si-Ge, which have melting temperatures of at least 360 °C. The binary phase diagram of AuSn intermetallic is shown in Figure 2.14 [84]. Besides a suitable
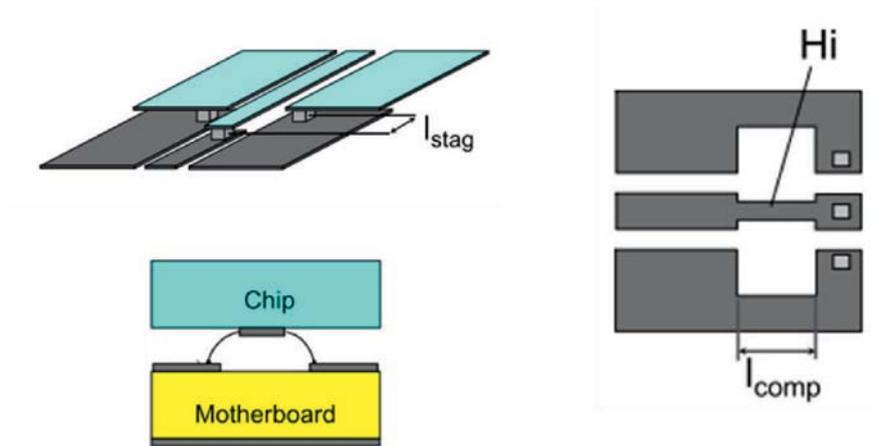
Figure 2.13: Compensation structures HI impedance [8].

soldering temperature, the eutectic AuSn offers a mechanical bonding stability, which is one of the hard-solder characteristic due to its elastic formation. Another point, which makes AuSn more attractive to broad applications is that AuSn is a fluxless bond-material. This is a very important criterion for electronic devices as used in optoelectronic and laser areas as well as for the HBT [85]. In the past, the use of flux is introduced in order to remove the native oxide layer, which is formed at the solder surface, degrading the bonding quality. But it is very difficult to clean these flux materials away without leaving any residues on the micro-features of the circuits, especially after the flip-chip mounting, where solely a small gap remains between a chip and a substrate [86]. Without using flux, two techniques are implemented for AuSn bumps to avoid the oxygen forming at the solder. First a gold cap is metallized on the outer bump surface to protect the oxide forming at the solder. Second, the flip-chip is bonded within the formic gas environment (N_2/H_2) to prevent the AuSn solder having direct contact with the O_2 atmosphere.

Several investigations regarding the formation of AuSn compound and its binary phase diagram have been carried out [84, 87]. It is well-known that when combining Au and Sn, Au quickly diffuses into Sn to form a Au-Sn intermetallic compound even at room temperature [88–90]. All of the mentioned work also reported the existence of four AuSn phases: ζ phase, AuSn, $AuSn_2$ and $AuSn_4$ can be detected after the unannealed evaporation. The experimental work of W. Pittroff et al. [91] presents the change of AuSn-bump textures during

the reflow process. It can be seen clearly in this study that during the reflow the evaporated multilayer AuSn bumps first develop into cluster structures. Subsequently, the clustering patterns turn into coarse grains and finally form the homogeneous eutectic textures. It is necessary to obtain uniform eutectic AuSn bumps, which offer excellent creep resistance, thus giving mechanical stability and reliability to the solder joints [92].

Although the quick diffusion is a major key of forming a good alloy, the interdiffusion between the AuSn bump and the supporting Au-pillar or Au-plating structure beneath the bump is undesired. Hence, the under-bump material (UBM) is needed as a diffusion barrier against unwanted reaction between Au pillar (or Au plating) and Sn in order to reserve the adequate amount of Sn for the eutectic forming process of AuSn, avoding the inaccurate final AuSn compositions. Several under-bump metallurgy materials such as W, Ni, Co and Pt were studied for this purpose [91, 93–97]. In this work, we have chosen the conventional UBM system: Ti/Pt/Au. As in several applications, Ti layer behaves as an adhesive layer, and Pt is the real diffusion barrier [98].
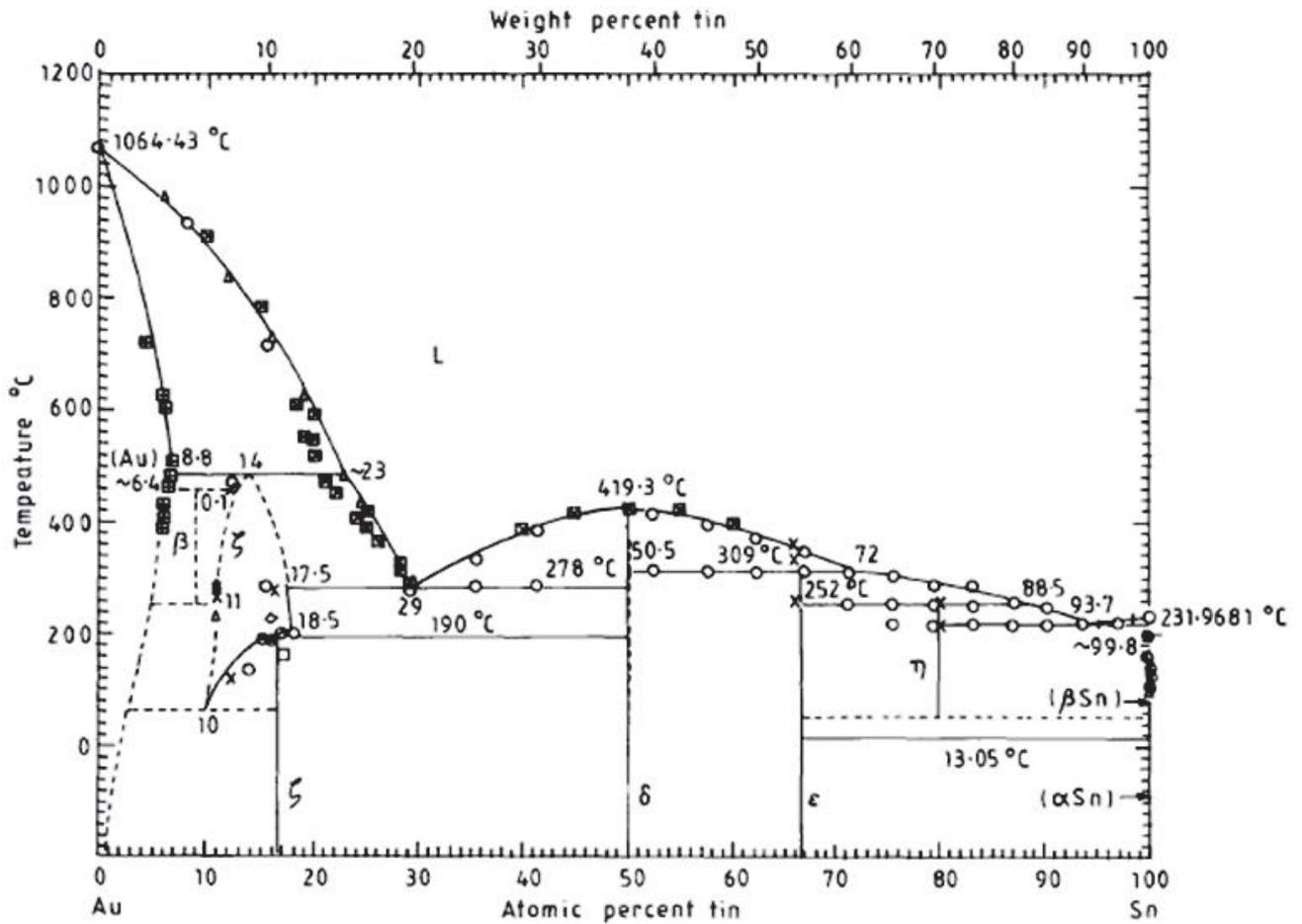
Figure 2.14: Binary phase diagram of AuSn intermetallic compound adapted from [84, 87].

2.4.4 Flip-Chip Bonding

The flip-chip bonder used in this work is a FC150 from 'Smart Equipment Technology (SET)', former product of Karl Suss, as illustrated in Figure 2.15. This bonder supports several bonding processes, including flip-chip soldering and thermo compression. The machine offers a high placement fidelity of $\pm$ 1µm and a great post-bonding accuracy in between 1-3 µm. The system supports a chip size of 0.2-100 mm with a chip thickness up to 2 mm, and a substrate size of 0.5-150 mm with a substrate thickness up to 6 mm. The machine allows

working temperatures from room temperature to a maximum of 450 °C with a resolution of 1 °C. The bonding arm force for the soldering technique can be set in the range of 0.2 - 4 N (around 20 - 410 gram-force). The mounting technique of this machine is compatible to vulnerable chip materials such as InP, which is the material used for the HBT devices in this project.

Practically, there are four important machine operations during flip-chip bonding, which are a) chip picking, b) chip flipping, c) chip-to-substrate alignment and d) bonding as illustrated in Figure 2.16. The operation principle of the flip-chip bonding is described as follows.

Before beginning the flip-chip assembly, small diced chips are placed in a plastic tray, which provides a suitable space dimension for each device as shown in Figure 2.15. The first step is to load this chip tray manually into FC150 chamber and to place a substrate die carefully onto the chuck. The bonding program, which includes the definition of chips, tray and substrate (dimensions and layout), bond temperatures and bond forces can be set and stored in library templates.

Prior to the chip pick up, it is necessary to align a vacuum hole at the end of the pick up tool to the center of a chip. Subsequently, the pick up tool sucks the selected chip from the plastic tray in the face up position (see Figure 2.16, step a). In the next movement, the faced-up chip is flipped and transferred to the arm tool, which pulls the chip from the backside. The arm tool contains a tiny vacuum aperture and has a shape similar to the substrate tool, which is presented in Figure 2.15. Both arm tool and substrate tool need to be chosen in the way that the vacuum-hole dimension fits to the die size.

The next sequence is to align the chip to the substrate before the mounting. Prior to the alignment, the program will ask on which position of the chuck the chip should be placed on. As mentioned above, chuck positions can be set in the library according to the substrate-layout information. After giving the exact position of the chuck, the chuck table will move automatically in XY direction to the defined substrate location.

The alignment procedure starts first with the XY alignment. In order to proceed this lateral alignment, two alignment structures lying diagonally to each other are required on the chip as well as on the substrate. The alignment marks can be inspected through a monitor and a microscope provided at the machine. The coordinates of alignment marks can be adjusted using the joysticks. According to the machine specification, a placement precision of $\pm$ 1μm

can be obtained. The machine provides a pattern recognition system (PRS) in order to recognize alignment patterns and results. After the first alignment mark is recognized, the system will jump automatically to the second feature. The procedure is repeated forth and back between the first and the second marks until both structures obtain a good alignment.

The next step is to level the chip to the substrate (Z-direction alignment) using the optical laser system of the machine. In order to operate this function, three leveling structures, preferable at least one pair placed diagonally to each other, are required. The structures need to be provided on both chip and substrate using smooth metals in order to reach the best optical result. Leveling can be performed either automatically or manually. In the same fashion as the lateral alignment, this is also a repetitive procedure, and will be operated until an excellent value is obtained. After successful leveling, it can happen that the XY alignment needs to be adjusted again.

Finally, the flip-chip bonding can be performed. At this step, the adequate temperature is given to the chip and substrate side. This can be adjusted independently according to the temperature property of chip and substrate materials. The machine offers the maximum temperature of 450 °C. In our experiment, chips and substrates are bonded with temperatures ranging between 320-350 °C on the chuck, and < 250 °C applied to the chip. During the mounting, a suitable force, which is in our case around 1.45 gram/ bump, is applied to the system. Figure 2.17 shows a sample of bonding profile with different chip and substrate temperatures. After the flip-chip bonding is done successfully, arm tool and chuck stage will move back to their home positions, and they are ready to operate the next chips.
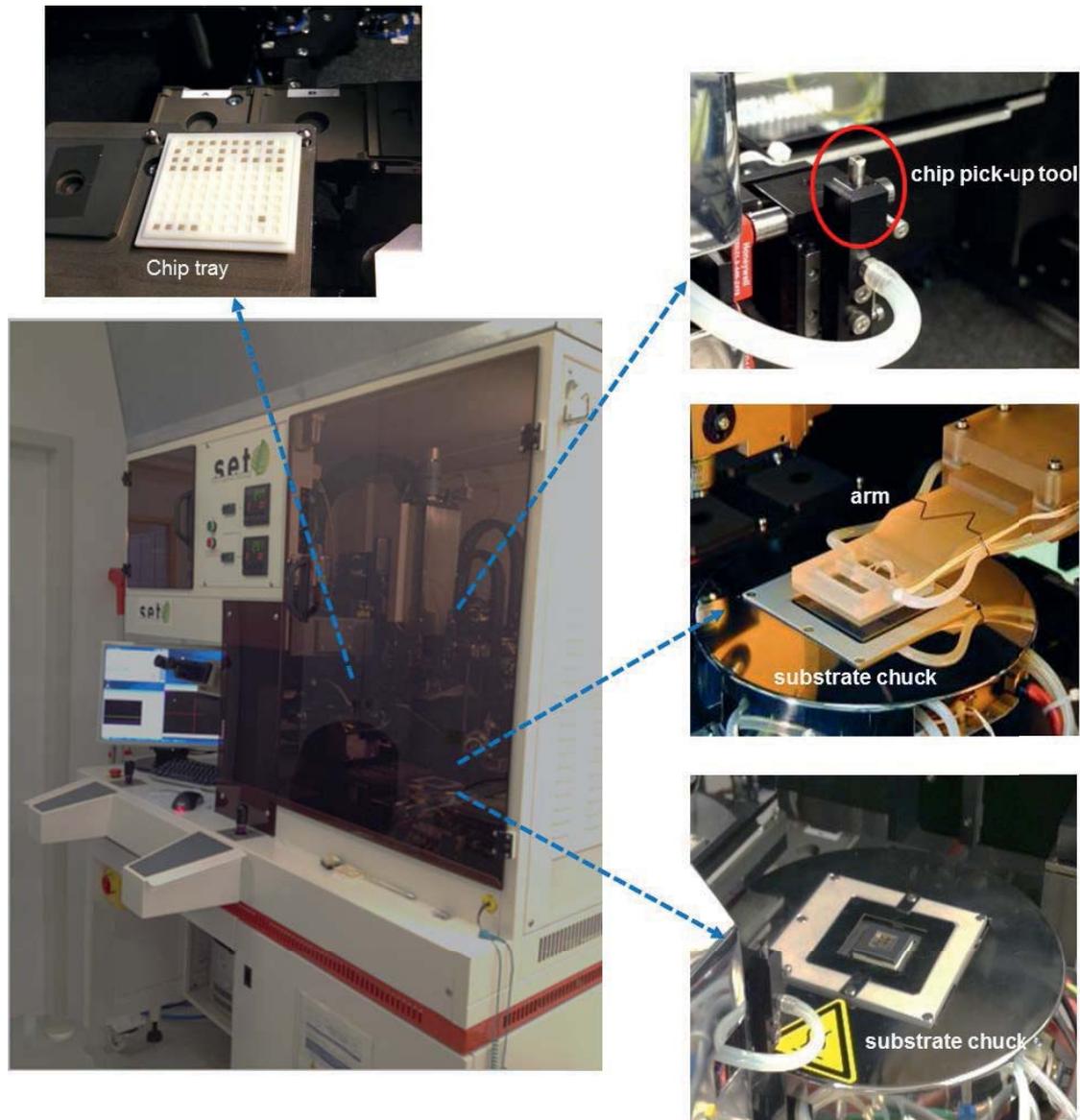
Figure 2.15: FC150 flip-chip bonder and its functional components.
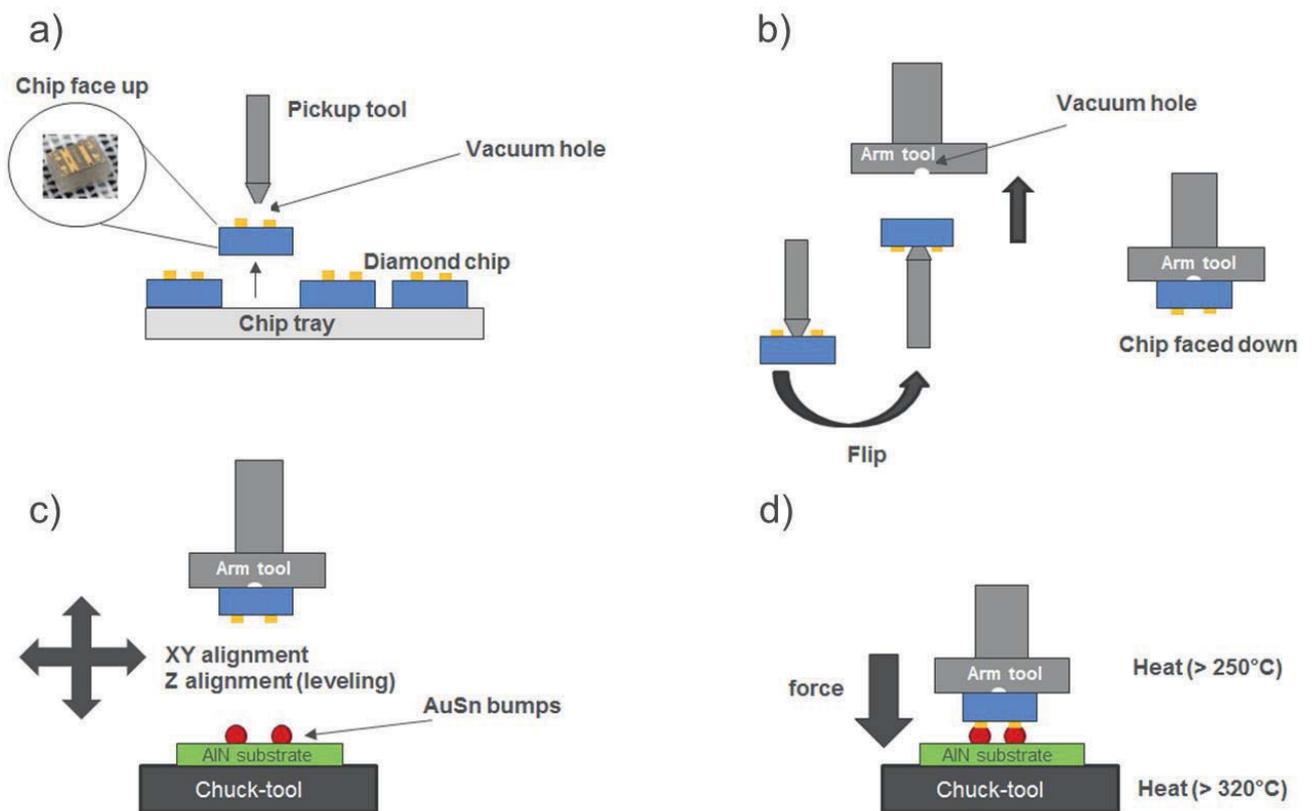
Figure 2.16: Flip-chip bonding steps starting from a) chip pick up, b) chip flipping, c) chip alignment and d) chip bonding.
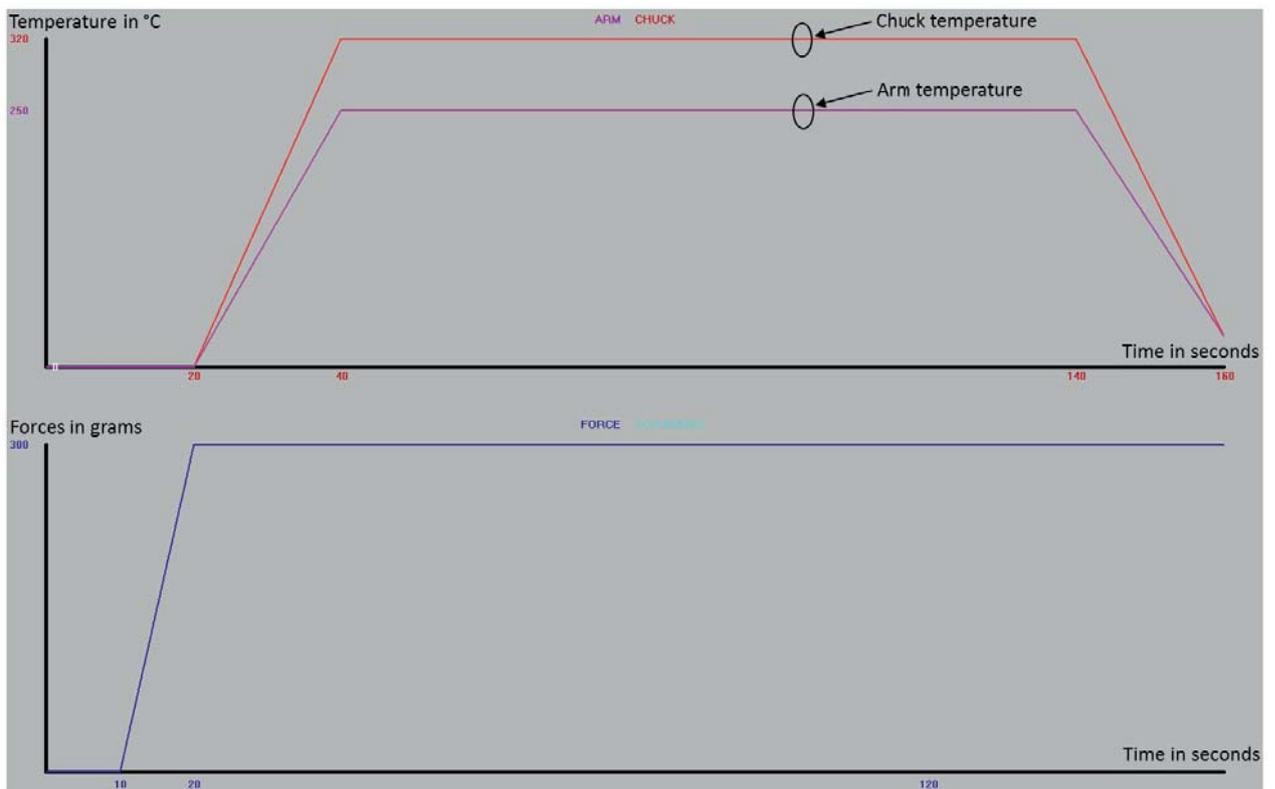
Figure 2.17: Example of flip-chip bonding profile: the bonding temperature can be set individually on chip and substrate.

Chapter 3

AuSn Flip-Chip Interconnections Using CPW Lines

In the past few years, interest in sub-mm wave and sub-THz wave applications has rapidly increased with the availability of semiconductor technologies offering high operating frequencies, such as 250 nm and 130 nm SiGe BiCMOS and 45 nm RF-CMOS. Furthermore, high-end technologies such as InP and GaN HEMT and InP HBT are gaining traction for sub-mm wave power applications as these technologies are maturing. Packaging and interconnection technologies play a major role allowing the system to operate in the high-frequency areas. The flip-chip technology is a promising chip packaging method which can overcome the wire bonding limitation on transition bandwidth, offering a path to connect chips within multi-chip modules, and enabling heterogeneous module integration of different chip technologies.

This chapter presents the development of the first version of sub-mm wave interconnects using the least complicated planar transmission lines, CPW, combined with miniaturized AuSn bumps. As already discussed in several studies shown in the previous chapter, the smaller bump diameter leads to a higher bandwidth [62,63,72]. Therefore the aim of this experiment is also to develop the smallest feasible bump dimensions, which can be realized from the manufacturing standpoint. The design rule for the structure was done for a bandwidth from DC to 220 GHz because radiation losses for this architecture are expected to be severe beyond 220 GHz.
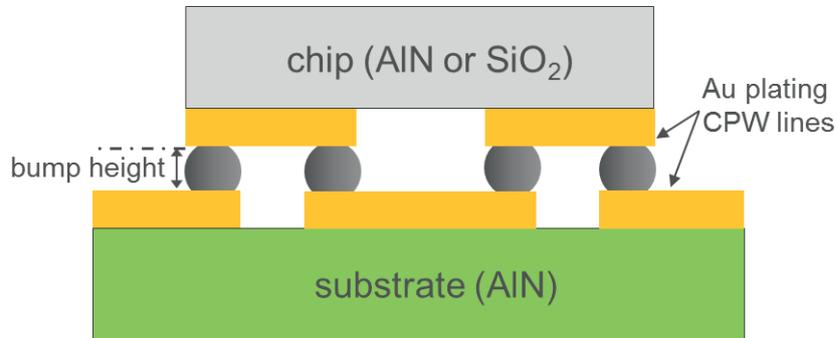
Figure 3.1: Drawing schematic of a basic CPW-CPW flip-chip.

3.1   Concept Design

CPW lines and chip-to-substrate transitions were designed with the 3D EM software CST Microwave Office. The simulation work was done by the group of microwave technology at Ferdinand-Braun-Institute. In this first experiment transparent SiO_2 glass is selected as a chip material in order to inspect the post-bonding lateral alignment of the flip-chip. The materials defined in the simulation are SiO_2 glass chip (borofloat) and AlN carrier substrate. The 3-inch borofloat glass wafers are selected in order to be able to verify the alignment of flip-chip bonding through the transparent glass chip. The structures composed of the 2 mm-long CPW lines with the optimal signal width of 15 µm and 11 µm gap between signal to ground were fabricated by electroplating of 3 µm thick Au on both chip and substrate side. At the end of the CPW lines, landing pads for coplanar on-wafer probing were structured, and the miniaturized AuSn bumps with a diameter of around 10 µm and a bump height of 6 µm are defined. The cross-sectional structure of the experimental model is shown in Figure 3.1.

The simulation takes also the detuning effect [8, 61, 72, 73] into account by investigating the influence of varied bump heights of 0, 5, 10 and 15 µm up to 220 GHz. The results are shown in Figure 3.2. It is clear that the detuning effect dominantly occurs when there is no gap (0 µm) between a chip and a substrate. The three bump heights of 5, 10 and 15 µm give no different in $|S_{21}|$. The insertion loss of these three heights is around 1.4 dB at 220 GHz while the zero bump height results in a $|S_{21}|$ increase of 0.6 dB at the same frequency. The same

behavior is observed for the return loss. A bump height of more than 5 μm yields a $|S_{11}|$ of at least 30 dB at 220 GHz, whereas the zero bump height degrades the $|S_{11}|$ to around 23 dB. It can be concluded from this analysis that the minimum gap between chip and substrate should be at least 5 μm. The taller bump height up to 15 μm does not affect the transition quality. In order to simplify assembly and manufacturing in this study, a target bump height of 6 μm is selected.
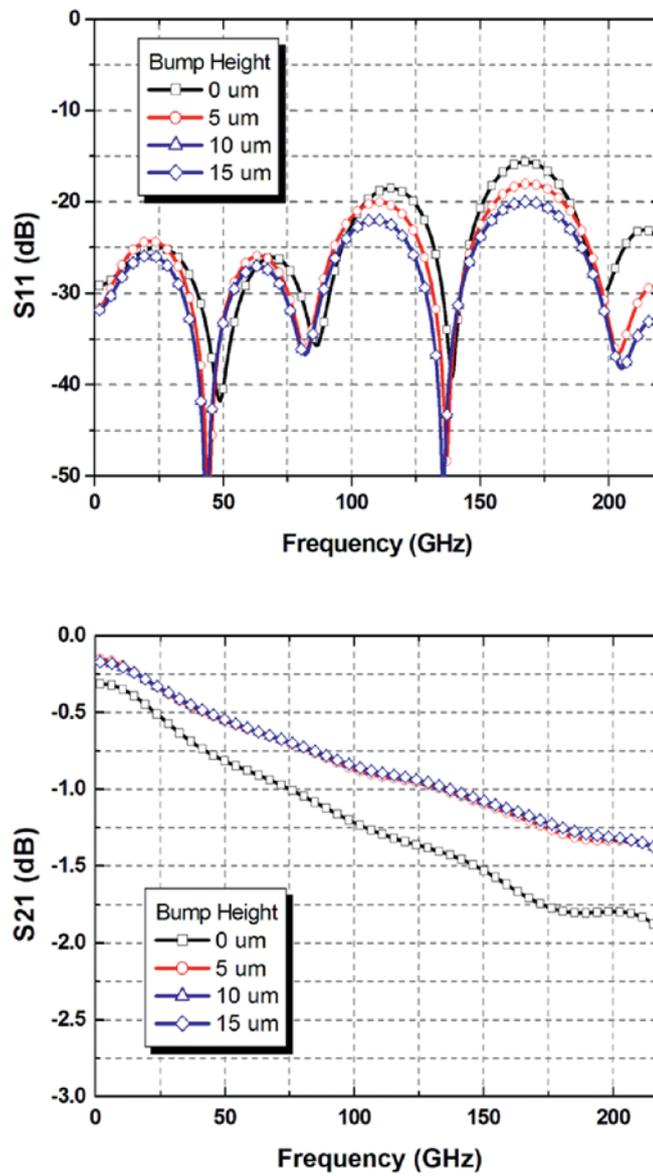
Figure 3.2: *S*-parameter simulations of the influence of bump heights from 0 μm to 15 μm with 5 μm intervals using the simple CPW flip-chip model.

3.2 Fabrication

This section presents the fabrication techniques of miniaturized AuSn bumps in detail. Unlike most of the recently published electroplated AuSn bumps [99, 100], the micro bumps in this work are fabricated by electron beam evaporation [85]. However the bump processing is not limited to any deposition method as long as the necessary critical dimensions can be attained. The microbumps were integrated with Au plating transmission lines, including a barrier to avoid uncontrolled AuSn diffusion. In general, the flip-chip interconnect consists of two main elements: Au-plating transmission lines and pads (either in the form of MS, CPWs or striplines) and AuSn bumps.

3.2.1 Transmission Line Processing

In this dissertation, all of the transmission lines are constructed using gold electroplating. The thickness of the gold plating is between 2 and 3.5 µm depending on the designed layer. Prior to Au plating, a thin seed layer of TiW/Au/TiW is deposited on the wafer to assist the adhesion of the photoresist. The transmission structure is defined by i-line stepper lithography using a 5.5 µm negative photoresist with a straight-sidewall profile. The signal line widths range between 9 and 15 µm according to the transmission line designs. Before the Au plating process, the TiW top seed-layer at the photoresist-opening areas is etched away using SF_6 plasma exposing, the Au layer underneath. The electroplating of Au is performed in two steps, plating with two times half target thickness in order to avoid over deposition. After each plating step, the gold thickness is measured with a profilometer. Note that the gold-plating process increases the pattern width by 0.45 µm on each side. Therefore it is important to shrink the signal width in total 0.9 µm in the layout to guarantee the exact signal width after the electroplating process. Subsequently, the photoresist is removed using an O_2 plasma strip. Finally, the seed layer TiW/Au/TiW in the unwanted area is removed using SF_6 plasma for TiW, degussa dip for Au and H_2O_2 for the last TiW layer. The final thickness of the line structures is again measured with the profilometer, with the Au-plated structures inspected using a scanning electron microscope (SEM).

In Figure 3.3, steps (a)-(f) describe the process flow of CPW transmission lines of the first experiment, which were fabricated by electroplating of 3 µm thick Au on the chip (either

AlN or SiO_2) and on the AlN substrate as shown in the cross-sectional structure in Figure 3.1.
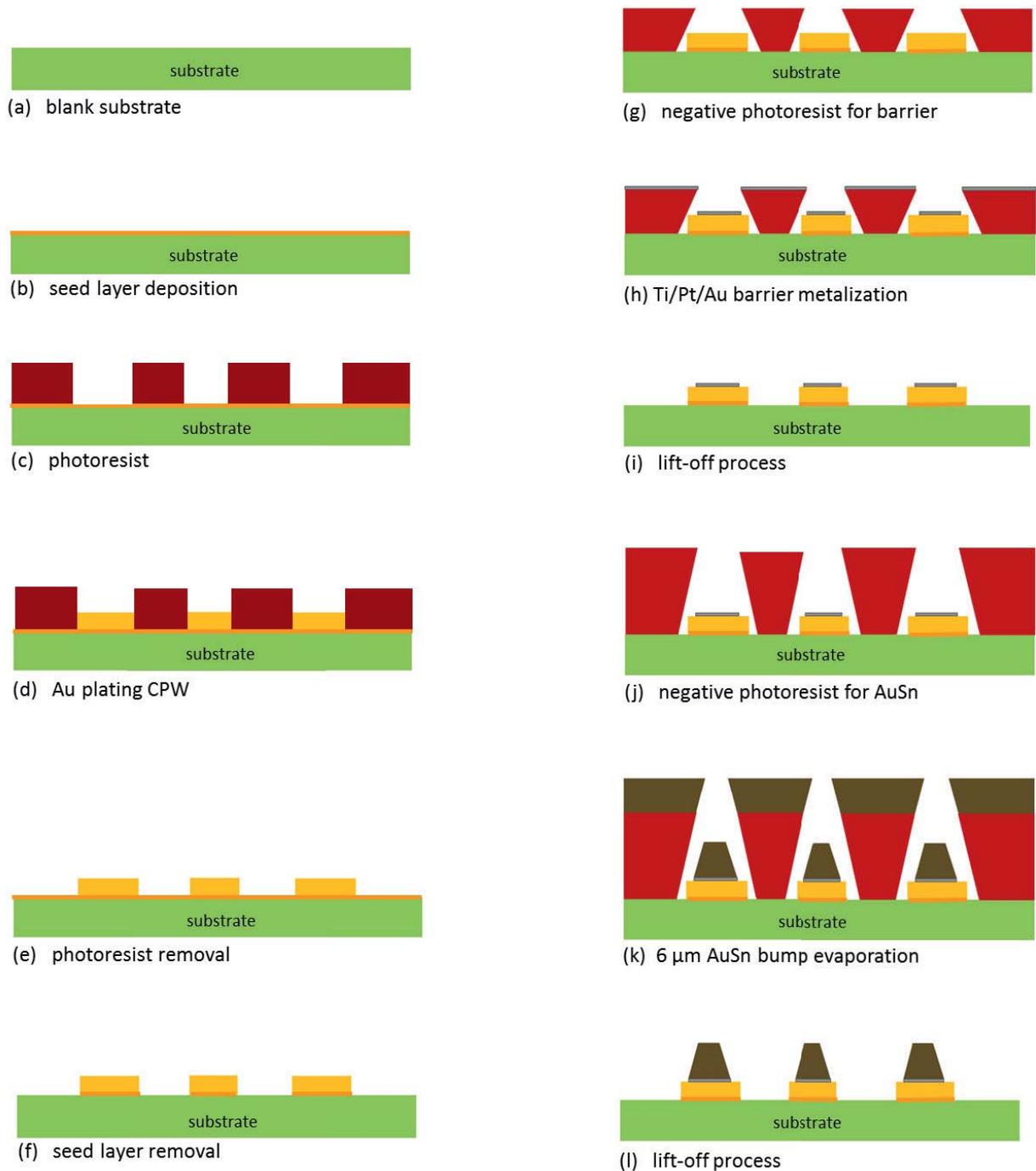
Figure 3.3: Process flow of miniaturized AuSn bumps (lateral dimension < 10 μm) established in FBH.

3.2.2 Fabrication of Miniaturized AuSn Bumps

Figure 3.3 (g)-(l) describes the optimized process steps of AuSn microbumps. The AuSn evaporation is done in the scheme of multilayer evaporation in the same equipment, starting from a thin Ti adhesion layer, converting to the first thin Sn layer, switching to Au layer, repeating the Au/Sn loop, and ending with a gold cap layer to prevent a quick oxidation of Sn material. In total 8 layers of Au/Sn stacking are created. The thickness of each layer is within the range of 450-1200 nm.

In the beginning of this study, AuSn evaporation was processed directly after barrier deposition, using the same photoresist. But this process was not optimized since the diffusion barrier was deposited in a different equipment. As the wafer was taken out of the barrier-deposition chamber, the photoresist quality changed while waiting for the AuSn metallization. This generated difficulties in the subsequent lift-off process. From this outcome, two lithography steps for barrier metallization and AuSn evaporation are then separately provided, followed by their individual lift-off process.

During the first design of experiment (DOE), the fabrication process was evaluated using different bump diameters starting from 4 µm up to 10 µm. The results show that only the lateral dimension of 10 µm assures satisfactory process stability and yield. The smaller bump dimensions limited the opening area of photoresist, and led to missing bump after the bump metallization. The AuSn material is chosen because it provides a stable mechanical connection under a suitable temperature for the later active device. Therefore the eutectic $Au_{80}Sn_{20}$ bumps with a diameter of 10 µm, and a height of 6 µm are selected. Prior to the AuSn evaporation, it is essential to provide thin layers of a Ti/Pt/Au diffusion barrier on the surface of Au plating to avoid the dissolving of Au pillars into Sn, which results in a deviation of AuSn composition [88]. The same photomask can be employed for barrier and AuSn. Subsequently, the round-shaped AuSn microbumps are structured on the top of barrier structures using i-line stepper lithography with an lateral accuracy of ±1 µm.

As mentioned the support Au plating has a thickness of around 3 µm, therefore to evaporate 6 µm AuSn bumps, the negative photoresist of 15 µm with a lift-off profile from Microchemical is selected. The sufficient undercut of the opening photoresist is one of the most important criteria assisting the lift off. Another important factor that strongly affects the outcome of the lift-off process is the adequate ratio of photoresist opening area to the whole wafer.

Since our bump structure is very small (10 μm), and there are only few signal bumps at the end of the CPW lines, several mechanical bumps are required to increase the whole photoresist-opening area on the wafer. These mechanical bumps (or so called filler structures) facilitate the NMP (1-Methyl-2-pyrrolidon) solvent, which is a typical photoresist stripper, to penetrate into the photoresist. As a result, the photoresist can be efficiently removed from the wafer. The microscope image (Figure 3.4) shows the filler structures around the CPW area and the huge undercut obtained from the lithography process (left). The SEM picture of the AuSn photoresist profile is illustrated in this figure (right).
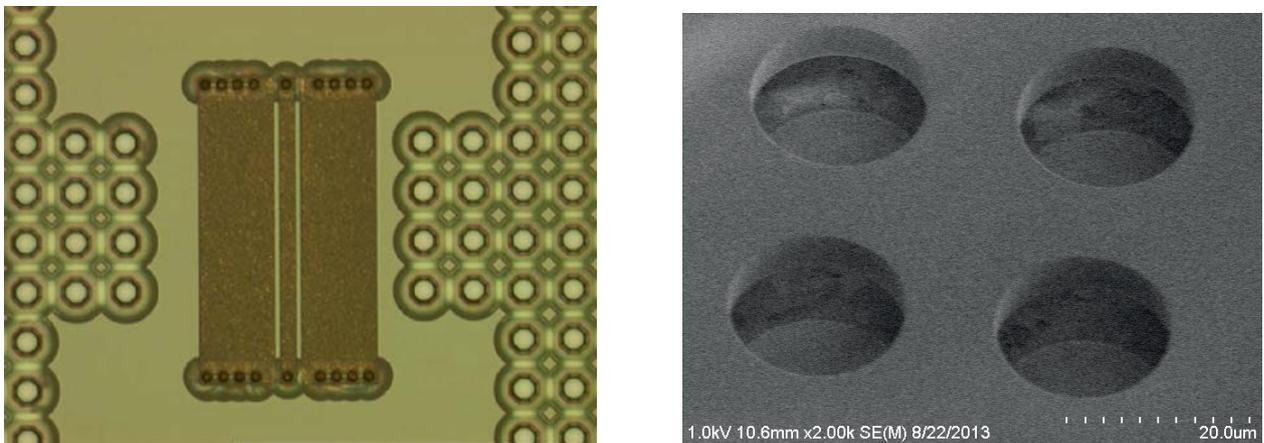
Figure 3.4: Undercut profile of negative photoresist for AuSn bumps.

During evaporation, the temperature inside the evaporation chamber needs to be carefully controlled in order to avoid temperature effects on photoresist which can generate cracks and deform the photoresist. Figure 3.5 shows the evaporated wafer after the cooling system has cooled down the equipment to a temperature of -18 °C. As indicated by the cracks in the photoresist all over the wafer this temperature is too low. Process optimization finally resulted in a suitable evaporation temperature in between 25 °C and 50 °C. The optimized lift-off process is done by soaking the wafer for at least 120 min using low pressure (100 psi) in order to avoid the microbumps being removed by excessive pressure.
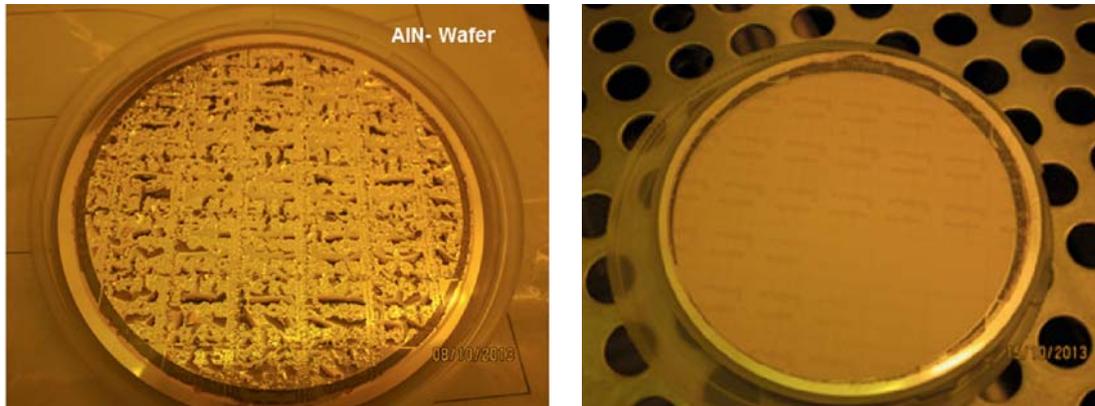
Figure 3.5: Wafers after AuSn evaporation: a wafer with photoresist cracks due to the extremely low chamber temperature (-18 °C) during evaporation (left) and a wafer with the controlled evaporated temperature in between 25 °C and 50 °C: no photoresist cracks found (right).

Figure 3.6 shows that the multilayer AuSn stacks, directly after evaporation, are in the form of a truncated cone. Several AuSn compositions (AuSn, AuSn$_4$, AuSn$_2$) occur after the evaporation. Applying a reflow temperature of around 320 °C, the AuSn bumps are molten and reveal a round shape. At this point, the AuSn zeta phase (Au$_5$Sn) will be generated leading to the eutectic composition of 80% wt. Au and 20% wt. Sn, as shown in Figure 3.7.
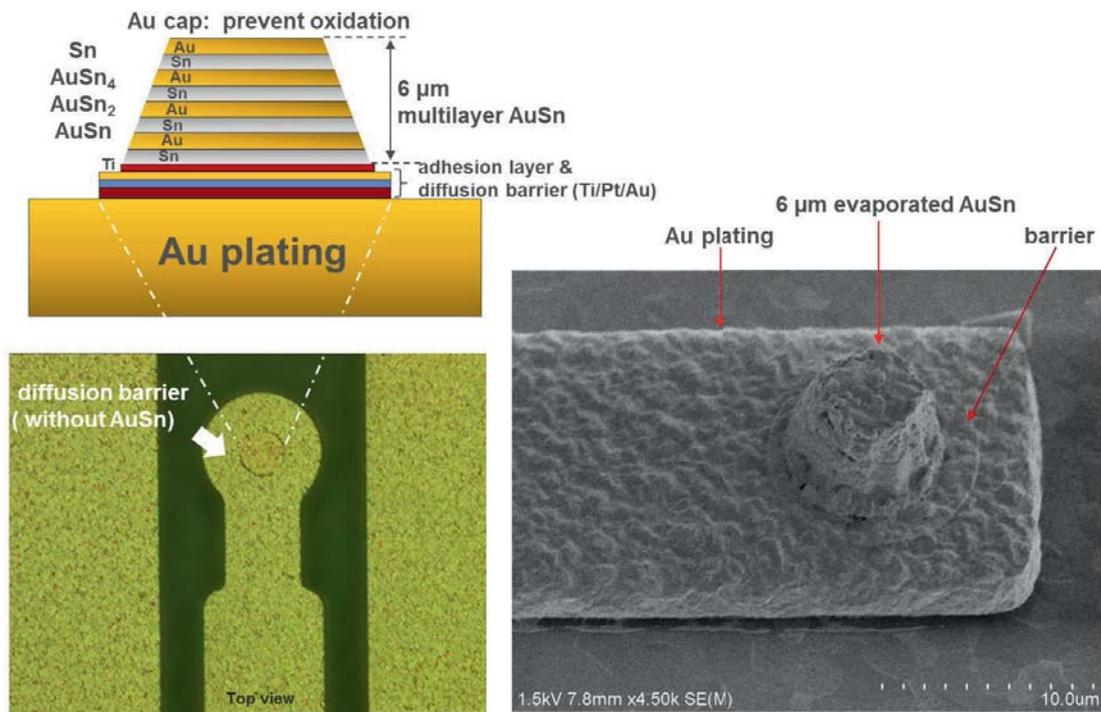
Figure 3.6: Multilayer AuSn bumps after evaporation. Illustration of the stack layer on gold plating including diffusion barrier (left) and a SEM image after lift-off (right).
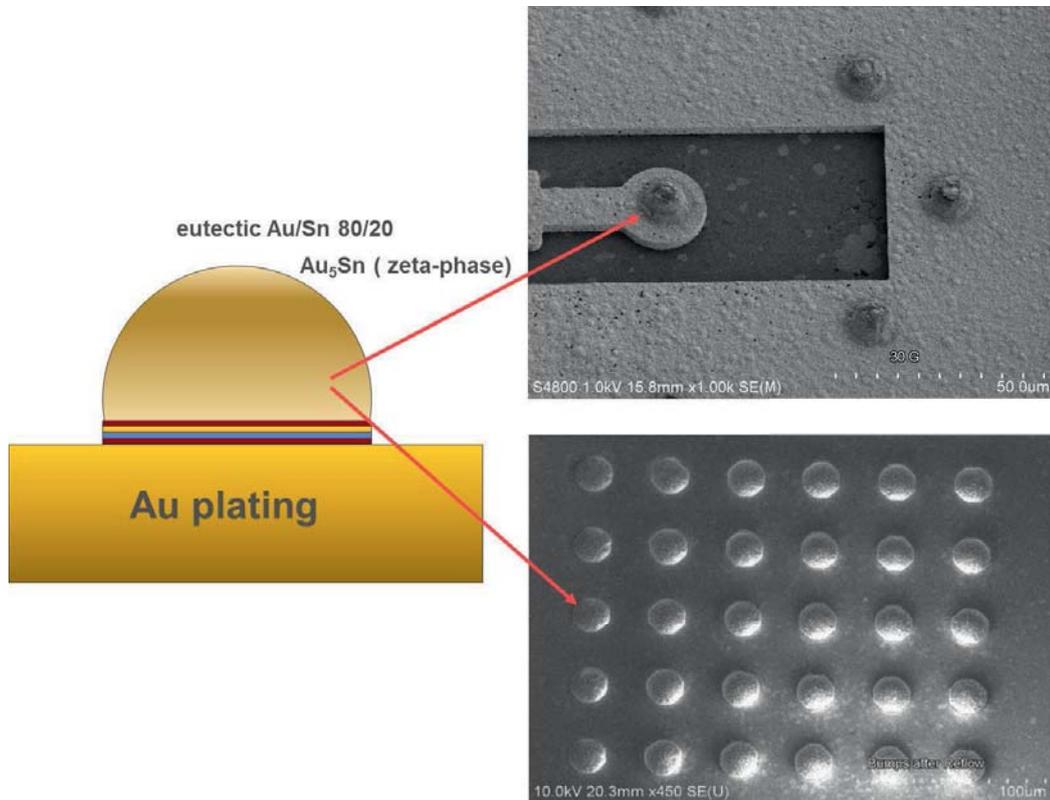
Figure 3.7: The ball shape of AuSn bumps after passing reflow temperature > 320 ˚C.

3.2.3 Flip-Chip Mounting

In the end, both chip (quartz and AlN) and substrate (AlN) wafers are diced with a conventional diamond-dicing blade. For the CPW-CPW flip-chip, chip and substrate sizes were defined as 2×2 mm^2 and 10×10 mm^2, respectively. The chip was mounted on the substrate carrier using the FC150 bonder. To obtain a good ohmic contact after flip-chip bonding, it is necessary to remove the Sn oxide on the bump surface before starting the flip-chip assembly process. The samples are dipped in a dilute hydrochloric acid (HCl:H$_2$O 1:1) solution for 10 seconds. The flip-chip alignment and bonding was performed using FC150 commercial flip-chip bonder as described in section 2.4.4. During the bonding process, the temperature of the chuck substrate was set to 350 ˚C. The bonding was done under a formic gas, i.e. 95% N$_2$ and 5% H$_2$ environment. The first sample glass flip-chip is demonstrated in Figure 3.8.
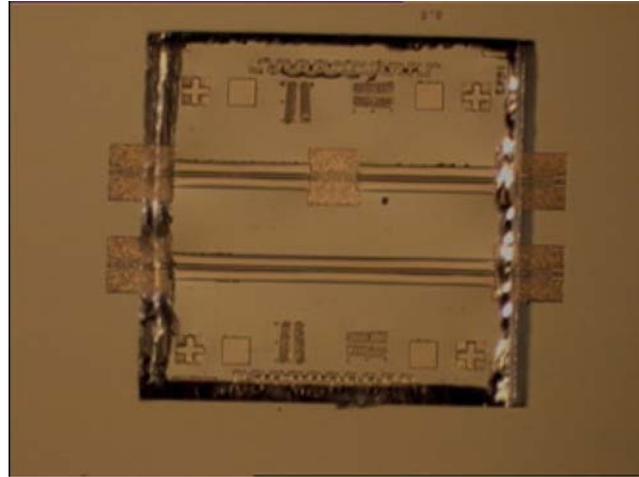
Figure 3.8: Demonstration of a quartz flip-chip.

From the transparent flipped chip, the lateral accuracy of the mounting using FC150 is observed to be less than 2 μm as depicted in Figure 3.9. On the left side, the top view of CPW-to-CPW connections of glass chips on AlN carriers are shown, whereas on the right side the DC chain structures are demonstrated. The images of the interconnects were taken through the glass chips using a microscope. Within the frame of this experiment, the bond forces are also tested. The glass chips are bonded using three different bond forces: 100, 200 and 300 grams. Figure 3.9 also presents the mounting results of these bond forces. With the total pressing force of 100 grams, almost no AuSn material is spread out of the interconnect area. But with more than 200 grams, the out-spreading solder material can be clearly seen. The electrical test of these three chips confirms the optical outcome. With the 100-gram force, no current flows through the connection path. Only pressing the chips with more than 200 grams yielded the good electrical contact.
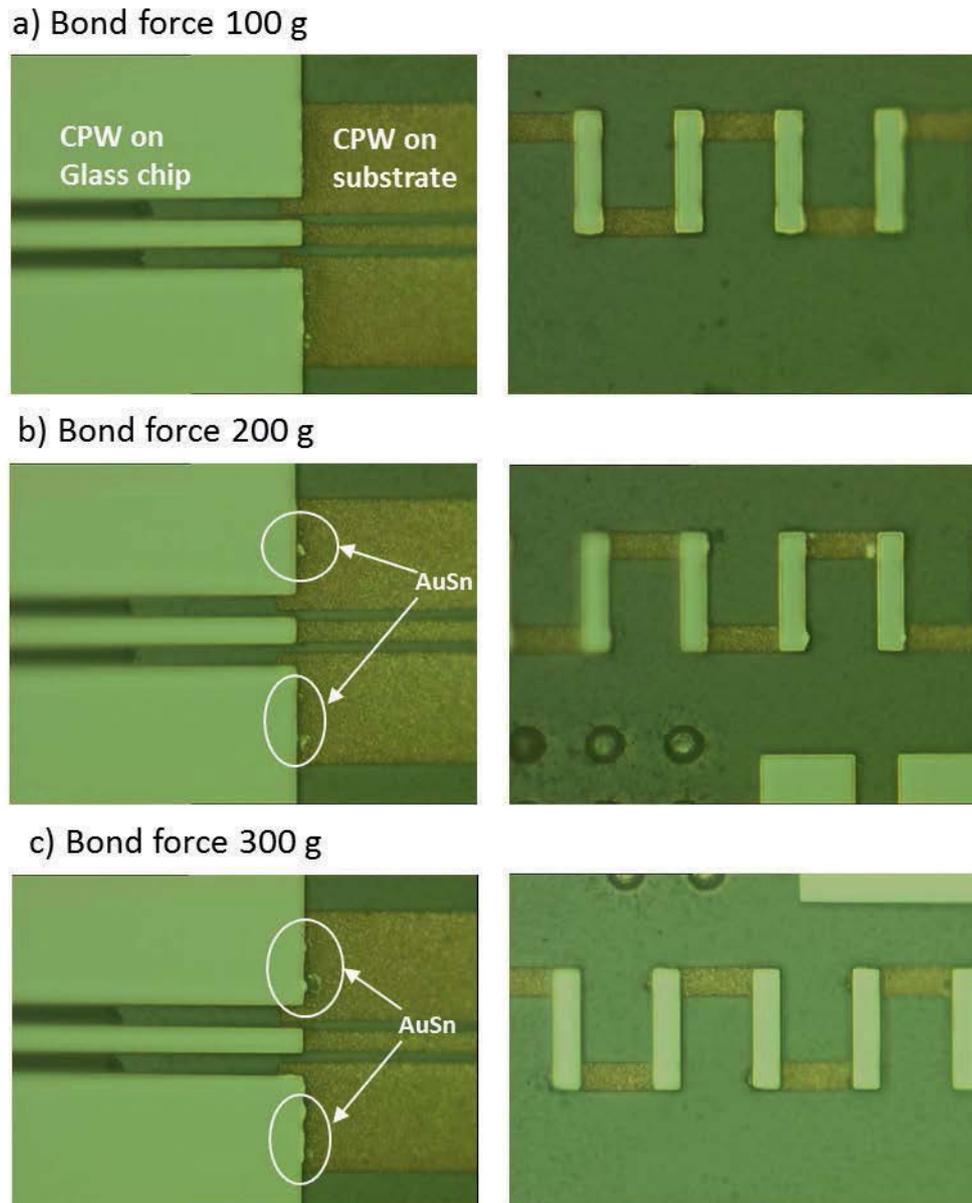
Figure 3.9: Optical inspection of flip-chip mounting through glass chip. Different bonding forces are applied; 100 g (top), 200 g (middle) and 300 g (bottom). The bonding structures indicate a good alignment of < 2 μm.

After verifying a good lateral alignment from the transparent glass chip, the AlN chip is also provided. The flip-chip was performed again, mounting an AlN chip on an AlN substrate. Maximum 9 different chips can be bonded on the substrate for the given layout. Figure 3.10 demonstrates the photographs of a diced AlN chip (left) and a flip-chip mounting of an AlN chip on AlN substrate.
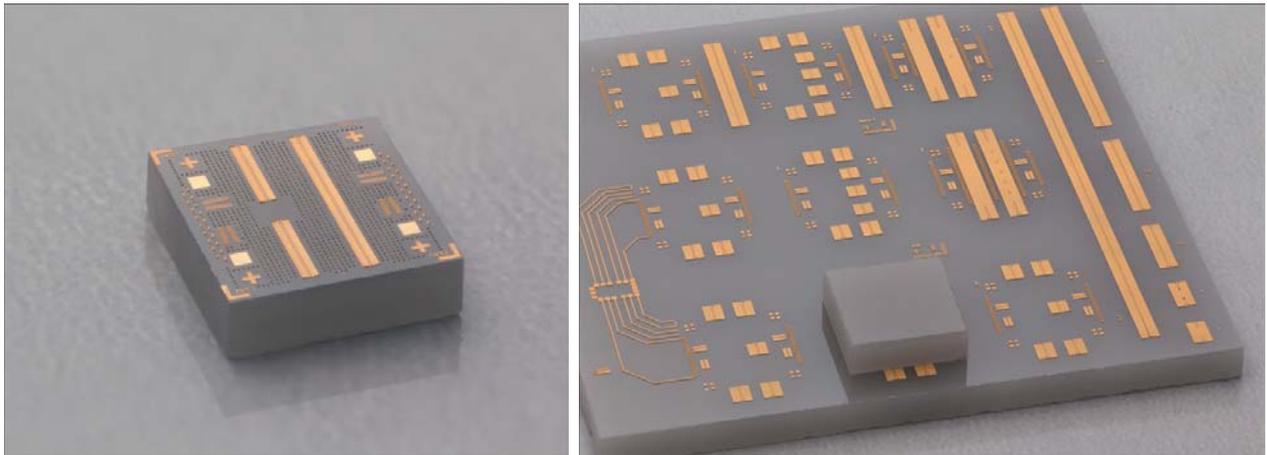
Figure 3.10: Photograph of a successfully fabricated AlN chip (left) and a flip-chip of 2×2 mm^2 AlN chip on 10×10 mm^2 AlN substrate (right).

3.3   Measurement Results and Discussion

The characterization was done on two mounted AlN chips on an AlN submount. Each chip contains two different CPW structures (two transitions and four transitions) as can be seen in Figure 3.10 (left). The on-wafer scattering parameter measurements were carried out up to 220 GHz on the two transition CPWs, using an Agilent PNA vector-network analyzer (VNA) and a Rohde & Schwarz® ZVA67 vector network analyzer (VNA). The system was calibrated using the on-wafer multi-line Thru-Reflect-Line (mTRL) method [101].

Figure 3.11 shows the measurement results of the structure with two back-to-back flip-chip interconnects up to 220 GHz. The CPW-to-CPW structures have a total length of 2.45 mm, which includes a thru-line of 1.70 mm on the chip side. The measured small-signal

transmission curves show a loss which is gradually increasing with frequency. At 220 GHz a total insertion loss between 2.5 and 2.75 dB and a return loss of greater than 13 dB of these two transition structures are observed. Most of the losses can be attributed to line loss of the structures. By excluding the CPW line loss, the insertion loss remains only around less than 1.0 dB per transition. The dielectric constant value of the AlN is adjusted in the simulation model because in reality the AlN substrate material changes due to the wafer processing such as a strong wet chemical etching or a long period of plasma etching. The conductivity value of gold used in this simulation is 4 x 10^7 S/m, which is the value that already considers the gold roughness from the processing (typically 3 x 10^7 S/m). With this model, the measurements have a good agreement with simulation and the two chips give similar output.
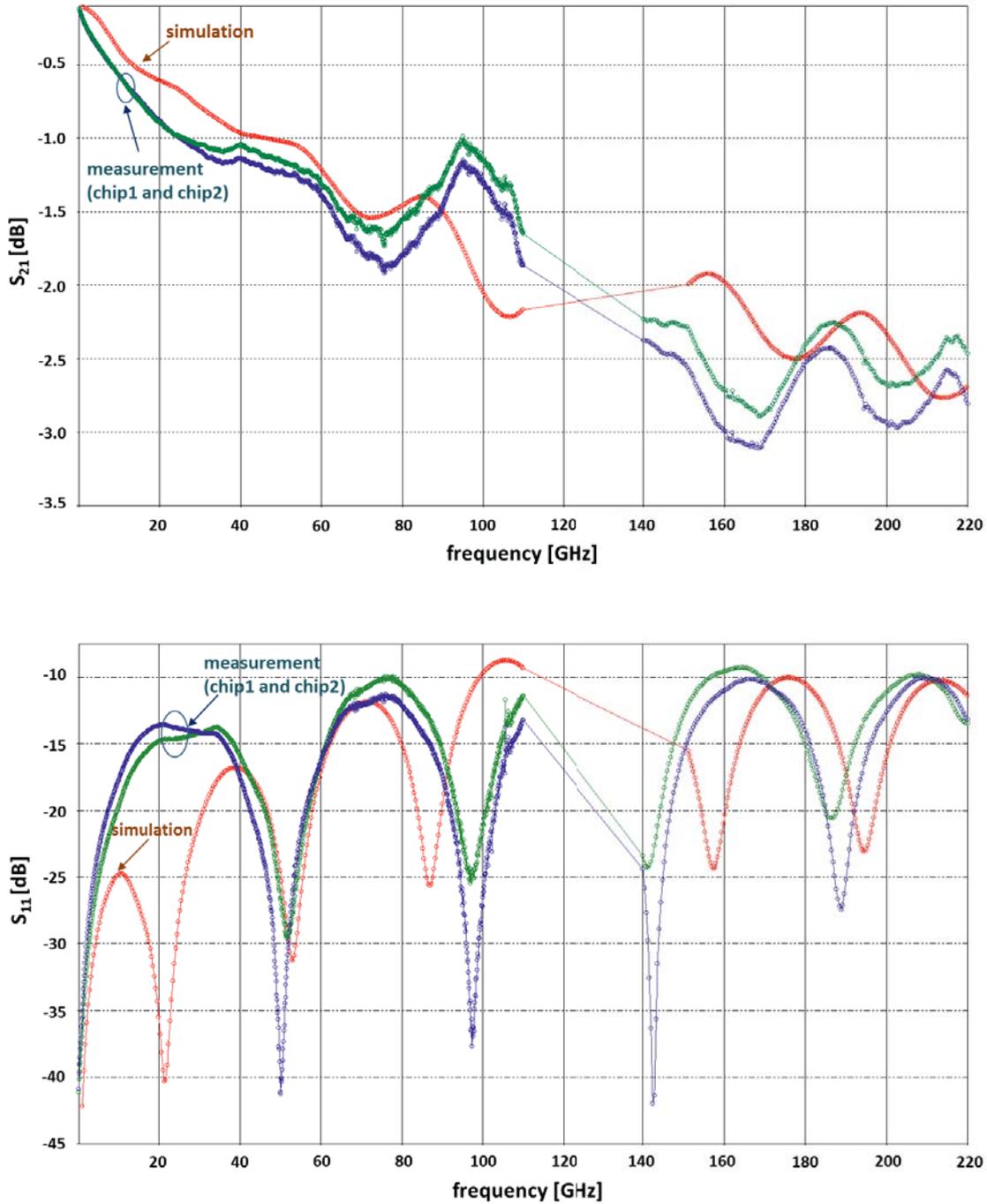
Figure 3.11: The measured back-to-back structure of AlN chip as a function of frequency up to 220 GHz compared to simulation results: the insertion loss S_{21} (top) and return loss S_{11} (bottom).

Comparing to the simulation, there are two factors which can be reasons for the deviation of the measurement results. These parameters are from the influence of fabrication process, which are:

1) The over deposition of the gold plating, which exceeds the top of the photoresist. From the first prototype it is observed after the gold electroplating that the gold deposition grew over the photoresist, however, no short circuiting between structures occurred. Nevertheless, this results in the deformation of the CPW structures as depicted in the SEM image in Figure 3.12. As a result, the transmission line width changes by 3.5 μm each side, and therefore the characteristic impedance (Z_0) changes from 50 ohm to around 42 ohm, resulting in the deviation in S-parameter measurements.
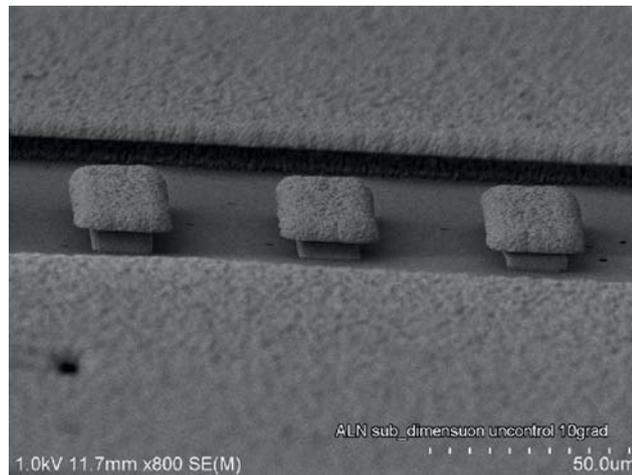
Figure 3.12: SEM images of fabricated CPW with over-deposition of Au plating, which can affect the S-parameters.

It was also observed that generally the electroplating process enhances the structure dimension of 0.45 μm each side. Therefore, during the layout design, the structure dimension needs to be shrunk in order to obtain the exact design dimension after processing. This finding was implemented into the next design which is presented in Figure 4.3.

2) As mentioned previously, some process steps such as a strong wet chemical etching and a long period of plasma etching exert an influence on the AlN substrate material. This could lead to a) the thinning of AlN material or b) making the substrate to be more porous, which

can lead to the deviation in dielectric constant values of AlN, and therefore, reflect to the scattering parameters. However, this problem can be prevented by providing a thin layer of dielectric film such as SiN_x or BCB layer directly at the first step on the AlN surface in order to protect the AlN material. This method has been implemented in all the further experiments in chapter 4 to chapter 6.

Chapter 4

Stripline-to-CPW Flip-Chip Interconnects

While circuit development advances at a rapid pace, the corresponding packaging approaches still need to be developed since most of today's interconnect technologies do not work properly at the mm-wave bands from 110 to 325 GHz. This section presents the development of flip-chip interconnects for the frequency band > 250 GHz. In order to provide such high-frequency interconnects, a stripline, which is an excellent shielding planar transmission line system, is selected for the design on the chip side. The CPW submount and the flip-chip interconnects, using miniaturized AuSn flip-chip bumps, which have been developed in chapter 3, are adapted into this experiment, forming a stripline-to-coplanar (CPW) chip-to-chip interconnect.

Specially, a diamond heat-spreading layer is integrated to the chip construction. The diamond is used because of its very high thermal conductivity [102], which facilitates heat sinking of active devices [9,103]. However, the influence on the flip-chip module performance is minor, i.e., the results presented in the following could be obtained also for a standard chip without the diamond layer. The chapter is divided into four sections. In the first section, the design concept of the transition is described. In the second part, details of chip and substrate fabrication as well as flip-chip mounting are revealed. The measurement results are compared to the simulation output in part three. In the final part of the chapter, the effect of process tolerances to the interconnect quality is discussed.

<center>59</center>

4.1   Flip-Chip Structure Design
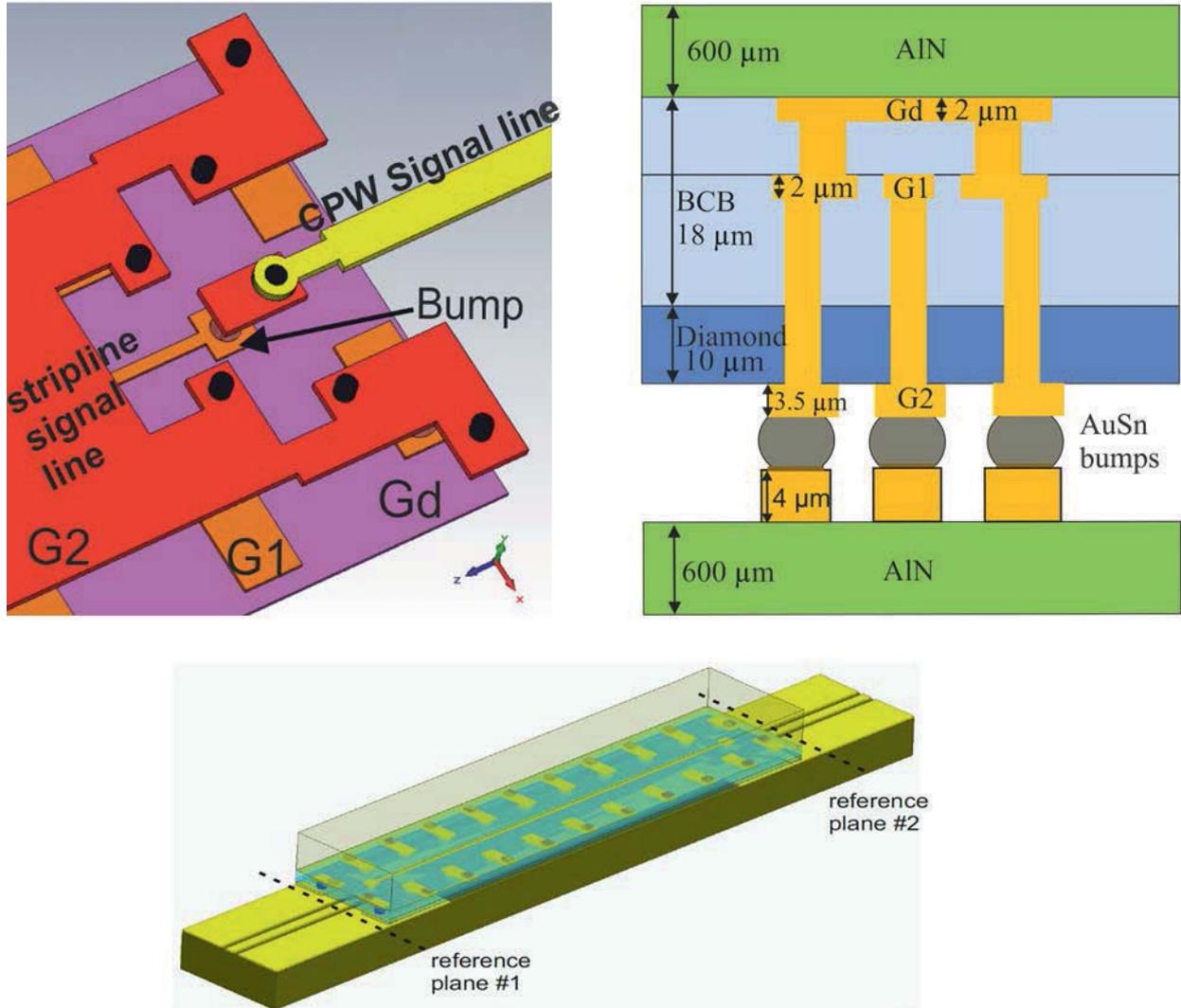
Figure 4.1: Design structures of stripline-to-CPW flip-chip.

The line system and the interconnect were designed using the full-wave 3-D electromagnetic (EM) wave simulator CST Microwave Studio under the condition that geometry and properties of the dielectric layer stack of the chip are fixed since they are determined by the chip

process. The layer system consists of three metal layers (Gd, G1, and G2) with 6 μm and 12 μm thick BCB between Gd-G1 and G1-G2, respectively (see Figure 4.1 (top right)). Since open line structures such as micro strip (MS) and coplanar waveguide (CPW) are susceptible to radiation losses at high frequencies, a shielded line system was adopted on the chip. A stripline using G1 as the signal line and G2 and Gd as upper and lower ground, respectively, is considered. The upper shield (G2 in Figure 4.1) is comparatively far from the signal line due to the dielectric thickness and, therefore, the distance between Gd and G1 is more significant for characteristic impedance. A signal line width of 9 μm is chosen. The shielding vias at the side form a fence and ground-connect Gd and G2. Due to fabrication issues, the vias cannot be stacked vertically but with a horizontal offset instead. This is also the case for any other via (e.g., the signal via inside the transition).

Simulations show an insertion loss below 1.2 dB and a return loss beyond 10 dB up to 250 GHz, which are quite acceptable values. The transition connects the stripline inside the chip to the CPW on the substrate as shown in Figure 4.1 (top left). It consists of a central signal via plus bump, surrounded by vias and bumps for the ground. The ground bumps and vias form a via fence to reduce radiation. Thus, as much shielding as possible is realized on the chip side. The transition was optimized by repeated 3D EM simulation runs. The positions of the flip-chip bumps and vias, as well as the pattern of the metallization in Gd, G1, G2 and G-substrate have been optimized carefully to achieve a good RF performance (low radiation and low reflection) which becomes critical at sub-mm-wave frequencies. The design takes into consideration all hardware constraints including process technology (gaps and tolerances), packaging (flip-chip tolerances) and probing (probe tip pitches).

The CPW on the substrate suffers from radiation losses in the higher frequency range, which, however, was acceptable for the investigation described here. In the following chapter, the CPW on the substrate will be replaced by a (shielded) stripline. An additional advantage of the stripline is that it ensures single mode propagation with negligible radiation and crosstalk effects. The module fabrication process can be divided into three parts: chip fabrication, substrate fabrication, and flip-chip assembly. The details are described as follows.

4.2 Process Technology

4.2.1 Chip Fabrication
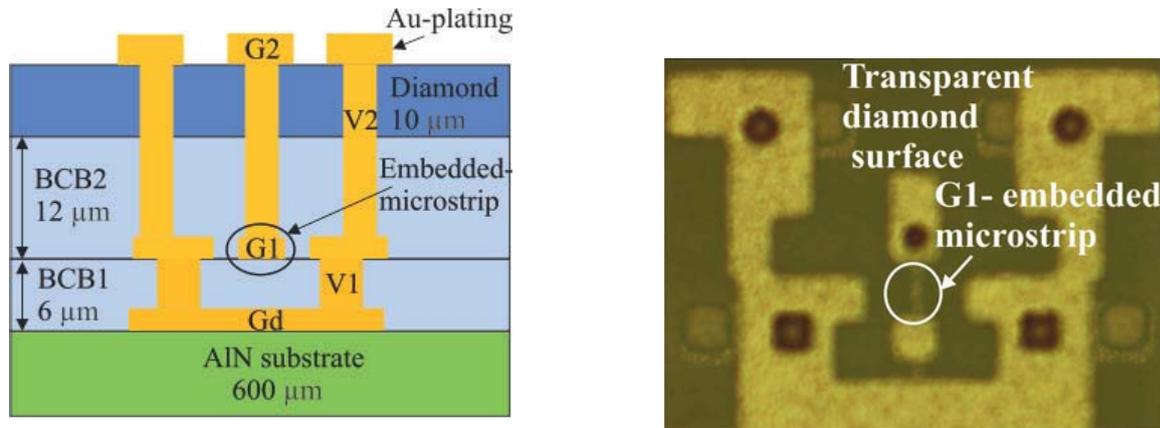
Figure 4.2: Cross-sectional stripline diamond chip (left) and a top-viewed microscopic photograph of the embedded MS under transparent diamond layer.

Figure 4.2 shows the cross-sectional structure of the chip. The stripline (G1) is embedded within the benzocyclobutene (BCB), which is a widely used low-k dielectric material (dielectric constant = 2.65) for mm-wave applications as reported in several studies [18, 104, 105]. Two layers of vertical vias are available for the layer stack of the chip: first, V1 with the depth of 6 μm from the G1 layer to the Gd layer, and second, V2 with a depth of approximately 12 μm from the diamond surface to the G1 layer. Both of them are patterned separately by i-line stepper lithography using a negative photoresist. BCB via openings are done by anisotropic reactive ion etching (RIE) using SF_6 plasma.

All of the metal interconnects are fabricated by Au electroplating in a cyanide-based plating bath as already described in chapter 3, section 3.2.1. But for the interconnects in vias, pulse-plating is chosen because it results in better plating uniformity in vias as compared to the DC electroplating method [106–109]. The signal stripline is deposited and the V1 vias are filled in the same G1 lithography and electroplating step. The most critical dimension in this process step is the MS signal width, which was designed to be 9 μm. To obtain signal line width precisely, the layout is shrunk by 0.45 μm to values lower than the actual ones, in

order to compensate for the structure expansion during the Au-plating process. Figure 4.3 illustrates SEM images of G1 (MS) dimensions after gold plating. The fabricated structure dimensions of transition width (position 1) and MS width (position 2) are around 5.9 µm and 9 µm, which is very close to the design values of 6 µm and 9 µm, respectively.
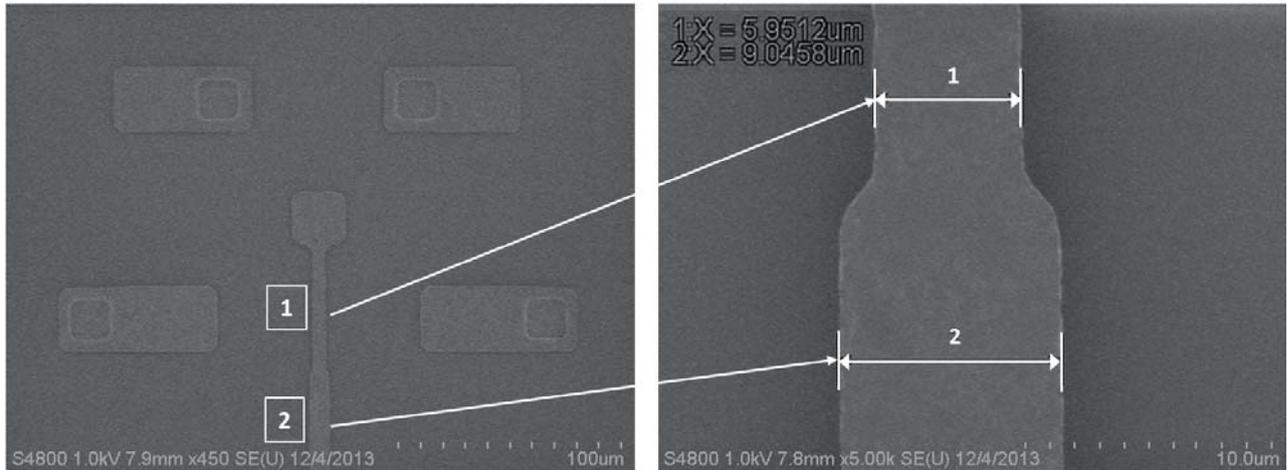
Figure 4.3: Stripline dimensions after gold plating. The target values of structure width at the transition area (position 1) is 6 µm, and the designed stripline width (position 2) is 9 µm. By shrinking the layout dimensions of 0.45 µm on each side, the fabricated features are highly accurate comparing to the design .

After the G1 layer is fabricated, the patterned AlN wafer is bonded to a diamond-on-Silicon wafer (either chemical vapor deposition (CVD) [110, 111] or ultra nano crystalline (UNCD) [112] diamond), using BCB as a bonding medium. Subsequently, the Si substrate supporting the diamond film is removed by mechanical lapping using SiC grains, followed by wet chemical etching in 30% KOH at 95 °C before patterning of V2 and the G2 contact. The Si etch rate in fresh KOH solution is around 2-2.5 µm per minute. After lapping, the remaining Si thickness is around 50-70 µm leading to an etching time of 30-50 minutes. It is important to keep the KOH etching time less than one hour because after this time the KOH solution will start penetrating through the edge of the wafer causing delamination.

Wafer	Diamond type	Diamond thickness	Diamond thickness after V2 etching
1	UNCD	10.95	9.09
2	UNCD	10.26	8.88
3	CVD	8.0-13.3	10.18

Table 4.1: Diamond thickness before and after V2 complete etched (using diamond as a hard mask for BCB etching)
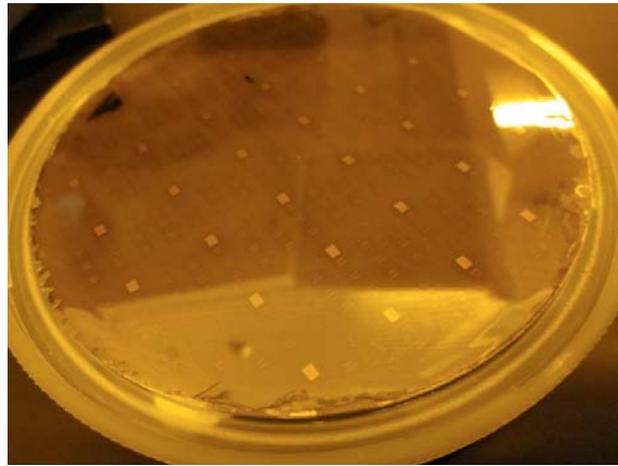
Figure 4.4: Bonded diamond-AlN wafer after KOH etching of remaining Si substrate. The delamination starts appearing at the wafer edge when the etching time increased. .

When the silicon is cleanly removed, the stripline underneath the diamond/ BCB stack can be assessed in an optical microscope due to the transparency of the diamond layer, as is illustrated in Figure 4.2 (right).

Subsequently, the diamond vias (V2) are etched using RIE O_2 plasma. During the 10-μm diamond etching, 500 nm SiN_x is utilized as a hard mask to protect the unetched area of the diamond surface. However, in order to further etch the approximately 12 μm thick BCB layer, the diamond itself functions as an etch mask. Because the diamond can also be etched by SF_6 plasma, at the end of this process around 1-2 μm of diamond is also thinned away. Table 4.1 summarizes the three different diamond wafers with their original thickness and their end thickness after V2 etching using diamond as an etch mask for BCB.

To ensure exposure of the underlying metal layer, the depth of via etching was measured with a profilometer, and the exposed surface was examined in a Scanning Electron Microscope (SEM). Figure 4.5 illustrates SEM pictures of V2 diamond etching (left) and BCB etching (right). In this design, the via diameters for both V1 and V2 are 20 μm.
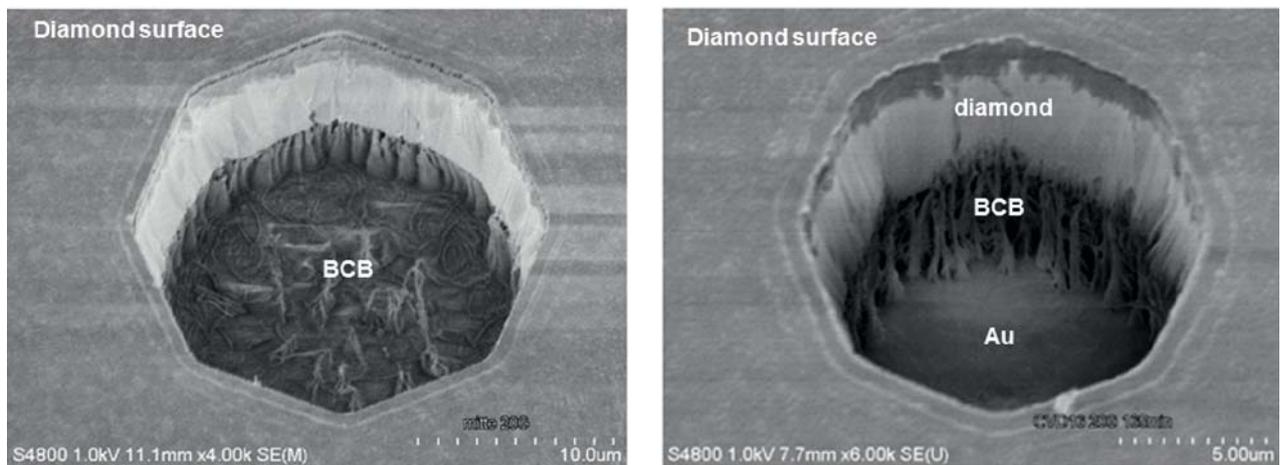
Figure 4.5: V2 diamond via etching: etching of 10-μm diamond surface until BCB surface (left) and a SEM image of continuing BCB etching until gold surface exposed (right).

The detailed process steps of the AlN chips are illustrated in the following.

(1) substrate – **AlN wafer start**
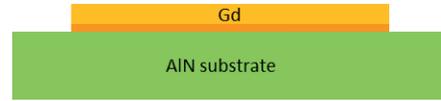
AlN substrate

(2) Gd: Plating base TiW/Au/TiW

AlN substrate

(3) Gd: Lithography for GD Au-plating

AlN substrate

(4) Gd: Au plating

Gd

AlN substrate

(5) Gd: PR removal

Gd

AlN substrate

(6) Gd: Plating base removal

Gd

AlN substrate

(7) SiNx adhesion layer for BCB

Gd

AlN substrate
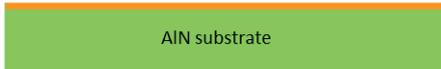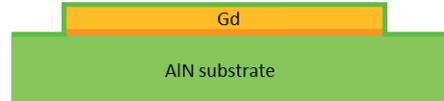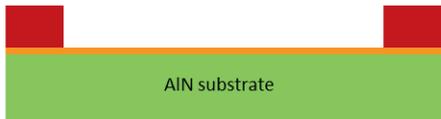
(8) First layer BCB (BCB1)

BCB1

Gd

AlN substrate
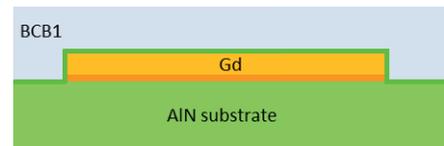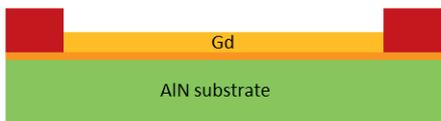
(9) V1: Lithography for BCB-via etching

BCB1

Gd

AlN substrate
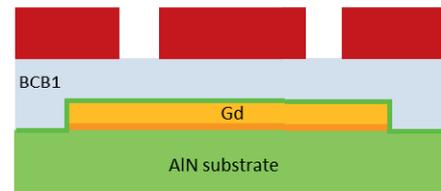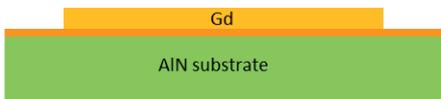
(10) V1: BCB-via etching to Gd layer (SF$_6$ plasma)

BCB1   V1

Gd

AlN substrate
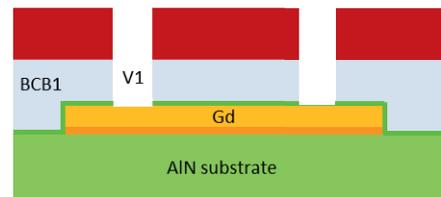
(11) V1: photoresist removal
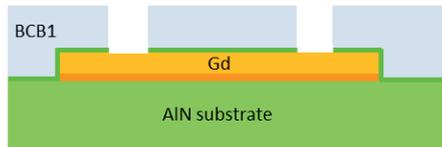
(16) G1: plating base removal
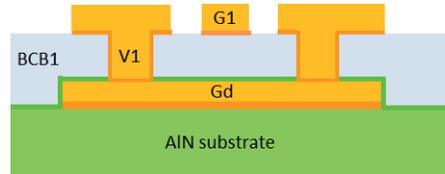
(12) G1: plating base TiW/Au/TiW
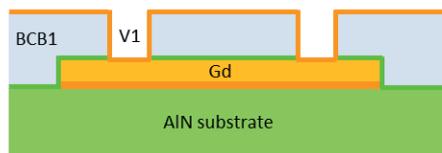
(17) SiNx adhesion layer for BCB2 layer
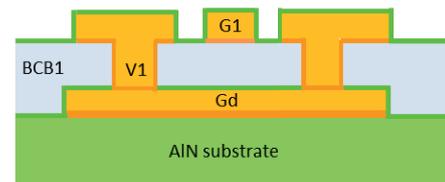
(13) G1: photoresist for Au plating
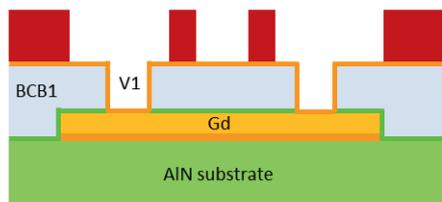
(18) planarization and bond BCB (BCB2)
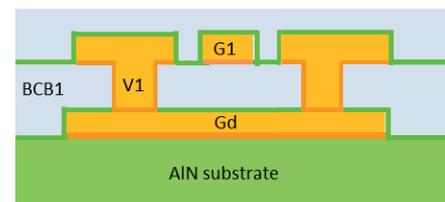
Continue with diamond wafer

(14) G1: Au electroplating G1
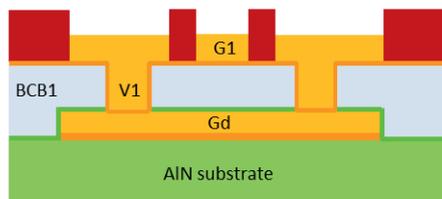
(15) G1: photoresist removal
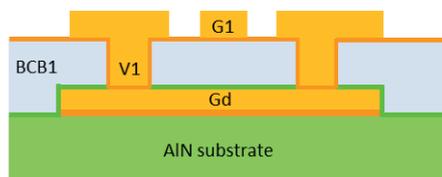
(19) diamond-on-silicon **wafer start**

(20) SiNx adhesion layer

(21) planarization and bond BCB (BCB2)

(22) Wafer bonding: diamond wafer and AlN wafer
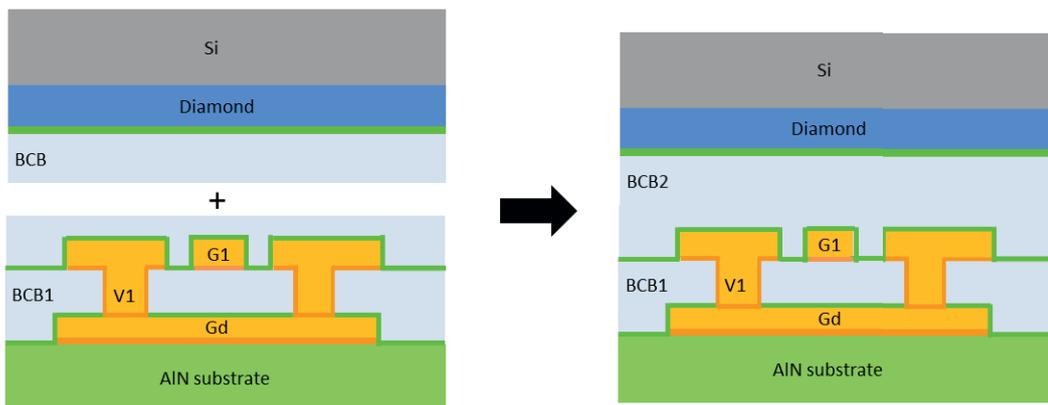
(23) silicon substrate removal (lapping and KOH etching)

(24) V2: SiNx hard mask for diamond etching

(25) V2: photo lithography

(26) V2: SiNx hard mask etching (SF$_6$ plasma)
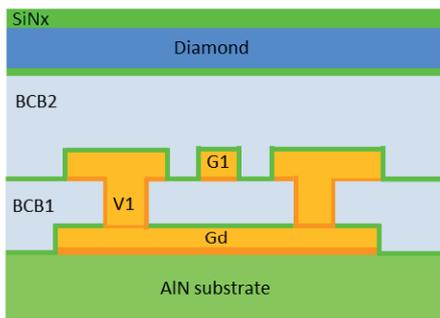
(27) V2: diamond etching (O$_2$ plasma)
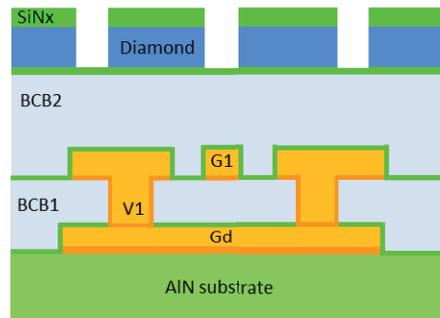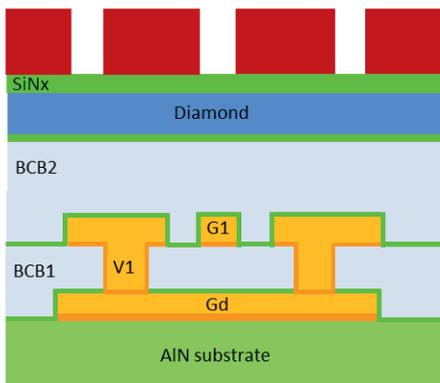
(28) V2: BCB2 etching (SF$_6$ plasma)

(29) G2: plating base G2 layer TiW/Au/TiW

(30) G2: photo lithography

(31) G2: Au plating G2 layer

(32) G2: photoresist removal

(33) G2: plating base removal
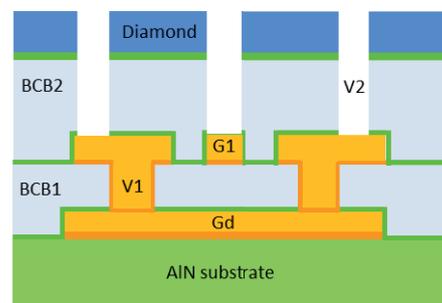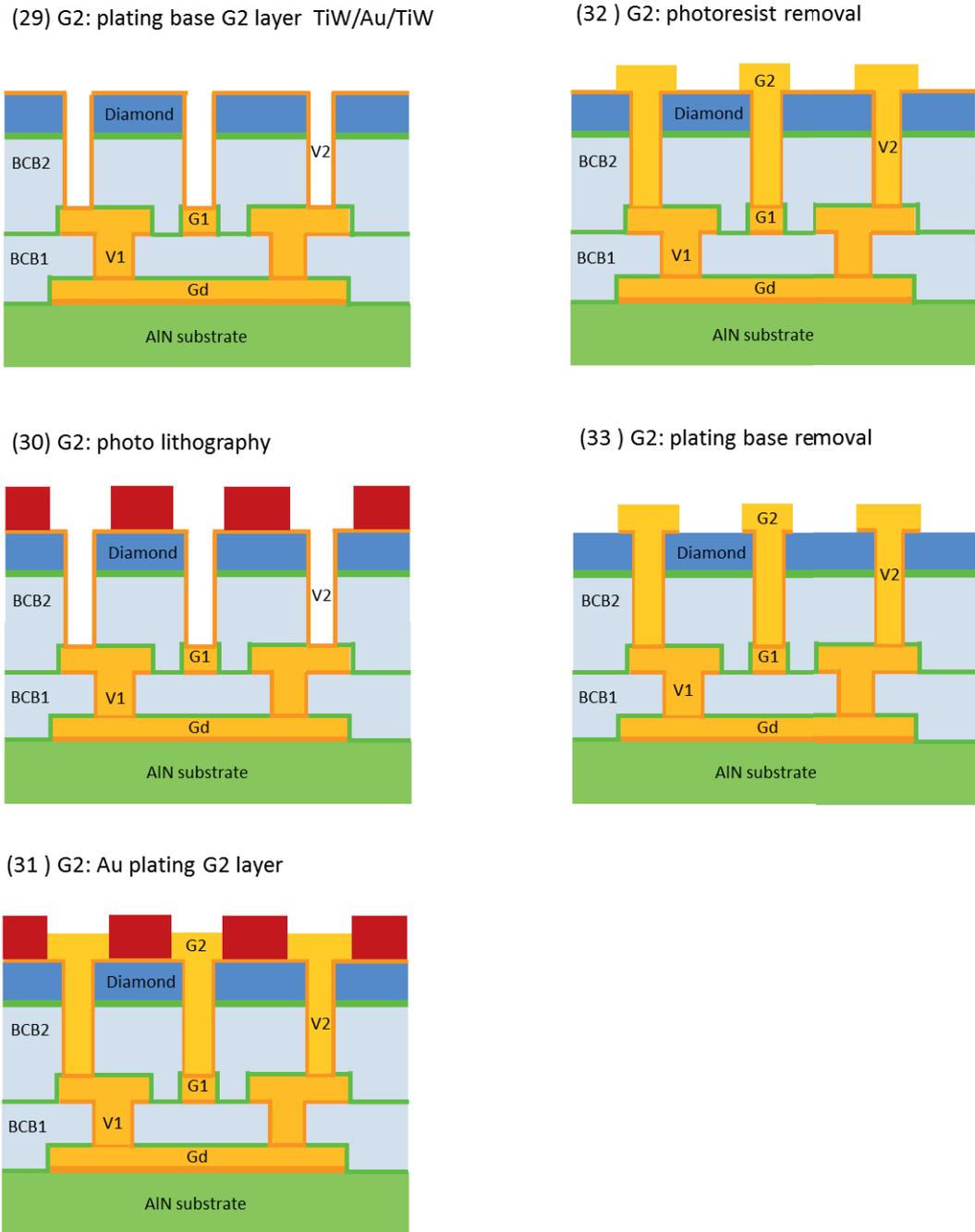
Figure 4.6: Process flow of stripline fabrication with a diamond bonding as a heat sink

For the chip separation process, the hard diamond layer at the saw street, which has a width of 300 µm, needs to be taken into account. The diamond needs to be removed from the saw street to avoid breakage of the dicing wheel. Additionally, a sub-experiment has shown that the mechanical dicing through the thick BCB leads to BCB peeling at the chip corner. Therefore it is necessary to remove the diamond and BCB from the dicing streets before dicing. This can be achieved using a $SiN_x/Al/SiN_x$ hard mask system to etch the diamond and BCB using RIE as in V2 layer, as shown in Figure 4.7.
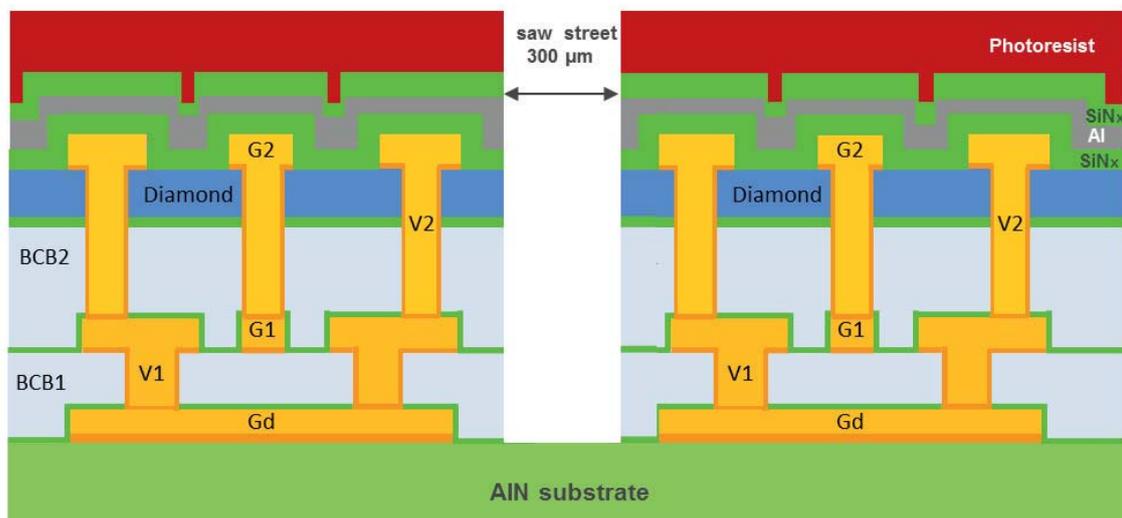
Figure 4.7: Cross-sectional structure of $SiN_x/Al/SiN_x$ hard mask system for saw street etching.

The top SiN_x layer is used as a hard mask during the diamond etching itself. The middle Al mask is to protect the diamond layer during the BCB etching, which is in total 18 µm deep. Without this Al mask, the diamond would be massively etched away. The last SiN_x is to avoid a direct contact of Au structure to the hard mask Al.

To begin the dicing street etching, the 300 µm saw street is defined on the top layer of SiN_x hard mask using i-line photolithography with a positive photoresist of 2.5 µm before the SiN_x is opened by SF_6 plasma etching, followed by the removal of Al using H_3PO_4 solution. Again, the last SiN_x layer is removed by RIE in the same way as its first layer. After the removal of diamond and BCB, the whole hard mask layer has to be removed again with the same methods. The mechanical dicing can then be performed directly to the exposed AlN

surface in the saw street area. Figure 4.8 illustrates the AlN surface at the saw-street area after diamond and BCB have been clearly removed by RIE etching.
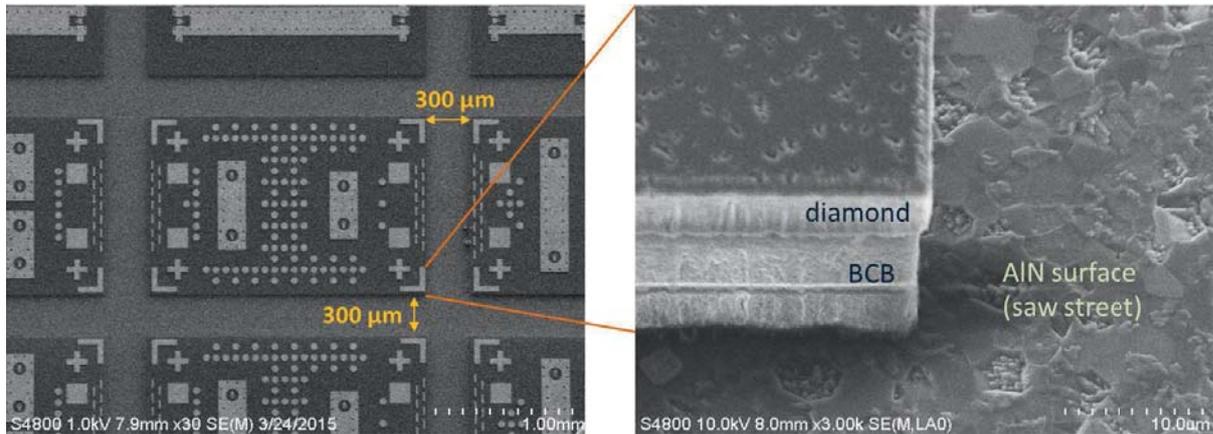
Figure 4.8: SEM images of the diamond and BCB etching at the saw street area before the mechanical dicing of AlN substrate.

4.2.2 Substrate Fabrication
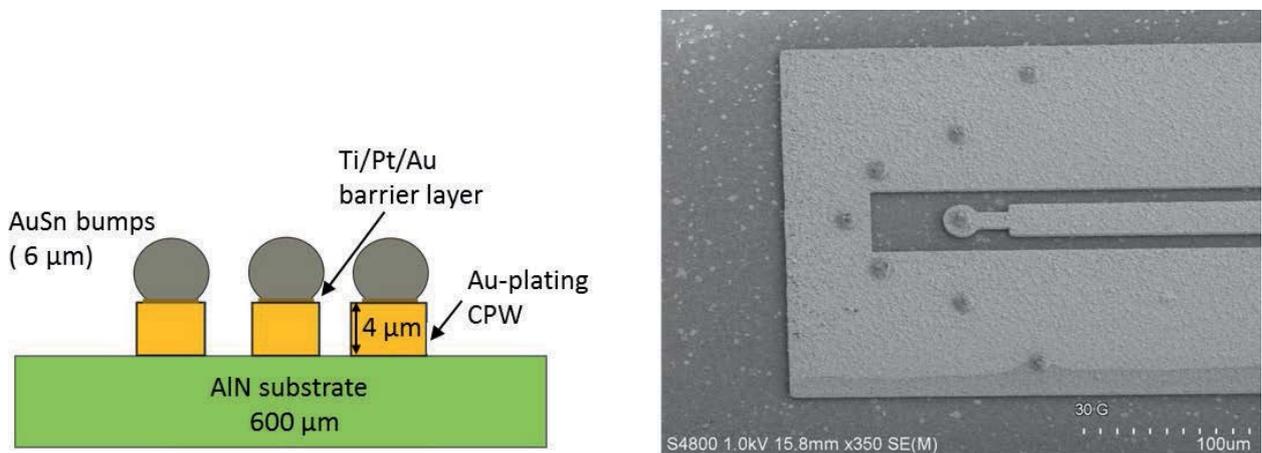
Figure 4.9: Cross-sectional CPW substrate (left), SEM image of fabricated substrate (right).

As already described in chapter 3, the substrate process starts with the deposition of a seed layer, TiW/Au/TiW, directly on the 3 inch AlN wafer. Subsequently, CPW lines

are patterned by stepper lithography, followed by Au plating of 4 μm thickness. At the location of the flip-chip microbumps on top of the CPW lines a barrier layer stack consisting of Ti/Pt/Au is deposited through a lift-off mask in order to suppress unwanted diffusion between the AuSn bumps and the electroplated Au in the CPW line. Subsequently, another lithography step for miniaturized AuSn bumps with the lateral dimensions of 10 μm was implemented. The photoresist used in this step is a negative photoresist of 15 μm thickness, which allows to evaporate 6 μm thick AuSn bumps on top of a 4 μm thick Au-plated CPW. AuSn bumps are structured and evaporated as multilayers directly onto the surface of the barrier layer, starting with a Sn layer and ending with a gold cap layer. The overall AuSn stack composition is 80% wt. Au and 20% wt. Sn. The process flow of forming miniaturized AuSn bump was described in chapter 3. Figure 4.9 shows the cross-sectional structure of the CPW on the substrate (left) and the top view of the fabricated AuSn bumps on Au-plated CPW (right).

4.2.3 Flip-Chip Bonding

To obtain good ohmic contact during flip-chip bonding, it is necessary to remove the Sn oxide on the bump surface before the flip-chip assembly. Therefore, prior to soldering, the substrate chip is immersed in a dilute hydrochloric acid (HCl) solution with 1:1 $HCl:H_2O$ concentration for about 30 seconds. The flip-chip alignment and bonding is performed using the FC150 flip-chip bonder.

During the bonding, the temperature of the chuck substrate is set to 320 °C. The bonding is done under formic gas atmosphere, i.e., in a 95% N_2 and 5% H_2 environment. The alignment of the flip-chip bonding can be measured with the help of a transparent test chip as shown in Figure 3.9. Under optimum conditions, the equipment can achieve ±1 μm lateral accuracy. An offset of less than 2 μm across the samples is observed. The design included a margin of around 5 μm from the bump position to the metal edges.
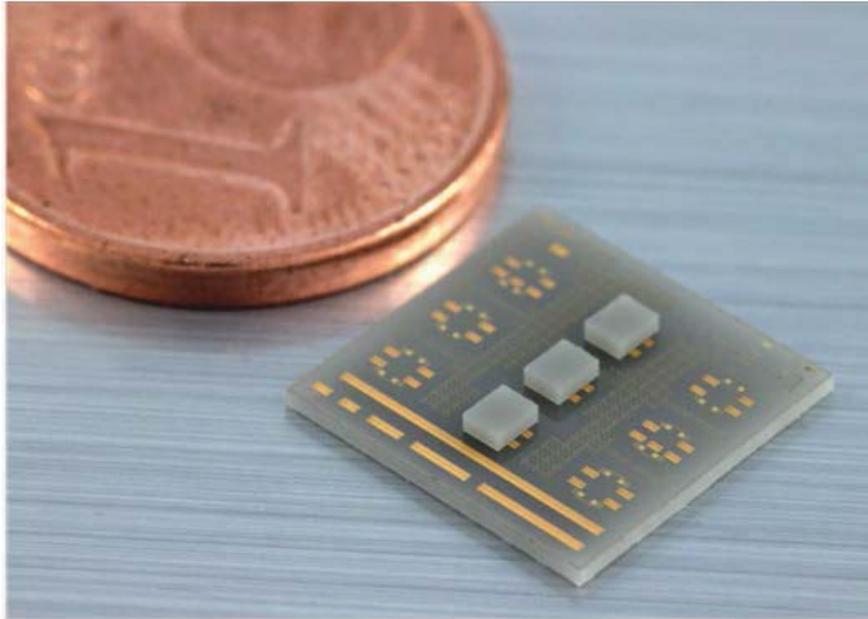
Figure 4.10: A photograph of a successfully fabricated diamond flip-chip on AlN carrier.

4.3   Measurement Results

The interconnects were characterized using a back-to-back test structure with a flip-chip bonded chip containing a thru-line (see Figure 4.1). S-parameters were measured using a vector-network analyzer (VNA) with coplanar wafer probes. The VNA was calibrated using the on-wafer multiline Thru-Reflect-Line (TRL) method [101], to the CPW on the substrate. The reference plane is placed on the CPW at the interconnect. The measured S-parameters (solid curves) are plotted in Figure 4.11 up to 325 GHz, together with the 3D EM simulation data (dashed curve).

The signal path of the test structure includes two transitions and a thru-line of 800 μm length, realized as stripline. Up to 250 GHz, the structures exhibit a total insertion loss below 2.0 dB and return loss values larger than 10 dB. One concludes that the insertion loss of a single transition with 400 μm stripline is less than 1.0 dB. As can be seen in Figure 4.11, the measurement results are in good agreement with the results from 3D EM simulation. Beyond 250 GHz, the measured transmission data show a local maximum. This is due to uncertainties in calibration, mainly caused by severe radiation effects of the CPW lines on

the substrate, which are used for calibration. Nevertheless, the measurements indicate that the overall behavior continues to be smooth also beyond 250 GHz, thus showing the potential of the transitions for frequencies up to 325 GHz.
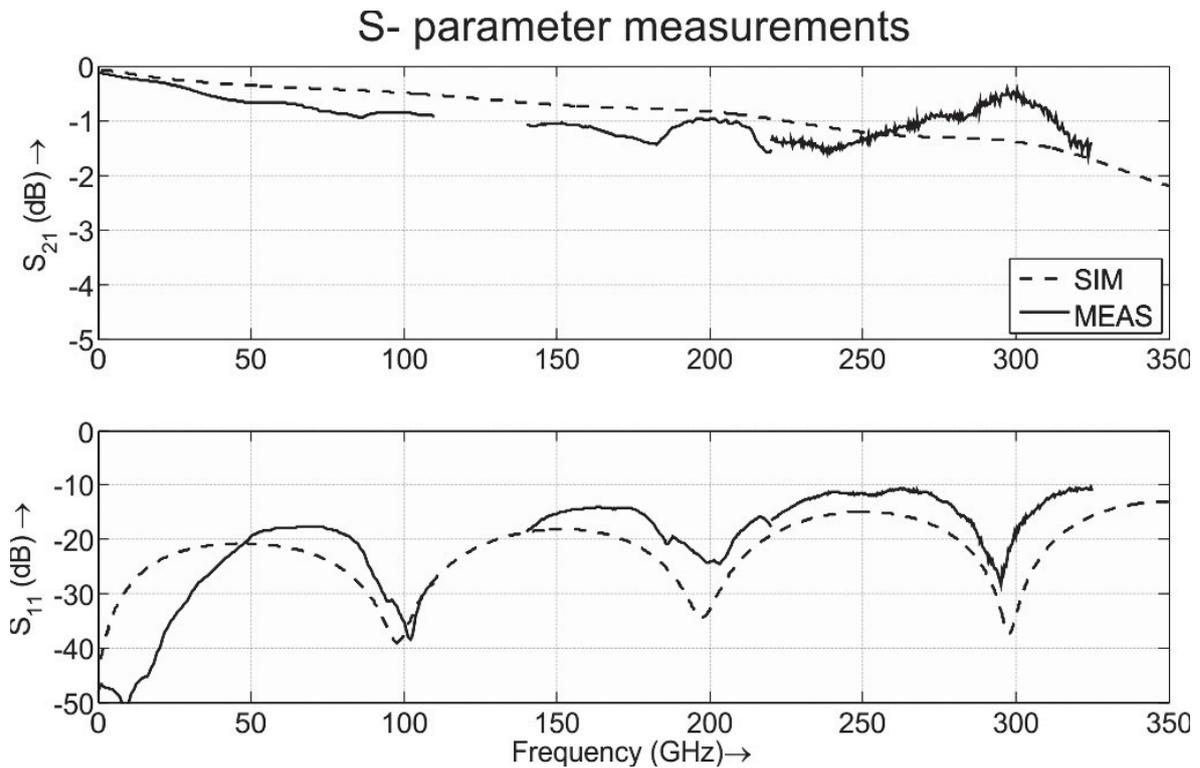
Figure 4.11: Comparison of S-parameters between the measurement (solid) and simulation (dash) of the back-to-back structure up to 325 GHz.

4.4 Lateral Alignment of Vias and Bumps

Among the critical tolerances in the process are the position of the bumps and the alignment of the vias in the chip side. Since this flip-chip transition is constructed by combining the excellent-shielding stripline system on the chip with an ordinarily exposed CPW waveguide line, therefore the strong radiation effect can be observed in the measurement when the operating frequency exceeds 250 GHz. To examine the influence of fabricated structural

dimensions on the transition behaviors, lateral alignments of vias and bumps are analyzed using 3D CST simulations, which was performed by S. Sinha as below.
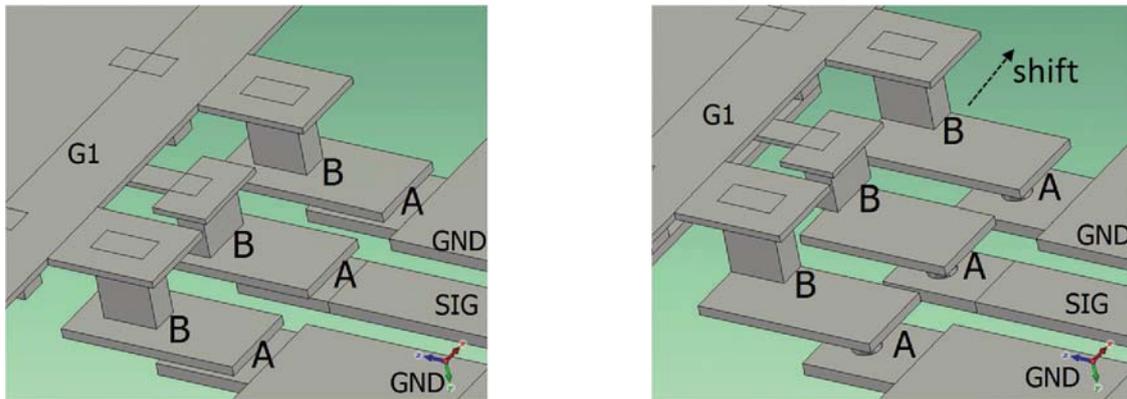
Figure 4.12: Standard transition with no tolerances (left), transition with cumulative shifts of all elements: bumps (A) by 10 μm , vias (B) again by 10 μm in both planar directions (right).
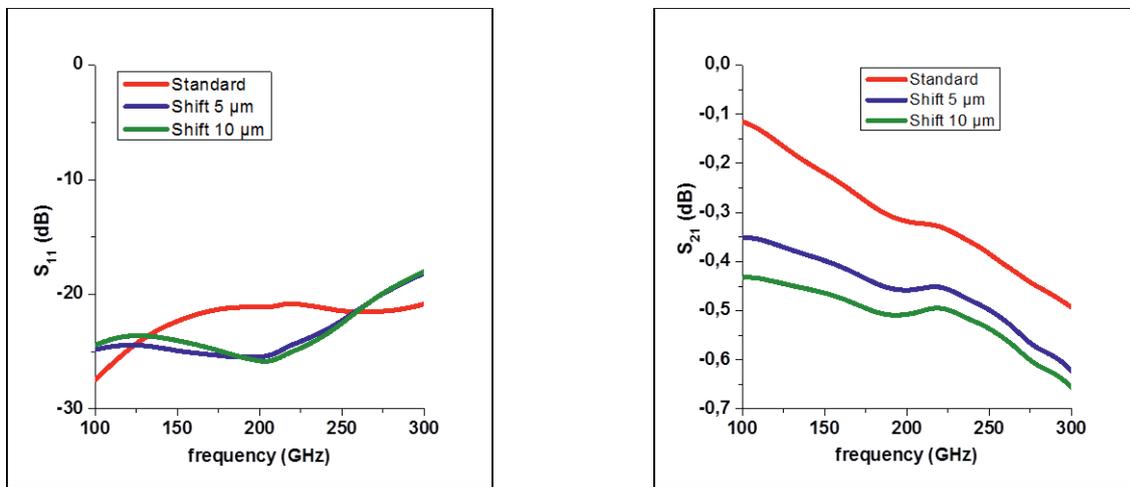
Figure 4.13: Reflection S_{11} of the transition with 0, 5 and 10 μm shift of bumps and vias in both planar directions (left), S_{21} insertion loss of the transition in the same way of horizontal shifting.

Owing to the stepper lithography process, the lateral alignment of the via and bump positions is within $< 1 \mu$m accuracy. Simulations were carried out applying cumulative shifts to the bumps and vias. Each type is shifted by 5 and 10 μm in both planar directions against the metal level below. As it is demonstrated in Figure 4.12 the shift of 10 μm leads to the worst possible configuration where the transition can operate properly because GND and signal elements are still unconnected. The simulation results of the misalignments up to 300 GHz are shown in Figure 4.13.

As can be seen in Figure 4.13 (left) there is no difference in the return loss $|S_{11}|$ between the lateral displacement of 5 and 10 μm. Both of the shifts lead to the $|S_{11}|$ of 21 dB at 300 GHz, while the accurate placement (standard) gives the loss of 18 dB, which is only 3 dB difference in such a massive misalignment. A similar situation occurs for the insertion loss $|S_{21}|$ at the same observed frequency. The standard placement gives the $|S_{21}|$ value of around 0.5 dB, whereas crucial displacements of 5 and 10 μm only slightly increase the $|S_{21}|$ to 0.6 and 0.65 dB, respectively. From these results it can be concluded that this design is very robust to bumps and via misplacements. Even such strong tolerances affect the transmission properties only slightly.

Chapter 5

Stripline-to-Stripline Interconnect

In chapter 4, utilizing a stripline on the chip side and a CPW on the mother board has shown an interconnect performance in sub-mm wave applications up to 250 GHz with the potential of frequency extension to 325 GHz. However, beyond 250 GHz the CPW lines on the substrate severely suffer from radiation losses. The results of this stripline-to-CPW module leads to the motivation for a new design, which can well suppress the radiation loss by replacing the CPW lines on the substrate carrier with a stripline, forming a stripline-to-stripline interconnect. The aim of this re-design module is to develop a flip-chip connection up to 500 GHz.

5.1   500 GHz Interconnect Design Approach

In order to develop flip-chip interconnects, which achieve such extremely high frequencies, there are two distinct technological challenges related to scale RF flip-chip assemblies: 1) the fabrication of miniaturized AuSn bumps, and 2) the predictable construction of low-loss waveguiding chips and submount substrates. The 10 μm diameter AuSn microbumps and the technological based-line for AuSn fabrication were already discussed in detail in chapter 2 and chapter 3. To minimize radiation loss, the stripline, with its optimized shielding, is chosen for the chip-to-submount connection.

The design and fabrication of suitable waveguiding structures on the chip and the submount was done in a multilayer conductor scheme consisting of up to three gold layers with benzocyclobutene (BCB) as an interlayer dielectric, including vertical connections through gold-filled via holes. Beyond 250 GHz, radiation losses become the main limiting factor in RF waveguide design. To overcome this issue, maximum shielding systems are applied including the replacement of the CPW lines on the submount carrier in our previous design in chapter 4 by a shielded stripline. By maintaining the stripline on the chip side, a coaxial-like 'stripline-to-stripline' interconnect between chip and submount is formed. The further shielding techniques, which are 1) adding via fences along the feature length and 2) placing circular ground bumps around the transition areas, are also implemented to the system in order to obtain a transition functioning up to 500 GHz. The proposed structure is illustrated in Figure 5.1.
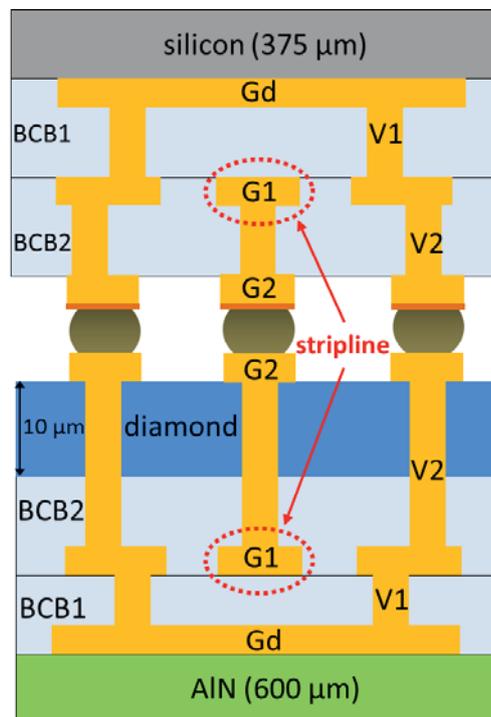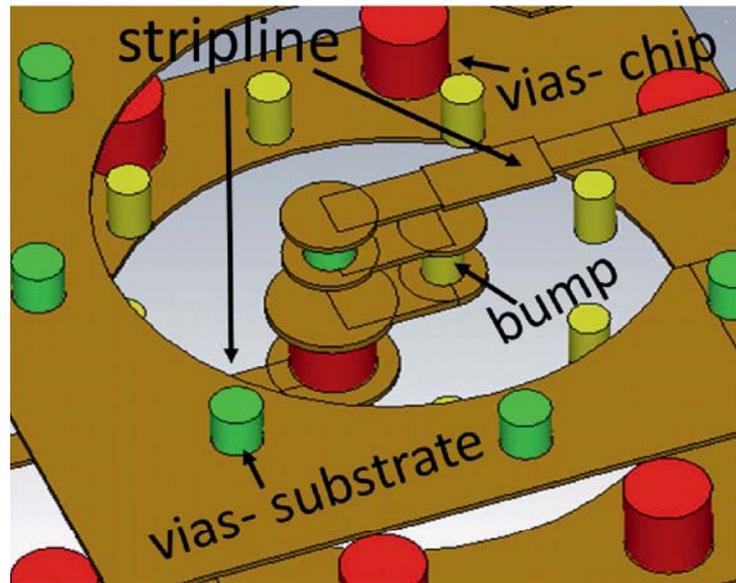
Figure 5.1: The 3D structure of stripline-to-stripline transition area (top) and cross-sectional view of flip-chip mounting (bottom).
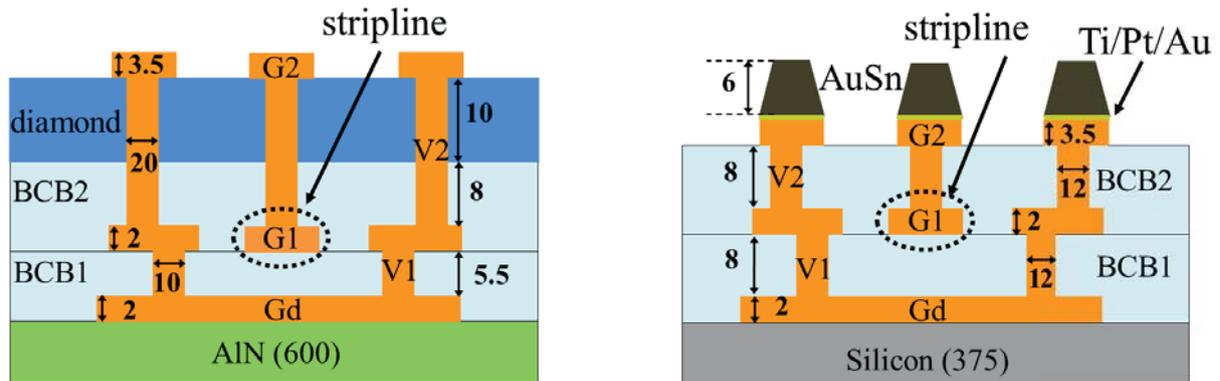
Figure 5.2: Cross-sectional views of chip (left) and submount (right) wiring levels and interconnect vias. All dimensions are shown in micrometer (μm).

5.2 Fabrication Process of Chips and Substrates

Figure 5.2 shows the cross-sectional structures of chip and submount of the stripline-to-stripline connection which provides the highest degree of shielding. Both chip and submount structures are fabricated in conventional front-end semiconductor processes on 3″ substrates. The use of i-line stepper lithography in the fabrication of all layers results in very high structure fidelity and uniformity. The stripline chips are built onto AlN carrier substrates for compatibility with our in-house InP HBT transferred-substrate process [9]. Although the chip construction in this experiment is made in the same fashion as the chip structure presented in chapter 4, the detailed dimensions such as lateral structures, BCB thickness and via diameters are different. The stripline submounts were realized either on AlN or on silicon substrates. In this case, the silicon substrates do not incur additional propagation losses because of the complete shielding of the transmission lines.

As illustrated in Figure 5.2, chip and submount contain three metal layers: bottom ground (Gd), stripline (G1), and upper ground (G2). The AuSn bumps connect the chip's G2 layer with the submount's G2 layer upon completion of the flip-chip process. The designed stripline width in layer G1 is 9 μm. The metal layers are separated vertically by the BCB. The distance between the upper metal surface of layer Gd and the bottom of the signal strip layer G1 is 5.5 μm for the chip side, and 8 μm for the substrate side. The distance between
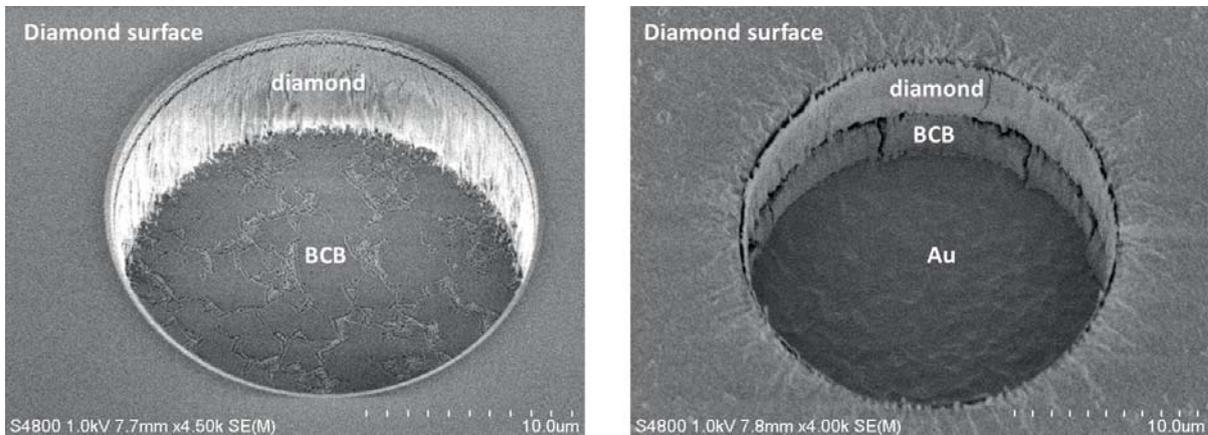
Figure 5.3: SEM pictures of the via etching V2, diamond etching until BCB surface (left) and BCB etching until G1 gold layer (right).

the upper metal surface of G1 to the bottom of layer G2 is 18 μm for the chip, and 8 μm for the submount.

The vertical connection between the metal layers is facilitated by via opening in the BCB interlayer dielectric (V1 and V2) as depicted in Figure 5.3, which are realized with SF_6 reactive ion etching (RIE), enabling a smallest possible via diameter of 10 μm, which is only half of the via diameter of the structure in chapter 4 (Figure 4.5). One critical problem from the RIE etching of V2 layer is the distortion of the stepper marks. This happens because the V2 stepper marks, which are also located on the diamond surface, have a size of 4x4 μm^2. These stepper marks are etched at the same time as the V2 vias, which are in total 18 μm depth. Due to this massively long etching time, the mark dimensions expand laterally and connect to each other. As a result, these deformed stepper marks cannot be used for the alignment with the next layer anymore. Hence, an additional layer is required to provide auxiliary stepper marks, leading to more processing steps and increased processing time.

All interconnect layers are formed by gold electroplating with a metal thickness ranging from 2 to 3.5 μm, which also fills the underlying via openings. For the chip wiring, a large vertical separation between G1 and G2 was chosen in order to accommodate into the layer stack a 10 μm thick nano crystalline diamond layer, acting as a heat spreader as required for the in-house developed InP HBTs [9]. Figure 5.5 illustrates the process sequence of the stripline fabrication of the 500 GHz submount, starting from the blank silicon substrate (step 1),

forming the gold plating of Gd layer (step 2 to 6), adding a passivation and dielectric BCB1 layer (step 7 to 8), structuring and etching the first via V1 (step 9 to 11), and filling the Au plating in V1 to create G1 layer (step 12 to 16). The same process fashion is done in order to form the BCB2, V2 and G2 layers as shown in step 17 to 26.

Around the signal bump within the flip-chip transition area, several shielding bumps are placed on top of the G2 layer, resulting in an electrical 'fence' around the signal connection, effectively suppressing radiative leakage losses. The eutectic $Au_{80}Sn_{20}$ bumps have a thickness of 6 µm and a diameter of 10 µm. The bumps are processed in the same way as described in chapter 3. The desired eutectic composition is obtained by alternating Sn and Au layers in a multilayer scheme with appropriate layer thickness. The evaporation sequence ends with a thin gold cap layer to suppress surface oxidation. The AuSn bumps and the underlying electroplated Au interconnect layer G2 are separated by a thin Ti/Pt/Au diffusion barrier layer, which is patterned in an additional lithographic lift-off step, in order to prevent the unwanted diffusion from Au to Sn.

Upon completion of the frontend processes, both 3 inch chip and submount wafers are mounted on blue tape and diced with a conventional diamond saw. The flip-chip assembly is carried out using an FC150 semi-automatic bonder. Prior to the bonding process, the natural oxide on the AuSn bump surface is removed with a dip in $HCl:H_2O$ (1:1) for about 60 seconds. The flip-chip bonding temperature used in this experiment is around 320 to 350 ºC, and the heating time during bonding is at least 100 seconds in order to transfer adequate heat through the entire BCB stacks to the AuSn bumps.
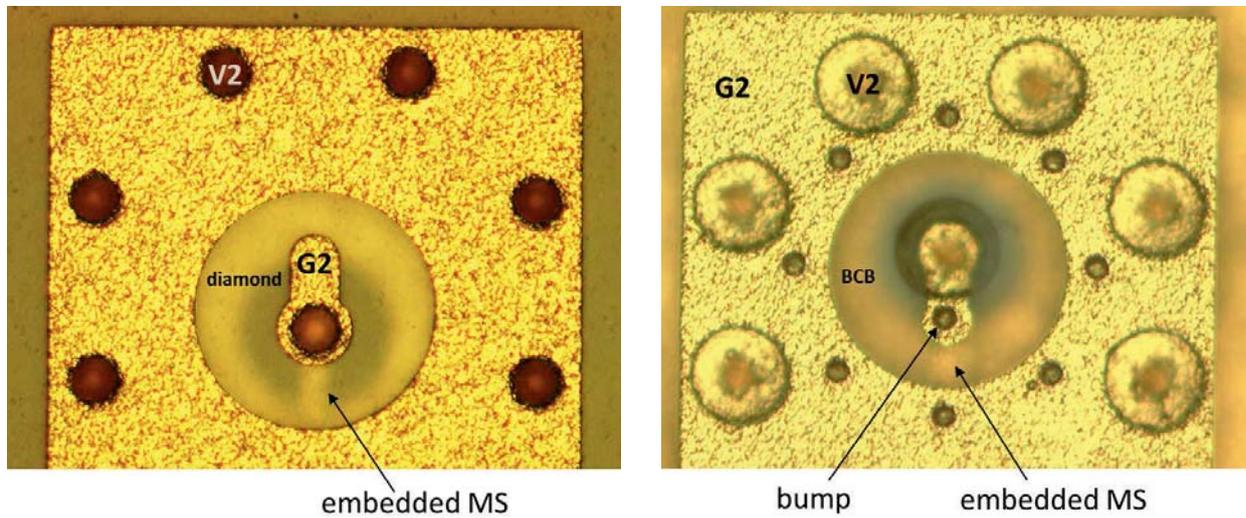
Figure 5.4: Top-viewed microscopic pictures of transition areas showing G2 as top layer of the chip side. The embedded MS is visible under the diamond layer (left). On the substrate side the MS is embedded under a BCB layer and the transition is surrounded by ground bumps (right).

1) blank substrate

Si

2) GD: seed layer

Si

3) GD: Lithography for Gd Au-plating

Si

4) Gd: Au plating

Gd

Si

5) Gd: PR removal

Gd

Si

6) Gd: seed layer removal

Gd

Si

7) SiNx PECVD

Gd

Si

8) BCB1

BCB1

Gd

Si

9) V1: Photoresist

BCB1

Gd

Si
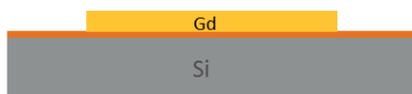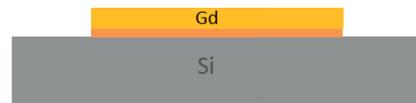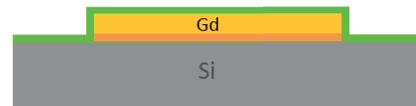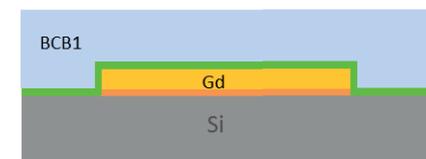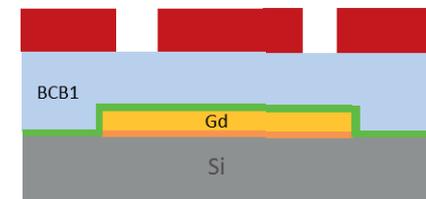
10) V1: BCB etching (SF$_6$ plasma)

V1

BCB1

Gd

Si
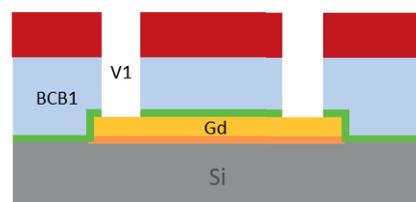
11) V1: PR removal

15) G1: PR removal (plasma etching)
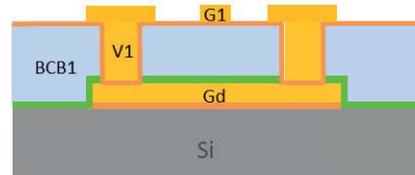
12) G1: seed layer

16) G1:plating base removal
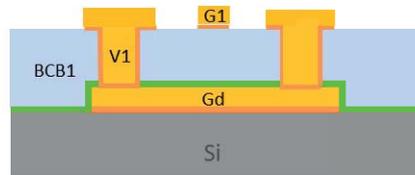
13) G1: Photoresist
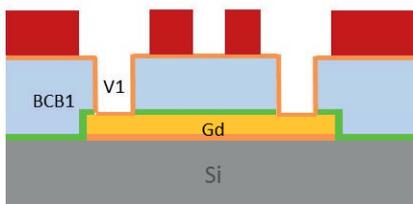
17) SiNx
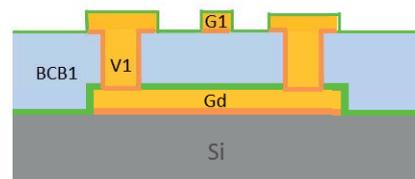
14) G1: Au plating
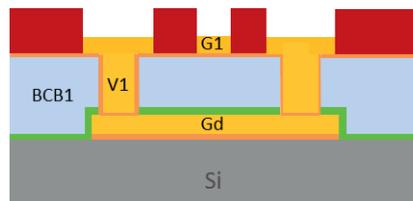
18) Second BCB layer (BCB2)
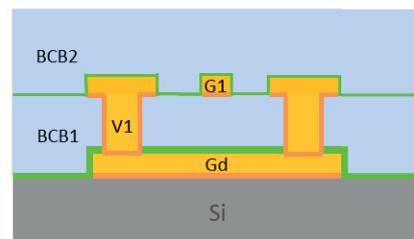
19) V2: PR for BCB via etching
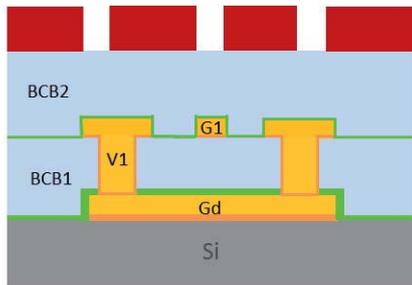
22) G2: seed layer
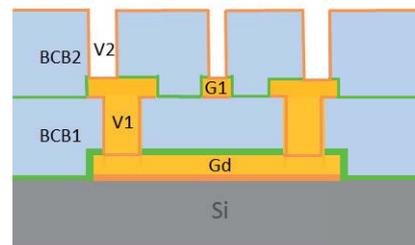
20) V2: via etching BCB (SF$_6$ plasma)
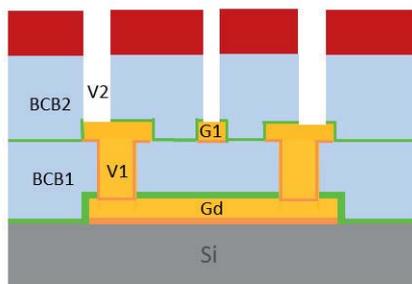
23) G2: PR for Au plating
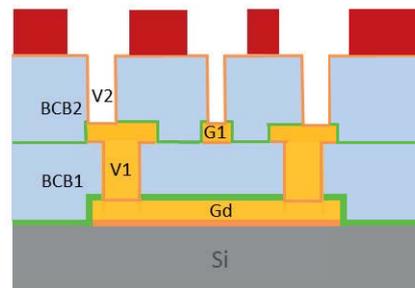
21) V2: PR removal
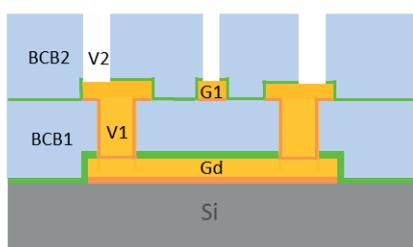
24) G2: Au plating
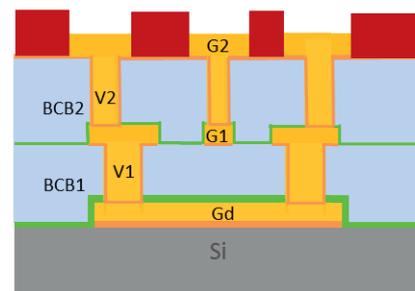
25) G2: PR removal
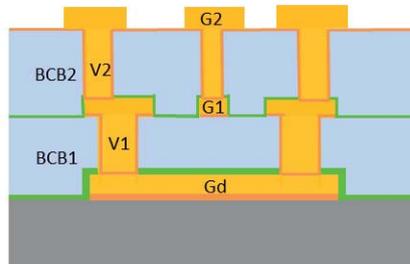
26) G2: seed layer removal
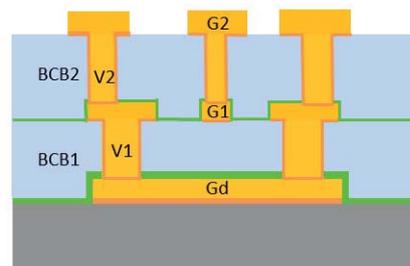
Figure 5.5: Process steps of stripline fabrication of the 500 GHz submount

5.3   Measurement Results

Figure 5.6 presents the results of scattering parameter measurements of three back-to-back flip-chip interconnects up to 500 GHz. These stripline-to-stripline structures have a total length of 1.8 mm, which contains a thru-line of 160 µm length on the chip side. The assemblies were tested on an on-wafer prober with two coplanar probe tips, containing a transition to hollow waveguide and being connected to one of several frequency extenders to enable banded measurements up to 500 GHz with a Rohde & Schwarz® ZVA67 vector network analyzer (VNA). The system was calibrated using the on-wafer multi-line Thru-Reflect-Line (mTRL) method [101]. Suitable calibration structures were provided on both chips and submounts. The measurement results of an optimized stripline-chip-to-stripline-submount transition are shown together with 3D EM simulations in Figure 5.6. At 500 GHz a total insertion loss of 5 dB and a return loss of greater than 18 dB of these two transition structures is observed. By excluding the stripline loss, the insertion loss remains only around 1 dB per transition. The measurements show good agreement with simulation, and the three measured chips give similar output. This indicates design robustness, technology stability and and also good reproducibility of the process.
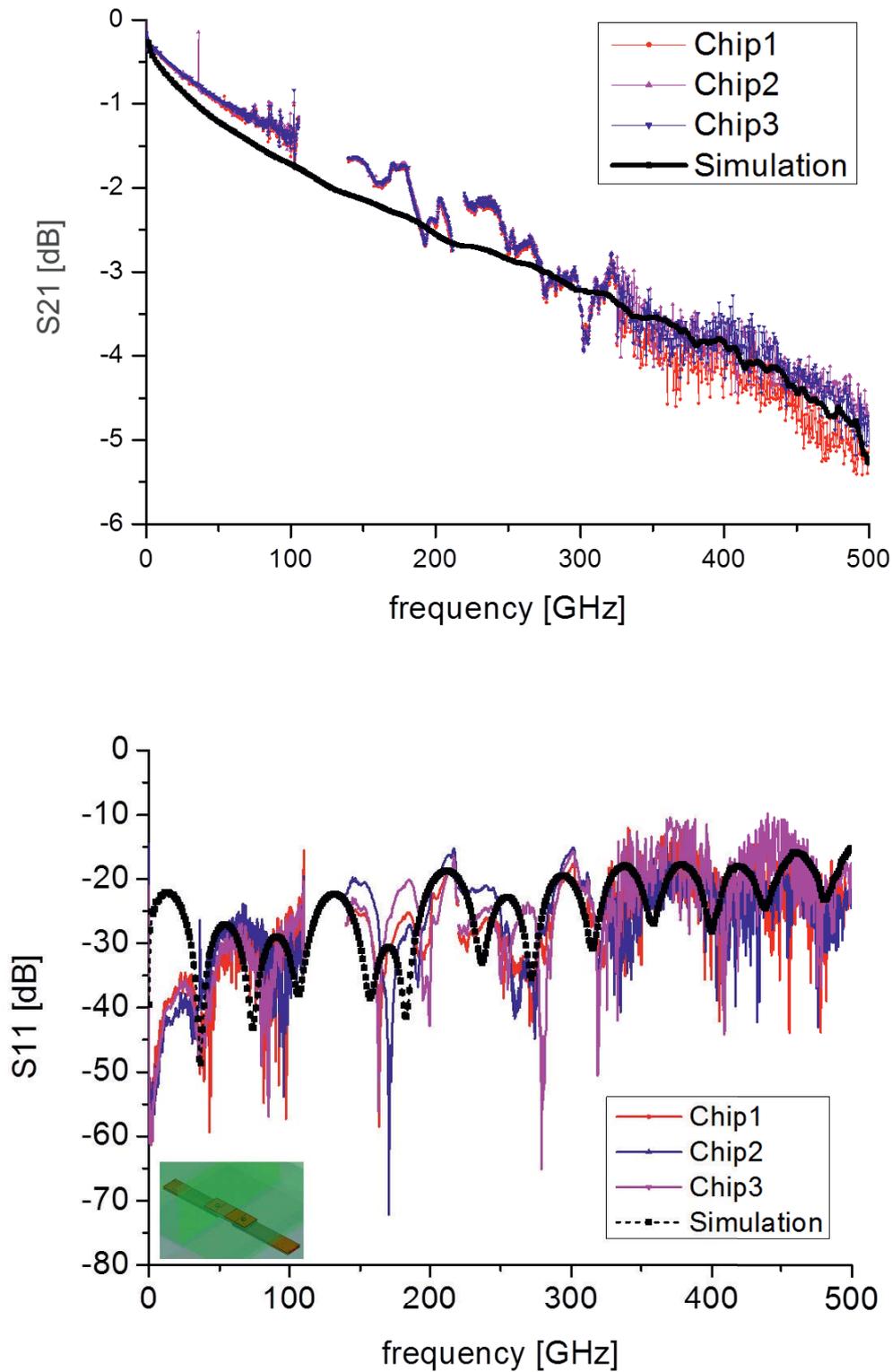
Figure 5.6: *S*-parameters of the flip-chip interconnects from simulation (black) and measurement (color) up to 500 GHz.

5.4 Design Robustness Versus Process Tolerances

In this section, the tolerances of process deviations, namely 1) bump height, 2) bump displacement, 3) stripline width, 4) lateral shifting of G1 layer, 5) V1 dielectric thickness, 6) V2 dielectric thickness, and 7) diamond thickness, are investigated up to 500 GHz using 3D EM simulation. In prior work, several studies have been conducted to examine the influence of physical interconnect dimensions on high frequency characteristics, however most of the previously published work is related to CPW-type transmission lines, and none of them is analyzed up to such high frequency [113].

5.4.1 Influence of Bump Height

The design is robust to bump height because the line is shielded. The striplines are well-shielded transmission lines with an embedded signal line inside the top and bottom ground planes. Hence, detuning effects due to bump height variation do not occur to this type of waveguide. As a result, only little influence from different bump height occur at the transition area.

Figure 5.7 shows the simulation of different bump heights of 1, 2, 5, 10 and 20 µm. The simulation indicates that the bump height only dominantly affects the S_{11}. However, the change from 1 to 10 µm still results in the return loss values of more than 20 dB, and there is no difference in the insertion losses. The situation turns critical when increasing the bump height to 20 µm, which does also degrade the insertion loss (S_{21}). Nevertheless, a bump height of 20 µm is not practical in our case since our original pre-bonding bump height is only 6 µm.
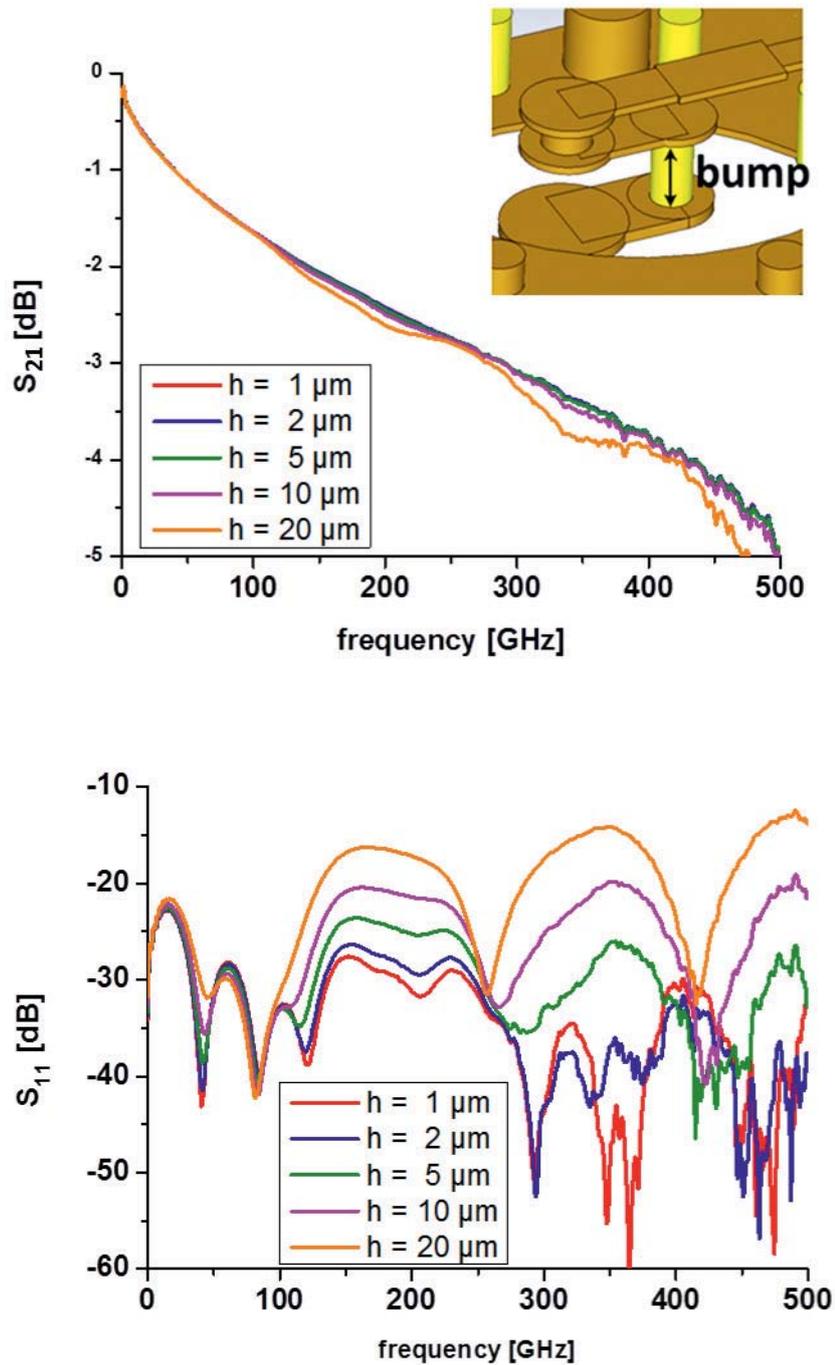
Figure 5.7: The influence of bump height variations (h- 1, 2, 5, 10 and 20 μm) on the S-parameters of two flip-chip transitions (back-to-back) from 3D EM simulation.

5.4.2 Bump Displacement

The accurate lateral alignment is owed to i-line stepper definition (Nikon i12) of the bump lift-off resist mask, using typically eight alignment dies per wafer in an enhanced global alignment scheme. The actual flip-chip assembly on the FC150 flip-chip aligner introduces an additional lateral offset inaccuracy of ± 1.0 μm. The 3D EM calculations of Figure 5.8 show that an extreme lateral bump shift in both directions S and I in the order of 10 μm would only slightly affect the transmission properties, owing to the robust design approach incorporating oversized landing pad structures at the bump location. Therefore, there is no concern of the bump misalignment towards the transition quality.
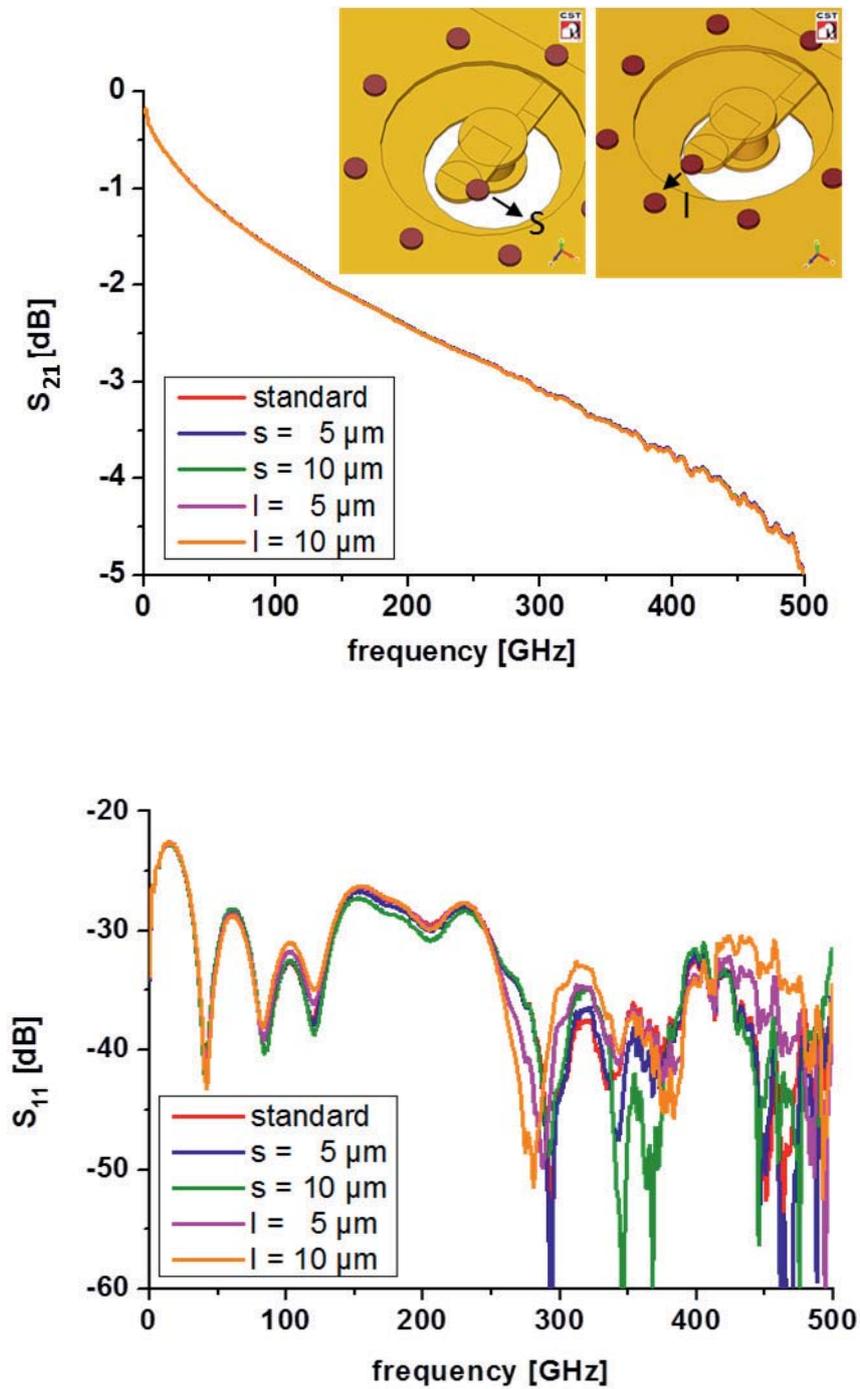
Figure 5.8: The influence of bump displacement in the S and I directions with the maximum shift of 10 µm on the S-parameters of two flip-chip transitions (back-to-back) from 3D EM simulation.

5.4.3 Stripline Width

As previously mentioned in chapter 4, the electroplating process leads to a slight expansion of the dimensions of the plated structures. Therefore, it is important to shrink the line width by 0.45 μm on each side in the layout, in order to obtain the exact line dimension after the Au plating.

The simulations in Figure 5.9 investigate the influences of stripline width deviations (G1 layer) of ± 2 μm to the S-parameters up to 500 GHz, compared to the standard 9 μm strip width. It is revealed that the S_{21} parameter does not change with the 2 μm width deviation. In the case of S_{11}, however, the above-mentioned variation of stripline widths, clearly increases the reflection coefficient from - 35 dB to -25 dB. Nevertheless, either of this width deviation still keeps the return loss $|S_{22}| \geqq 25$ dB, which is an acceptable value for the interconnects. Besides, a 2 μm change in the signal width would be considered as a major unrealistic process deviation. With the biasing layout method applied in this development, the Au plating process delivers a precise signal line width as can be seen from the SEM images in Figure 4.3. Width deviations of only ± 0.5 μm are observed on the fabricated structures.
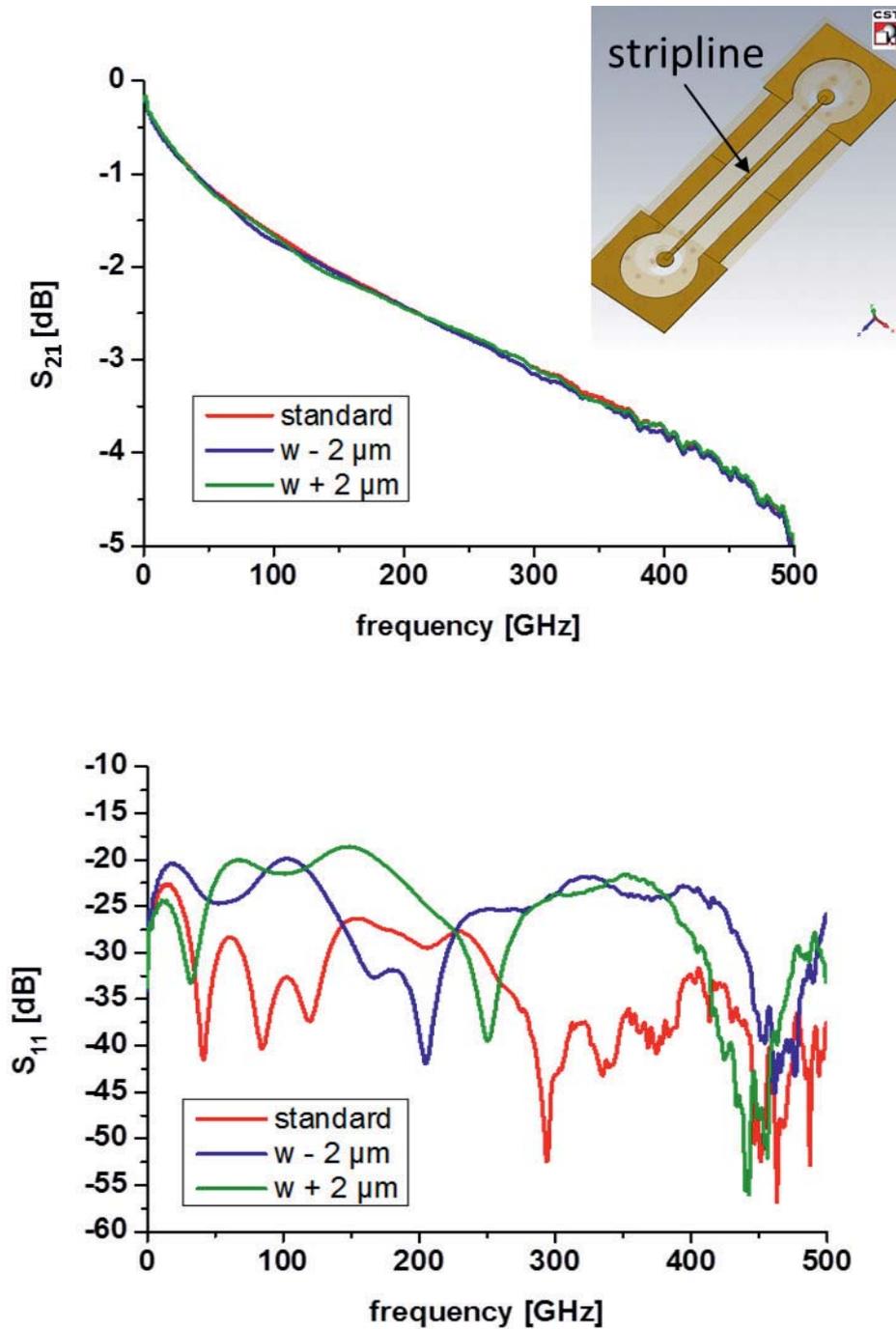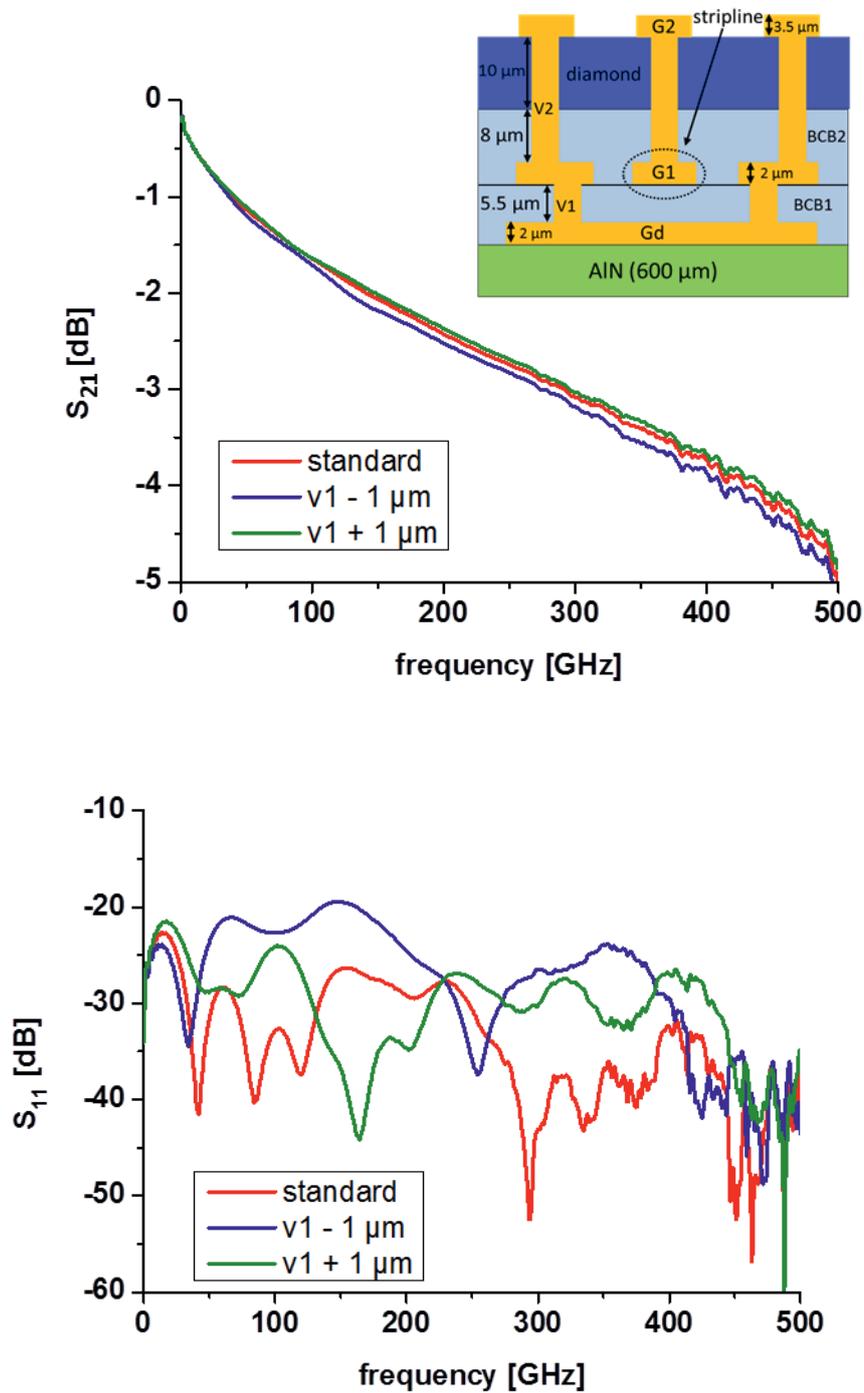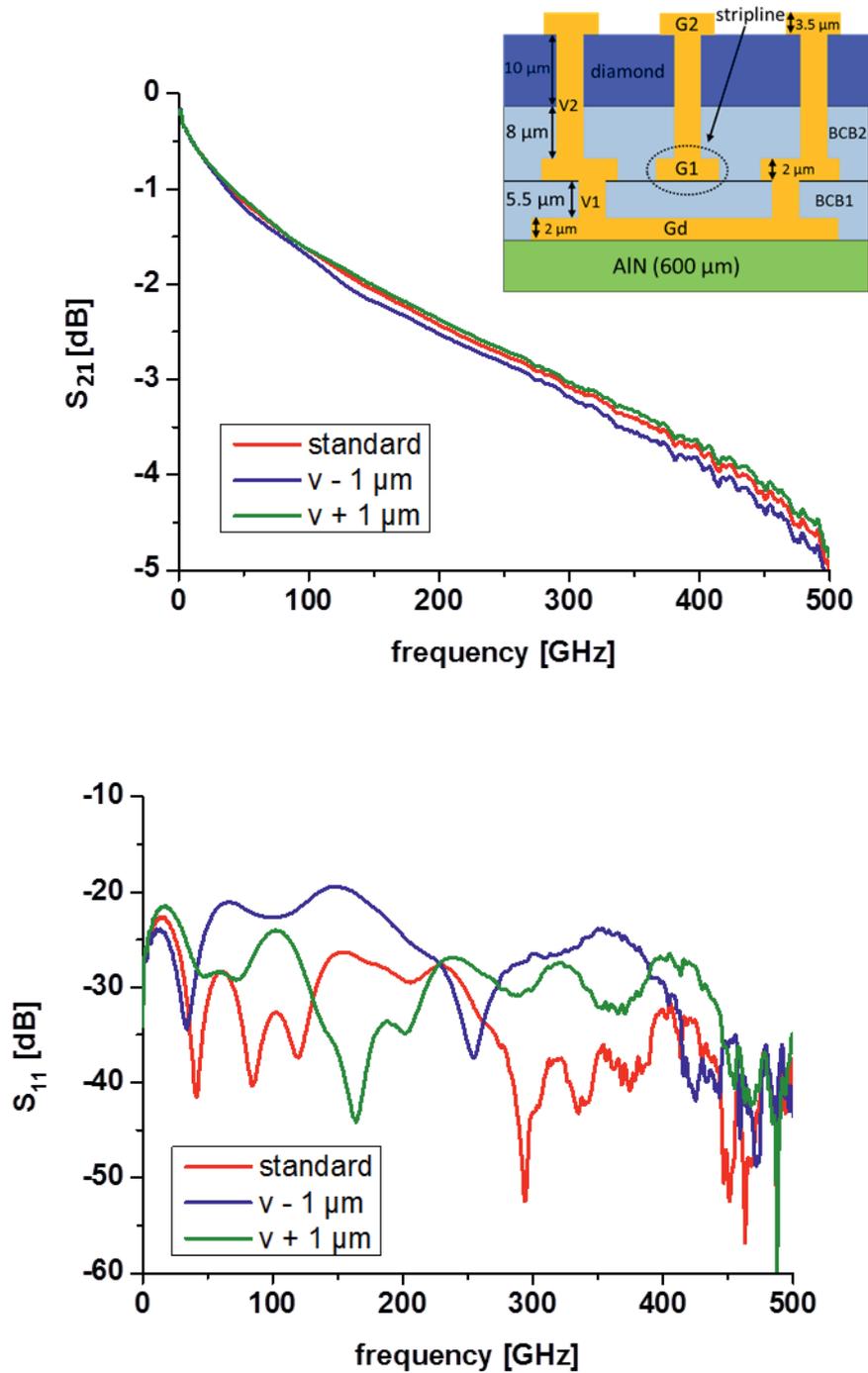
Figure 5.9: The influence of stripline width variations of $\pm 2\,\mu m$ on the S-parameters of two flip-chip transitions (back-to-back) from 3D EM simulation.

5.4.4 Lateral Alignment of G1 Stripline Layer

The misalignment of G1 metal is generally within ± 1 µm but it would be larger if the stepper could not read the alignment masks. However, the following simulations are performed from the standard situation (accurate placement) to the possible case of 2 µm misalignment and the extreme case of 4 µm shifting.

The simulation shows a strong influence of the lateral misalignment of the entire G1 layer on the S_{11} parameters. As depicted in Figure 5.10 a lateral shift of 4 µm can increase return loss values to around 16 dB at 500 GHz, whereas the shift of 2 µm results in 22 dB. Compared to the case with no misalignment, the interconnects show return loss values of 37 dB. The lateral shift of the entire conductor layer leads to an asymmetric placement of the signal line in the vertical transition region, which resembles a vertical coaxial connection when considering the placement of the ground fencing bump. The positional offset leads to a change in line impedance which mainly impacts the return loss values. The insertion loss is only slightly affected by the shift as shown in Figure 5.10. In any case, in all of our structures the lateral offset of the signal conductor within the multilayer waveguide structure was less than ± 0.5 µm thanks to i-line stepper lithography being used in all patterning steps. Even taking the lateral flip-chip alignment of ± 1.0 µm into full account S_{11} would not degrade to above -18 dB.
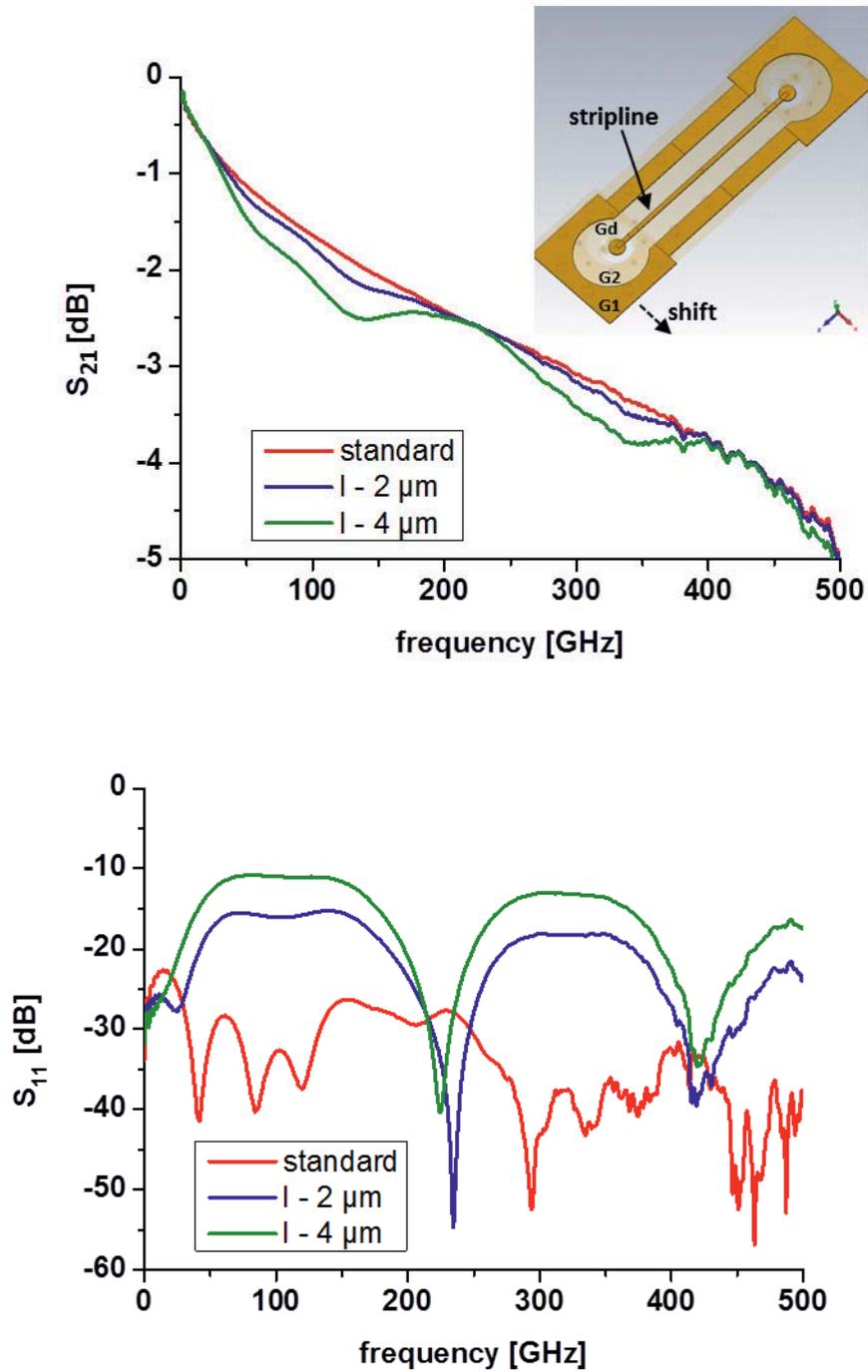
Figure 5.10: The influence of lateral shift in G1 pattern (0, 2, 4 μm offset) on the S-parameters of two flip-chip transitions (back-to-back) from 3D EM simulation.

5.4.5 BCB1 Thickness (dielectric between Gd bottom ground and G1 stripline layer)

BCB1 is the thickness of BCB as measured from the top surface of Gd layer to the bottom surface of the G1 layer as depicted in Figure 5.2. The design value (standard) of the BCB1 on the chip side is 5.5 μm, while on the substrate side it is 8 μm. In simulations, the BCB thickness deviations on the chip side are studied.

Practically, the BCB is applied to the wafer surface using the spin-coating process. Its thickness is controlled by the spin speed during the coating. In this case, the maximum spin speed of 6000 rpm is applied for the total BCB thickness of 6 μm. The obtained BCB1 thicknesses from the process vary between 4.5 and 5.5 μm.

The simulation investigates three different BCB thicknesses: standard (5.5 μm) and deviations of ± 1 μm in a frequency range from 0 to 500 GHz. The analysis results show that the change in BCB1 thickness has a strong influence to the S_{11} parameter. By varying the BCB1 of ± 1 μm the S_{11} degrades from -38 dB to -28 dB. But this deviation has only minor influence on $|S_{21}|$ as illustrated in Figure 5.11 (top).

The insertion loss is increased around 0.25 dB when decreasing the gap between Gd and G1 by 1 μm. Deviation in the opposite direction, i.e. increasing the dielectric distance between these two metal layers, does not have a big influence on the insertion loss.

Figure 5.11: The influence of BCB1 thickness variation of ± 1 µm on the S-parameters of two flip-chip transitions (back-to-back) from 3D EM simulation.

5.4.6 BCB2 Thickness (dielectric between G1 stripline and G2 top ground layer)

For the influence of the dielectric thickness (BCB2) between G1 and G2 metal layer, very similar results as for BCB1 are obtained from the S-parameter simulations. By changing the thickness of V2 by ± 1 µm, stronger effects can be observed in S_{11} but not in S_{21}. Nevertheless, with the modification of the mentioned dielectric thicknesses, the worst-case return losses are still greater than 35 dB.

Figure 5.12: The influence of BCB2 thickness variation of ± 1 µm on the S-parameters of two flip-chip transitions (back-to-back) from 3D EM simulation.

5.4.7 Diamond Thickness

The nanocrystalline-diamond wafers used in this work reveal supplier-related wafer-to-wafer thickness variations as well as limited uniformity across a wafer. Typically, the diamond wafers received from the provider have thicknesses between 9 and 11 µm. But in some cases, the thickness of one wafer can vary from 8 to 15 µm. With the non-mask V2 BCB etching step with SF_6 plasma, the diamond surface is also affected. As a result, the total diamond thickness after the BCB etching process can be decreased by 1 or 2 µm. Typical diamond thicknesses before and after this etch step are summarized in table 4.1.

As presented in the 3D EM simulation of Figure 5.13, a deviation of the diamond thickness of ± 3 µm exhibits no major change of the transition quality, especially not of the insertion loss. Comparing the dielectric thickness of BCB1 and BCB2, it is clear that the distance between Gd and G1 is much closer to the distance between G1 and G2, therefore the thickness of this BCB1 is much more critical than the thickness of BCB2 and the diamond layers.
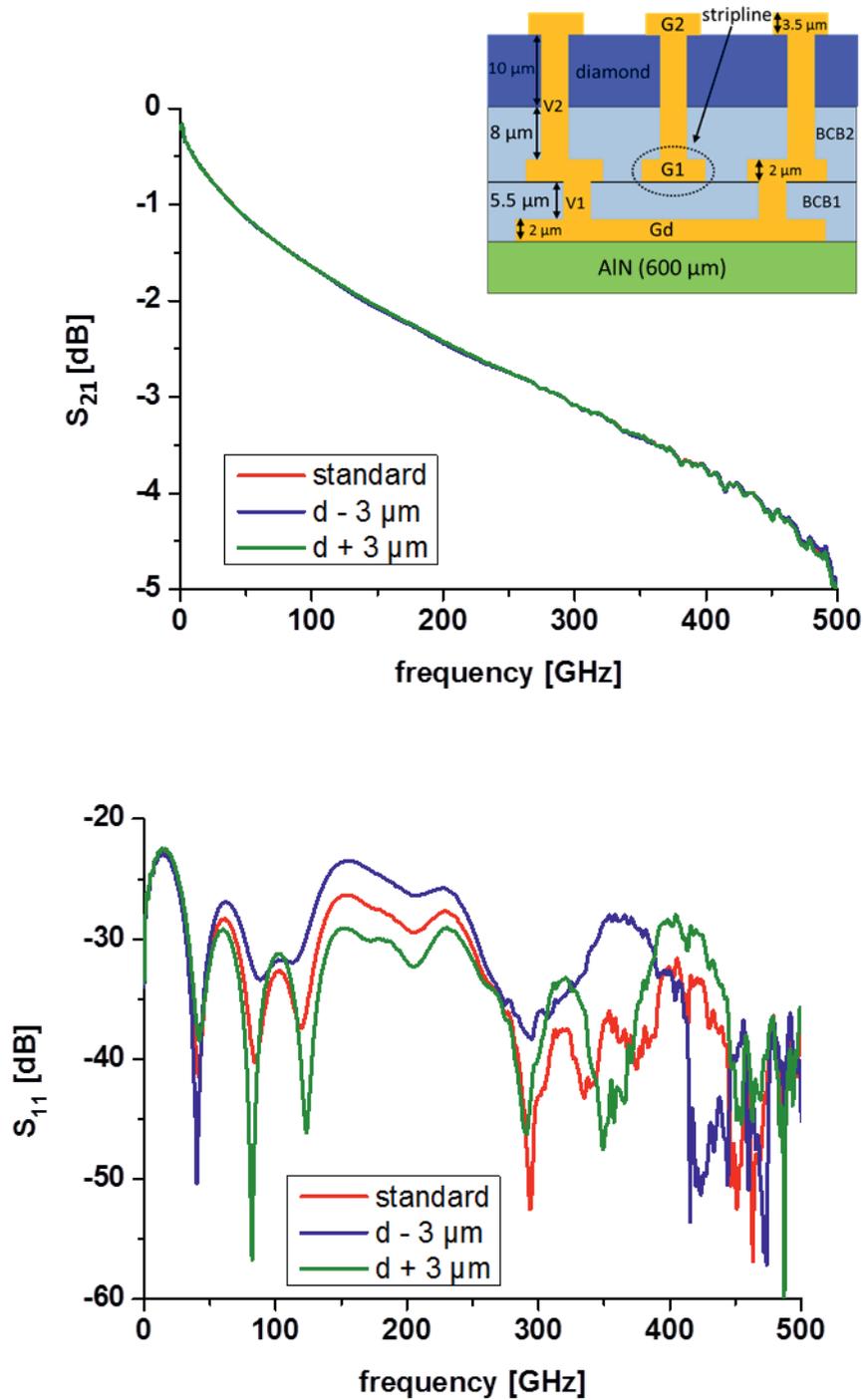
Figure 5.13: The influence of diamond thickness variation d ±3 μm on the S-parameters of two flip-chip transitions (back-to-back) from 3D EM simulation.

Chapter 6

Active InP HBT Amplifier Flip-Chip Assembly

In this chapter, the first attempt of flip-chip technology for InP MMICs with diamond heat sink and CPW line systems on the submount is demonstrated. The microbump flip-chip used in this interconnect was 10 μm in diameter, consisting of a multilayer eutectic AuSn (80% wt. Au and 20% wt. Sn). An AlN ceramic was selected as substrate due to its high dielectric constant. The CPW lines were defined by 3.5 μm thick Au plating technology. The substrate front-end process was taken from existing technology from the previous experiments of chapter 3. The diamond InP HBT chip was in-house fabricated using the transfer substrate technology as described in [9]. The CPW lines on the submount were designed to match the circuit footprint of the chip side. The results of two devices, which are 1) power amplifier and 2) tripler will be presented in the following.

Power Amplifier (90 GHz)
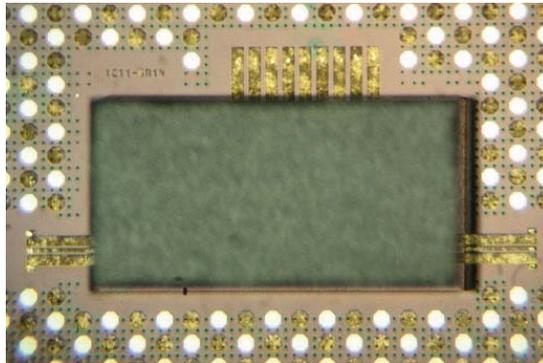
Figure 6.1: Top-viewed photograph of flip-chip power amplifier module on AlN carrier substrate.

A two-stage power amplifier, containing in total six transistors based on a 2-finger design with an emitter size of 0.8 x 6 μm^2, was mounted on an AlN carrier substrate using flip-chip technology in the same fashion as in the previous chapters. The photograph of mounted power amplifier module is shown in Figure 6.1. Figure 6.2 shows the measurement results of the diamond heat-sink InP HBTs, comparing between an unmounted chip and a flip-chip bonded device.
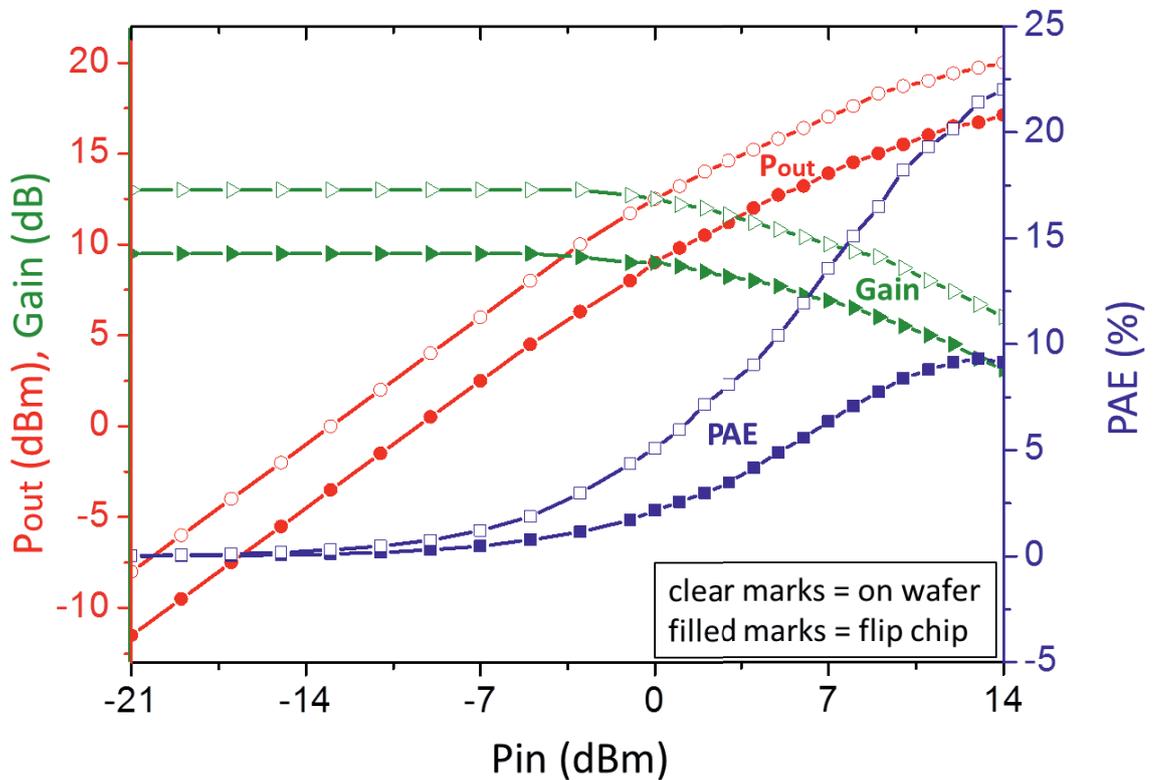
Figure 6.2: Large-signal measurement results of flip-chip power amplifier module, comparing between an on-wafer version and the flip-chip mounted MMIC.

From these results at the P_{in} of 13 dBm, the on-wafer chip obtained an output power P_{out} of 19.7 dBm, gain of 6.7 dB and the power added efficiency PAE of 21.42%, while the assembled power amplifier produced the P_{out} value of 16.7 dBm, the gain of 3.7 dB and the PAE of 9.32%. The measurement results are summarized in Table 6.1. It is clearly observed from the measurement results that after flip-chip mounting, P_{out}, PAE and gain of the device are lower than the unmounted chip.

Measurement	On-wafer chip	Flip-chip
P_{out}	19.7 dBm	16.7 dBm
PAE	21.42%	9.32%
Gain	6.7 dB	3.7 dB

Table 6.1: Summary of the measurement results of on-wafer and flip-chip power amplifier at P_{in} = 13 dBm

The possible root cause of the lower power values obtained after the flip-chip bonding is the 1 μm BCB layer on the substrate. This BCB layer is applied in order to planarize the rough AlN surface and to ensure good quality of the stepper marks. As it has already been mentioned in Chapter 3 that the strong wet chemical etching and a long plasma etching time exert an influence on the AlN substrate material. The cross-sectional structure of this additional BCB coating is demonstrated in Figure 6.3 (left).
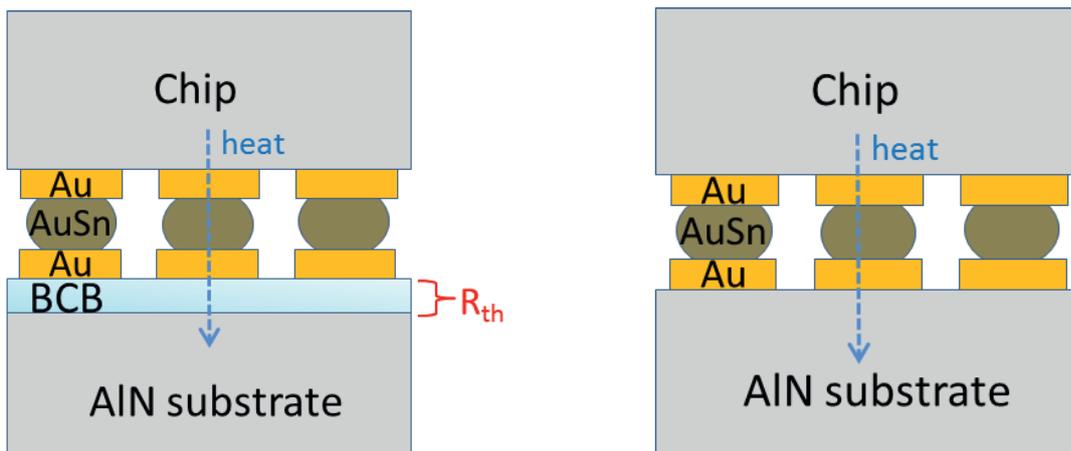
Figure 6.3: Cross-sectional structure of the flip-chip bonding with the BCB planarization on the AlN surface (left) and the flip-chip bonding without the BCB planalization.

However, with this BCB layer, which has a poor thermal conductivity of 0.29 W/m·K, an additional thermal resistance (R_{th}) occurs in the heat-transfer path between thermal bumps and AlN carrier. This thermal resistance R_{th} from the BCB can be described in the following equation.

$$R_{th} = \frac{d}{k \cdot A} \tag{6.1}$$

where,

R_{th} = thermal resistance of BCB (K/W)

d = thickness of the BCB (m)

k = thermal conductivity of BCB (0.29 W/m·K)

A= area of heat dissipation, perpendicular to the direction of heat dissipation (m^2)

To demonstrate the approximate model of the heat dissipation due to the BCB layer, only the metal area under the thermal bumps, which is in this model equal to 0.08 mm^2, is considered as the heat dissipation area (A). The applied BCB thickness is 1 μm. Hence, $R_{th\text{-}BCB}$ can be calculated as below.

$$R_{th\text{-}BCB} = \frac{1\,\mu m}{(0.29\,W/m\cdot K) \times (0.08\,mm^2)} \tag{6.2}$$

$$R_{th\text{-}BCB} = 431.03\,K/W \tag{6.3}$$

The power dissipation can be determined by:

$$P_{Diss} = P_{DC} + P_{in} - P_{out} \tag{6.4}$$

From the above equation, there are two parameters, which still need to be determined. These are P_{Diss} and P_{DC} . The P_{DC} is the relation of P_{out} , P_{in} and PAE as shown in the following equation.

$$PAE = \frac{P_{out}\text{-}P_{in}}{P_{DC}} \tag{6.5}$$

From the measurement results in Figure 6.2, at the P_{in} value of 13 dBm (= 19.95 mW), the obtained P_{out} value is 16.7 dBm (= 46.77 mW), and the PAE is 9.3%.

Hence,

$$P_{DC} = \frac{46.77\text{-}19.95}{9.3\%} \text{ mW} \tag{6.6}$$

$$P_{DC} = 288.39 \text{ mW} \tag{6.7}$$

By adding the values of P_{DC}, P_{in} and P_{out} in equation 6.4, P_{Diss}, can, then, be calculated to be

$$P_{Diss} = 288.39 + 19.95 - 46.77 \text{ mW} \tag{6.8}$$

$$P_{Diss} = 261.57 \text{ mW} \tag{6.9}$$

As can be seen from the calculation, the planarization BCB is the cause of additional thermal resistance, which is the parameter affecting the power dissipation P_{Diss} of the system. The relation of the P_{Diss} to R_{th} can be written as:

$$P_{Diss} = \frac{\triangle T}{R_{th}} \tag{6.10}$$

From [9], one finger transistor of the same type of diamond InP HBT has the R_{th} of 1.1 K/mW. From this information, the temperature inside the transistor can be defined by

$$\triangle T = P_{Diss} \times R_{th} \tag{6.11}$$

Since this power amplifier contains 6 transistors, therefore the P_{Diss} of one single transistor is

$$\frac{261.57 \text{ mW}}{6} = 43.594 \text{ mW} \tag{6.12}$$

The temperature inside the transistor can be calculated, by substituting the R_{th} of single finger transistor (1.1 K/mW) and P_{Diss} of one single transistor (43.595 mW) in equation 6.11. Hence, the temperature inside the transistor is

$$\triangle T_{HBT} = (43.594 \text{ mW}) \times (1.1 \text{ K/mW}) = 47.95 \,°\text{C} \tag{6.13}$$

With the additional BCB of 1 μm the temperature outside the transistor can be determined by substituting the total P_{Diss} and the $R_{th\text{-}BCB}$ in equation 6.11.

$$\triangle T_{BCB} = 261.57\,mW \times 431.03\,K/W \tag{6.14}$$

$$\triangle T_{BCB} = 112.74\,°C \tag{6.15}$$

This means that the BCB layer creates the additional temperature outside the transistor of 112.74 °C, leading to a total junction temperature in the considered system of

$$\triangle T_{BCB} + \triangle T_{HBT} = 112.74\,°C + 47.95\,°C = 160.69\,°C \tag{6.16}$$

The junction temperature rise of 160.69 °C against room temperature is quite high. This leads to gain reduction in both amplifier stages. The total output power is reduced by the same ratio as the gain is reduced. The output power cannot be increased further even with higher input power, because the first amplifier stage is then driven into saturation. In order to increase the P_{out} , gain and PAE of the power amplifier, the BCB under the metal area should be removed as shown in Figure 6.3 (right).

Multiplier (246 GHz Tripler)

As a second example, a tripler circuit based on a 2-finger transistor with an emitter size of 0.8 x 10 μm² was flip-chip mounted. This flip-chip module delivers - 13 dBm at 246 GHz as shown in Figure 6.5. Even though test results at wafer-level are not available as a reference, it is assumed that the tripler is not likely to be affected by the non-working thermal bumps, because its circuit does not consume as much total power as the amplifier mentioned above.
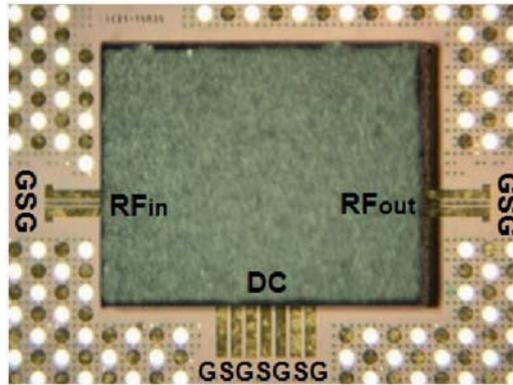
Figure 6.4: A photograph of 246 GHz flip-chip-mounted tripler (top view).
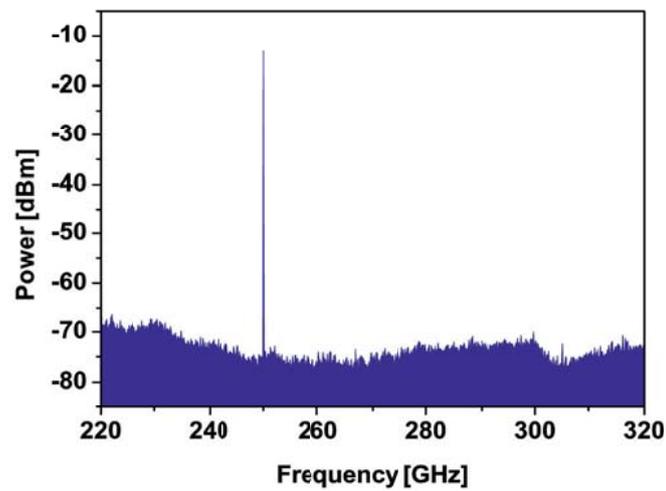
Figure 6.5: The measurement result of 246 GHz flip-chip-mounted tripler chip.

Chapter 7

Summary and Outlook

In this dissertation, an interconnect concept for sub-mm wave packaging has been demonstrated. Flip-chip technology was found to be a very good technology for ultra high-frequency applications in this area.

In chapter 3 the least-complicated planar transmission lines CPW-to-CPW structures together with the in-house miniaturized eutectic AuSn bumps (diameter $< 10 \, \mu m$) were demonstrated from DC up to 220 GHz, which is almost the maximum frequency for this line system. The RF characterization of the flip-chip interconnects revealed a low transition loss of less than 1.0 dB per transition at 200 GHz. This results confirm that the AuSn flip-chip technology is a very suitable packaging solution for mm-wave applications.

Chapter 4 presents the successful development of AuSn microbump flip-chip interconnect for frequency above 250 GHz using a stripline-to-CPW structure. The RF measurement of the back-to-back test modules at 250 GHz indicate an insertion loss below 1.0 dB per interconnect after subtracting of the line loss, and a return loss of more than 10 dB. Beyond 250 GHz, the interconnect shows a strong effect of radiation losses from the CPW lines on the carrier substrate. However the characterization showed that the designed interconnect still functions up to 325 GHz. This means that a more suitable line system could be applied to a carrier substrate to further increase the bandwidth.

Therefore, in the third iteration in chapter 4, instead of using CPW lines on the substrate, the stripline is introduced on the submount as well, keeping the vertical construction of the chip to be the same. However, the lateral design on the chip side needs to be adjusted ac-

Dimensions/ Designs	CPW-CPW	Stripline-CPW	Stripline-stripline
Frequency (GHz)	220	350	500
Signal width (µm)	15	9	9
Total structure length including pads (µm)	2450	1700	2470
Line length on chip (µm)	1700	800	160
Chip material	AlN (600), SiO$_2$ (500)	AlN (600)	AlN (600)
Substrate material/ thickness (µm)	AlN (600)	AlN (600)	Silicon (350)
BCB thickness chip (µm)	-	BCB1 = 6 BCB2 = 12	BCB1 = 5.5 BCB2 = 8
BCB thickness substrate (µm)	-	-	BCB1 = 8 BCB2 = 8
Diamond thickness (µm)	-	10	10
smallest via diameters (µm)	-	20	10
AuSn bump diameter (µm)	10	10	10
Diced chip dimension (mm^2)	2 x 2	1.5 x 2.0	1.2 x 1.5
Diced substrate dimension (mm^2)	10 x 10	10 x 10	10 x 10

Table 7.1: Details of dimensional structures of all flip-chip passive devices in this dissertation

cordingly and aligned to the submount patterns. The results show that with the appropriate transmission line types, line dimensions and bump sizes, the passive elements can function up to 500 GHz with a total insertion loss of 5 dB and a reflection loss of > 20 dB. This corresponds to the insertion loss of 1 dB per interconnect. At the time of this writing, the 500 GHz results denote a new state-of-the-art in flip-chip assembly.

Table 7.1 summarizes dimensional structures of each flip-chip design. More details about the fabrication process can be seen in chapters 3-5 .

In chapter 6, the CPW-to-microstrip flip-chip approach was used to assemble active InP HBT MMIC with integrated diamond heatsink onto AlN RF carrier substrate with a targeted bandwidth of 250 GHz. Since the active devices contain power amplifiers (PA), doubler and trippler and only require frequency below 250 GHz, the use of CPW on the PCB submount is adequate. The measurement results confirm that the technology works excellently also for the active devices. Nevertheless, the following research aspects should be considered in future work.

1. From the 500 GHz structures, the shielding is done at most of the structures using striplines and vias as mentioned previously. Nevertheless, to increase the operating frequency using the design based on this structure one could add more shielding to the structures. One way to achieve more shielding is to close the circular opening at the transition areas. By doing so, EM radiation is limited when going to higher frequencies. However, the characteristic impedance at this position will be changed since the capacitance is increased. Therefore, it is important also to adjust the BCB thickness between Gd and G1 layer. Possibly more BCB thickness is required.

2. In order to increase the reliability of flip-chip for different materials with different thermal expansion values, underfill materials should be implemented. Materials such as polyimide or BCB could be used as underfill materials [114].

3. Different bump materials can be further investigated in order to lower the bonding temperature. This would reduce the total thermal budget of chips. In term of processing, an alternative deposition process can be investigated, for example, to use AuSn electroplating instead of AuSn evaporation. This can eliminate problems from lift-off technology and save expensive materials.

4. The problem of submount housing of 500 GHz bandwidth needs to be addressed. Prospective studies of this topic could be expanded to molding systems to protect whole devices. Furthermore, from the production point of view, the reliability test of packages should be investigated in order to confirm the reliability of flip-chip technology for high-frequency devices.

Publications

Parts of this dissertation have been published:

1. S. Monayakul, C.-T. Wang, O. Krueger, N. Weimann, 'Design, Fabrication, and Characterization of Miniaturized AuSn Flip-chip Transitions up to 110 GHz', *WOCSDICE*, page 21-22, 2013.

2. S. Monayakul, S. Sinha, C.-T. Wang, N. Weimann, F. J. Schmueckle, M. Hrobak, V. Krozer, W. John, L. Weixelbaum, P. Wolter, O. Krueger, and W. Heinrich, '250 GHz Flip-chip Interconnect Module', *IEEE Microwave Component Wireless Letter (MWCL)*, vol. 25, no. 6, pp. 358-360, 2015.

3. S. Monayakul, S. Sinha, F. J. Schmueckle, M. Hrobak, D. Stoppel, O. Krueger, B. Janke, N. G. Weimann, 'Process Robustness and Reproducibility of sub-mm Wave Flip-Chip Interconnect Assembly', *Proc. EPEPS 2015*, San jose, USA, October 2015.

4. S. Sinha, S. Monayakul, M. Hrobak, R. Dörner, F. J. Schmueckle, N. Weimann, V. Krozer and W. Heinrich, 'Theory, design and characterization of broadband terahertz interconnects', *IEEE MTT Journal,* submitted.

5. N. Weimann, K. Nosaeva, S. Monayakul, V. Krozer, M. Lisker, B. Tillack, 'Transferred substrate InP DHBT processes for mm-wave applications', *Micro- and Millimetre Wave Technology and Techniques Workshop ESA-ESTEC*, The Netherland, 2014.

Award

***Best Oral Paper Award* from Electrical Performance and Electronic Packaging System (EPEPS)**, San jose, California, USA, October 2015

Paper: S. Monayakul, S. Sinha, F. J. Schmueckle, M. Hrobak, D. Stoppel, O. Krueger, B. Janke, N. G. Weimann, 'Process Robustness and Reproducibility of sub-mm Wave Flip-Chip Interconnect Assembly', *Proc. EPEPS 2015*, San jose, USA, October 2015.

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