# 1 Introduction

## 1.1 Motivation

We are currently living in an era of a rapidly developing technology. As a matter of fact, devices have to be faster, i.e. able to work in the higher frequency range. There is a demand for integrated circuits at frequencies up to 300 GHz and even higher for satellite communication, radars, spectroscopy, and imaging.

To realize the circuits for millimeter-wave and submillimeter-waves, the technology for fabricating the power amplifiers (PA), low-noise amplifiers (LNA), voltage controlled oscillators (VCO) and passive components have to be developed and established at a reasonable price. Therefore, the development of terahertz monolithic integrated circuits (TMICs) will revolutionize circuits and systems in the frequency band from 0.3 to 3 THz. It will enable the widespread adoption of new applications including active imagers and sensor arrays, where compact monolithically integrated circuits are the key to realizing the required element spacing and dense functionality [1].

Recent technological advances of InP-based devices have pushed the transistors bandwidth towards and even beyond 1 THz.

Indium Phosphide (InP) high-electron-mobility transistors (HEMTs) have attained bandwidth >1.2 THz at 50 nm gate length [2]. InP heterobipolar transistors (HBTs) have attained bandwidth >1 THz with 250 nm emitter length and lower [3], [4], [5]. The high $f_{max}$ of these devices could be achieved due to high electron velocity in the InP material. Another advantage is a high bandgap, that leads to the breakdown voltage >4 V for InP-based devices. However, HBTs have key advantages over InP HEMT that enable complex MMICs. Given their high breakdown voltage, high digital speed, InP HBTs provide a platform in which all receiver and transmit components (LNA, VCO, and mixer) can be constructed. Single-chip construction eliminates THz waveguide connections between circuit blocks. This greatly reduces package size and interconnecting losses that currently limit the performances of THz blocks.

Silicon-germanium (SiGe) HBTs in bipolar complementary metal oxide semiconductor (BiCMOS) technology are also able to work with $f_{max}$>200-300 GHz. Each of the high frequency technologies mentioned above have advantages and shortcomings depending on the targeted application. Due to their unique material properties, InP-based devices have a higher breakdown voltage (>4 V) than BiCMOS devises based on Si, but lower or comparable with GaN RF HEMTS (3-18 V), as can be seen from Table

1. Bipolar transistor cutoff frequencies are increased by scaling of device dimensions, with transit delays $\tau_b$ and $\tau_c$ reduced by thinning the epitaxial base and collector, and with an RC charging delay reduced by shrinking the emitter and base-collector junction widths, by reducing contact resistivity, and by increasing the emitter current density [3]. The cutoff frequency of HEMTs is increased by shortening the gate length. An advantage of SiGe HBTs over InP DHBTs is a lower microwave noise. However, due to their higher gain, advanced InP/InGaAs DHBTs are expected to have advanced noise performance at frequencies beyond 50 GHz, and therefore could be used for RF low-noise amplifiers (LNA) design at mm- and sub-mm wavebands.

A lot of efforts have been included into materials and device development of group III-nitride electronics to push toward the limits of cutoff frequency, breakdown voltage, power density and reliability of GaN HEMTs. GaN (thermal conductivity 130 W/m·K) transistors grown on SiC substrates (thermal conductivity 360 W/m·K) have enabled high power amplifiers with high power added efficiency (PAE) that have significantly higher output power and power density than is presently available from amplifier circuits based upon GaAs or InP materials. Moreover, SiC is an excellent heat sink. The improvements of performance available due to material characteristics of GaN that allow high electron sheet charge densities in transistor channel and very high electrical breakdown fields. InAlN/AlN/GaN HEMTs with a gate length in the 30-50 nm range [6], [7] performance in the frequency over 300 GHz are only a few examples .

**Table 1: Comparison of state-of-the art mm-wave technologies**

| $f_t$ (GHz) | $f_{max}$ (GHz) | $V_{CEO}$ (V) | $L_E \times W_E$ ($\mu m^2$) | Power density ($mW/\mu m^2$) | Technology | Institution | Ref. |
|---|---|---|---|---|---|---|---|
| 404 | 901 | 4.3 | 0.18×2.7 | 42 | InGaAs/InP DHBT | UCSB[1] | [8] |
| 480 | 1070 | 4.1 | 0.2×2.9 | 32.8 | InGaAs/InP DHBT | UCSB[2] | [3] |
| 520 | 1100 | 3.5 | 0.13×2 | 50 | InP DHBT | Teledyne[1] | [4] |
| 320 | 325 | 4 | 0.7×4 | 10.5 | InP/InGaAs/InP DHBTs | IAF[2] | [9] |
| 430 | 1030 | >4 | 0.25×4 | 19.8 | InP HBT | Teledyne[2] | [5] |
| 470 | 540 | 6.5 | 0.38×5 | 3.3 | Type-II DHBT | University of Illinois Urbana-Champaign | [10] |
| 429 | 715 | >5 | 0.3×4.4 | 12.7 | Type-II InP/GaAsSb DHBT | ETH-Zürich[1] | [11] |

**Table 1: continued**

| $f_t$ (GHz) | $f_{max}$ (GHz) | $V_{DS}$ (V) | $L_q \times W_q$ (µm²) | Power density (mW/µm²) | Technology | Institution | Ref. |
|---|---|---|---|---|---|---|---|
| 503 | 780 | 4.1 | 0.2×4.4 | 10 | GaAsSb-Based DHBTs | ETH-Zürich[2] | [12] |
| 603 | 305 | 4.2 | 0.3×11.5 | 2.47 | InP/GaAsSb/InP DHBTs | ETH-Zürich[3] | [13] |
| 410 | 330 | <2 | 0.5×4 | <12 | InP DHBT | Bell Labs | [14] |
| 400 | 350 | | 0.8×5 | 10.8 | InP DHBT-on-BiCMOS | FBH[1] | [15] |
| 410 | 480 | >5 | 0.8×5 | 10.4 | TS InP DHBT | FBH[2] | [16] |
| 300 | 500 | 1.6 | $W_E$=0.25 | | SG25H1 BiCMOS | IHP[1] | [17] |
| 273 | 423 | 1.5 | 0.11 × 4.9 | 7.5 | B4T BiCMOS | STMicroelectronics[1] | [18] |
| 240 | 380 | 1.5 | 0.13×2.7 | 6 | IFX B7HF200 | Infineon Technologies | [19] |
| 260 | 400 | 5 | 0.10×4.9 | 9.1 | BiCMOS9MW | STMicroelectronics[2] | [19] |
| 310 | 480 | 1.75 | 0.155 × 1 | 25.5 | SiGe:C HBT | IHP[2] | [20] |
| 215 | 400 | 1.7 | 0.08 × 0.9 | 13.1 | G1G SiGe HBT | IMEC | [19] |
| 515 | >1000 | | - | | mHEMT | IAF[1] | [21] |
| 385 | 1200 | - | - | - | InGaAs/InAlAs/InP HEMT | Northrop Grumman | [2] |
| 688 | 800 | - | - | - | $In_{0.7}Ga_{0.3}As$ MHEMTs | Teledyne | [22] |
| 710 | 478 | - | - | - | InAs HEMT | National Chiao-Tung University, Taiwan | [23] |
| 644 | 681 | - | - | - | InAs PHEMT | Microsystems Technology Laboratory | [24] |
| 80 | 192 | 15 | 2×0.1×25 | 2.5 | GaN-on-Silicon HEMT | IEMN/CNRS | [25] |
| 124 | 230 | 18 | 0.1 | 2 | AlGaN/GaN HEMT | UCSB[3] | [26] |
| 270 | 230 | 10 | 2×0.05×50 | 2.5-4 | InAlN/AlN/GaN HEMT | TriQuint Semiconductors | [27] |
| 359 | 347 | 5 | 0.03 | 2.6 | InAlN/AlN/GaN HEMT | TriQuint Semiconductors | [6] |
| 342 | 518 | 14 | 0.07 | - | GaN-HEMTs | HRL Laboratories | [28] |
| 310<br>454 | 582<br>444 | 3 | 0.02 | - | GaN-HEMTs | HRL Laboratories | [7] |

For InP (thermal conductivity 16.1 $W \cdot m^{-1} \cdot K^{-1}$ [29]) DHBTs, the limiting material is InGaAs (thermal conductivity of InAlAs 10.5 $W \cdot m^{-1} \cdot K^{-1}$ [29]). We chose the InP DHBTs technology to realize power amplifiers for mm-wave width band. But it is necessary to spread the heat away from the operated areas of

the device during operation. Perfect ability to conduct heat (with a thermal conductivity of up to 1000 $W \cdot m^{-1} \cdot K^{-1}$ for thin layers) and low dielectric losses make diamonds one of the best candidates for mm-wave applications. Moreover, commercially available thin diamond film grown by chemical vapour deposition (CVD) or ultrananocrystalline diamond (UNCD) gives the possibility to embed a diamond film into semiconductor chip's layer stack using a substrate transfer process, for example. The diamond thin films have a smooth surface, which is important for the integration into the process, reduction of thermal scattering in the film for thermal management, and for eliminating the internal stress in the devices.

Diamonds could be integrated using the following methods:

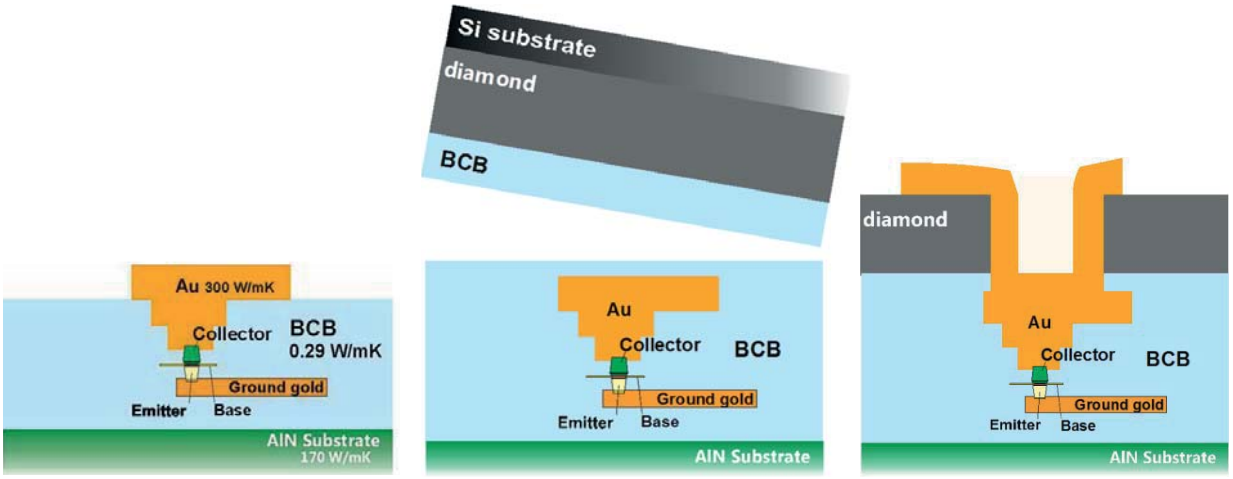
1. Bonding of the diamond heat-spreaders.
2. Submount (pick and place).
3. Diamond wafer scale integration by diamond direct growth [30],[31],[32],[33].
4. Near junction heat spreading [34], [35], [36], [37], [38], [39].

Other substrates with higher thermal conductivity could be used to improve the heat sink as well. Additional research shows improvement of the thermal resistance of devices using transferred substrate technology by transferring to high thermal conductivity silicon substrate [40], for example.

Another area, where the interest of diamond was and still is wide, is a power electronics based on diamond. Potentially, diamond is a perfect material for a high power electronics with material breakdown field of 10 M·V/cm [41]. The major challenges to realize devices based on diamond are cost of diamond growth, small substrate size, difficulties in the processing and lack of dopants.

## 1.2 Scope of the dissertation

My thesis covers the transfer of the diamond heat-sink onto $0.8\times 5\ \mu m^2$ InP DHBTs fabricated with a transferred substrate (TS) process, which was developed at the Ferdinand-Braun-Institute during the last 10 years [16],[42]. Using of a TS technology helps optimize high-frequency performances of InP DHBTs by the reduction of the collector area and the replacement of the extrinsic InP collector material with BCB [43]. This results in a significant reduction of the extrinsic base-collector capacitance. However, the important limit of InP DHBTs processed in TS technology lies on the thermal effects, because BCB is a poor heat conductor. Hence the dissipated heat needs to be effectively removed from the transistor. It was established using a 10 µm thick diamond layer.




a) b) c)

**Figure 1: a) Schematic of embedded in BCB InP DHBT, fabricated with a transferred-substrate process; b) Schematic of a BCB adhesive wafer bonding of Diamond-on-Silicon Substrate onto TS layer-stack; c) Schematic of an integrated diamond layer and fabricated thermal via to collector for heat spreading.**

The schematic of the integration of a diamond heat-spreading layer is shown in Figure 1. The BCB adhesive wafer bonding process was used for diamond transfer followed by subsequent removal of a silicon host substrate mechanically and chemically. Afterwards the heat bridges out of the collector into the diamond spreading layer were established

The mechanical and thermal properties of the diamond-on-silicon substrates used in this work are presented in Chapter 2. The possibility as well as challenges to use these substrates for diamond transfer using the adhesive BCB wafer-to-wafer bond process is described.

The definition and methods for measurements and extraction of HBTs thermal resistance is presented in Chapter 3. It allows describe numerally the improvements of the heat sink using diamond layer.

To transfer the diamond layer on top of the InP HBTs layer stack the development of bonding technology with following interconnection through the diamond and BCB to establish the electrical and thermal connection. It is necessary to develop the diamond transfer process described in Chapter 4. It includes adhesive wafer bonding and via etch holes process with following vias electroplating. The development of critical new process modules was conducted on test wafers which included passive RF and DC structures.

Chapter 5 describes the integration of diamond into the full InP HBT MMIC process. The characterization of diamond InP HBTs was done by using measurement of interconnection resistance, DC and RF

characteristic of processed transistors. The thermal resistance has been measured and extracted using DC measurement and developed extraction method.

In Chapter 6, the results are summarized and an outlook for future work given in Chapter 7.

# 2 Diamond substrate properties

## 2.1 Characterization of chemical vapor deposition (CVD) and ultrananocrystalline diamond (UNCD)

In the InP HBT transferred substrate technology, BCB is used for adhesive wafer bonding. A similar BCB bond process could be used for integration of diamonds into an InP layer stack. The issue of BCB's low thermal conductivity (0.3 W/m·K) can be circumvented with vertical metal connections serving as thermal vias, connecting the transistor's contact leads to the diamond heat spreading layer. To realize it, the diamond-on-silicon substrates must satisfy the following criteria:

- thickness less than 10 µm for integration with existing microstrip achieving thermal conductivity >300 W/m·K,
- insulating to fit the process and functioning of devices,
- diameter of wafer is at least 3 inch,
- low loss tangent (tan δ) to minimize losses during high-frequency operations,
- optical transparency for possibility to make lithography alignment to the underlying layers,
- low tensile stress,
- low roughness for bonding processes,
- low wafer bow for subsequent processing.

There are different methods to grow the synthetic diamond on silicon substrates [44], [45], [46], [47]. Chemical vapor deposition (CVD) is one of the most popular, well-established as well as commercially available method to grow diamond [48]. The first reproducible synthesis of artificial diamond with a process requiring high temperature and high pressure was reported by the General Electric Company in 1955 [49]. It involves chemical reaction of different selectable process gases on the growth substrate in the reactor. However, mostly methane ($CH_4$) is used for diamond growth as a precursor gas diluted in hydrogen ($H_2$) in a typical mixing ratio of 1% (see Figure 2). The substrate temperature during the diamond growth is bigger than 700 °C to prevent the formation of amorphous carbon. Atomic hydrogen reacts with or etches graphite about 20-times faster than diamond, so graphite and other non-diamond phases are rapidly removed from the substrate. Also $H_2$ stabilizes the diamond surface converting the hydrocarbons into radicals, a necessary precursor for diamond formation. Other reactants gases could be added to the chamber for different reasons. For example, the addition of oxygen to the reaction gases has a

beneficial effect on the growth rate and quality of the CVD diamond films allowing for diamond growth to occur at low temperatures.

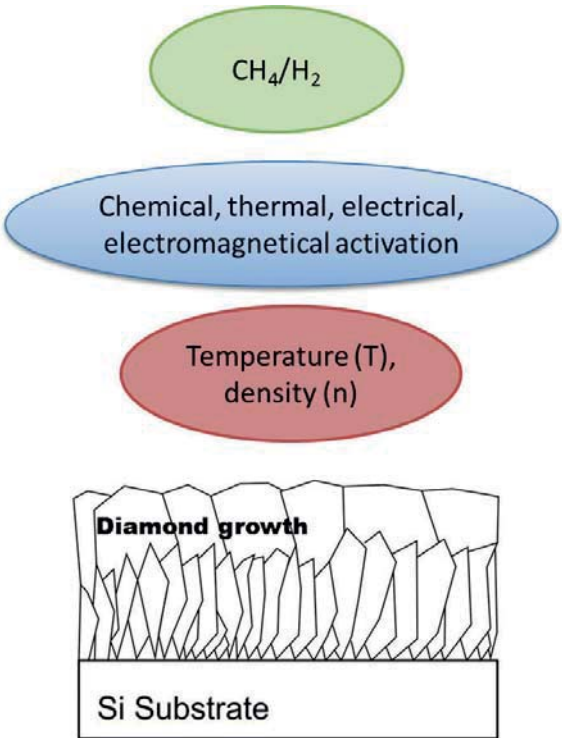



**Figure 2: Schematic diagram of the mechanism from CVD processes for diamond growth**

The various diamond CVD techniques differ mainly in the way of gas phase activation and dissociation. The most common techniques are microwave-plasma-assisted CVD and thermally- assisted CVD, usually realized by gas activation with a hot filament. The distinguishing features are the deposition rate, the deposition area and the quality of the deposited diamond. The maximum growth rate reported so far amounts to almost 1 mm/h. However, those high growth rates are usually limited to very small deposition areas (<< 1 $cm^2$). In general, there is an inverse relationship between film quality and growth rate. Optically transparent films with high thermal conductivities are usually deposited at rates not exceeding 10 µm/h, regardless of the deposition technique.

One type of thin film nanocrystalline diamond used in this work is CVD diamond-on-silicon, grown by Diamond materials GmbH (**DM**). The grain size of such material could reach 7 µm for 10 µm thick layers. A novel microwave plasma CVD technology is used. An ellipsoidal cavity focuses the microwave energy

into intense and extended plasma, resulting in a large area homogeneous deposition and long-term plasma stability enabling growth of thicker films.

The second type of diamond material used here is the so called ultrananocrystalline diamond, grown also on 3" silicon substrates. Nanocrystalline diamond films are readily grown by any of the conventional diamond CVD processes as well as CVD diamond, but the grain size of the final layer is noticeably smaller (from nano-range to micro-range). This material was grown by Advanced Diamond Technology (**ADT**) Company using the microwave CVD plasma deposition technique involving $CH_4$/Ar chemistry.

**Table 2: Overview of diamond properties**

| Property | Diamond Materials GmbH, Germany | Advanced Diamond Technology, USA |
|---|---|---|
| **Thermal expansion coefficient, α** | $1.0\times10^{-6}$/K @300K | $1.0\times10^{-6}$/K @300K |
| **Resistivity** | $10^{13}$-$10^{16}$ Ωcm | $10^{3}$-$10^{4}$ Ωcm |
| **Loss tangent at 40 Hz** | 0.0006 | 0.0006 |
| **Loss tangent at 140 GHz** | $<10^{-5}$ | $<10^{-5}$ |
| **Thermal conductivity** | 450 (calculated for 10µm) | 1500 (theoretical) |

### 2.1.1 Mechanical properties

*"There are three things extremely hard: steel, a diamond, and to know one's self."*

*Benjamin Franklin*

Diamond is one of the hardest materials and has exceptional wear resistance and a low coefficient of friction. Some of its mechanical properties are shown in Table 2 [50].

Normal deposition processes of 1-2 µm of UNCD film exert -200 to -300MPa of residual stress (compressive) on the Si wafer. As a consequence, the wafers with a 10µm thick film have a bow from -40 µm to -80 µm. The CVD diamond film exerts tensile stress. In this case, the wafers have a bow from 20 µm to 60µm after polishing. The stress could be explained due to differences of thermal expansion

coefficients of diamond ($1.0\times10^{-6}$/K) and silicon ($2.56\times10^{-6}$/K) as a host substrate and high deposition temperatures.

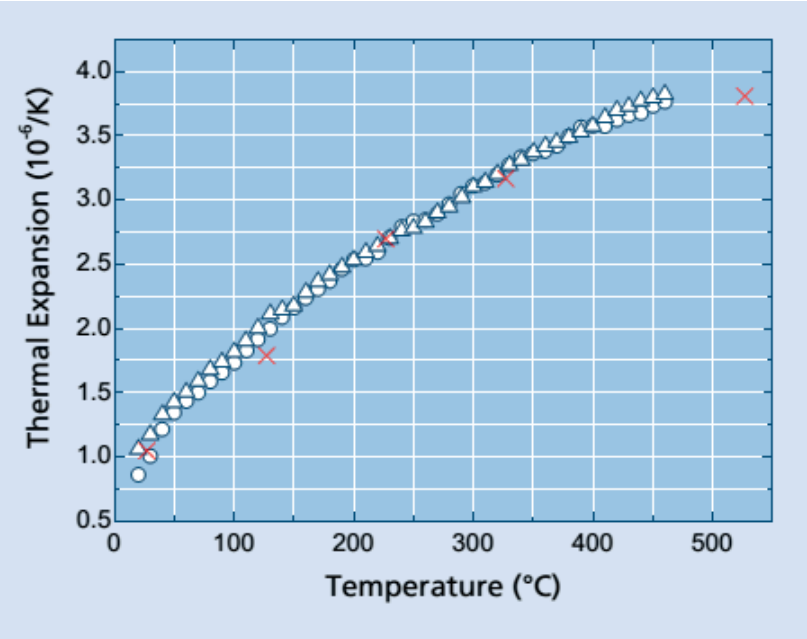



**Figure 3: Thermal expansion coefficient in dependence of temperature** [50]

### 2.1.2 Surface characterization

The surface characterization of diamond layer for both types (CVD&UNCD) has been done as grown and after the polishing process has been obtained. The scanning electron microscop (SEM) images of polished and unpolished surfaces are shown in Figure 4.