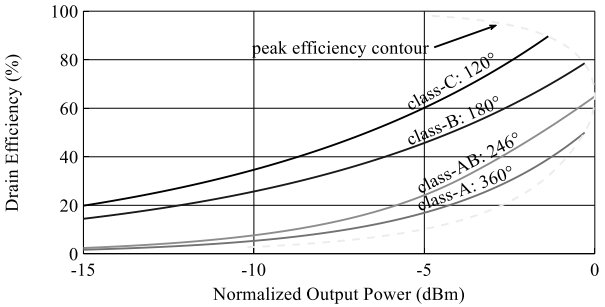
1 Introduction

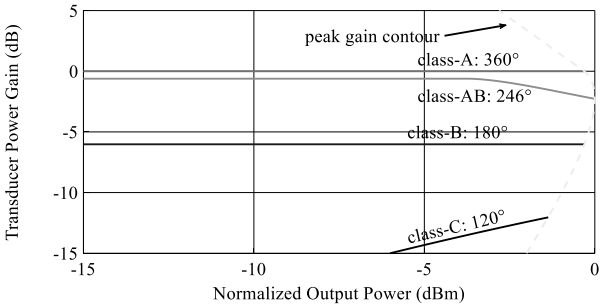
The worldwide power consumption of telecommunication networks is rapidly growing due to the steadily increasing demand on broadband internet access. With an estimated annual growth rate of over 10% and an estimated total power consumption of 257 TWh in 2012 [1], telecommunication networks contribute significantly to the worldwide power consumption. In line with this, broadband wireless data access is rapidly developing towards higher bandwidth, with a continuously growing amount of mobile subscriptions and mobile traffic [2]. For the required wireless transmission of data, a modulated radio frequency (RF) signal must be generated and amplified by an RF power amplifier (PA) to provide the output power that is high enough to compensate for the immense path-losses in a wireless transmission link, in which the attenuation scales with the square of the distance [3] - even for optimum free-space conditions. Therefore, an RF PA is needed in each base station transmitter and it is a key component when it comes to system efficiency: The RF PA consumes 50-80% of the total energy and is therefore the most power-hungry part in a base station [4]. The PA must fulfill the linearity requirements to avoid emission outside the specified RF band, since the frequency spectrum is densely utilized, and to allow transmission with low bit-error rates. This suggests operating the PA in a linear regime where it is guaranteed that also the highest power peaks are amplified without driving the PA into compression. The need for high data throughput and a high number of users demands for a structured and efficient utilization of the RF spectrum with modulation schemes that provide high spectral efficiency. In communication standards like long-term-evolution (LTE), which belongs to the 4th generation (4G) wireless networks, and the future 5G technology, orthogonal frequency-division-multiplexing (OFDM) is used for modulating the downlink channel, i.e., the transmission link from the base station to the mobile handset. For OFDM modulated signals the peak-to-average power ratio (PAPR), i.e., the ratio between peak power and average transmitted power, is usually very high [5]. The PAPR increases with the number of modulated subcarriers [6], which makes the design of broadband systems even more challenging. High PAPR requires the operation of the PA in power back-off to maintain linearity. PA architectures like class-A and class-AB [7] are significantly losing efficiency when operated at power back-off. For a class-A this is caused by the fact that the drain-source current is constant while the output power (P_{OUT}) is reduced. Simulations of the drain efficiency vs. power back-off for ideal PAs of different operation classes are shown in Fig. 1.1 (a). The

efficiency drops rapidly for all PA classes with conduction angles above 180°, i.e., class-A to -B. For conduction angles above 180° the efficiency increases, but the gain decreases rapidly under power back-off, which is plotted in Fig. 1.1 (b). A good trade-off between gain and back-off efficiency is found in the class-AB range.

Fig. 1.2 shows the simulated drain efficiency at power back-off for different supply voltages and a class-AB PA. The efficiency can be improved in output power back-off by reducing the supply voltage of the PA. This is the key point which most supply modulation techniques are based on: Whenever the PA is operated at an output power below its maximum level, the supply voltage is decreased to achieve an increase in efficiency. In envelope tracking (ET) topologies the supply voltage is modulated with the envelope of the modulated RF signal. In contrast to the Kahn envelope elimination and restoration (EER) approach, the RF input of the PA is still driven with the modulated signal and contains phase- and amplitude information. The supply modulation can be implemented either analog with continuous supply-voltage modulation or with discrete supply voltage levels. In this work, the discrete level supply modulation is referred to as class-G supply modulation. The class-G modulator is in principle a multilevel switch which selects between two or more fixed supply voltages. This thesis investigates theory, design, and operation of such systems.



(a)



(b)

Fig. 1.1: Theoretical (a) drain efficiency and (b) transducer power gain for different conduction angles/amplifier classes vs. output power normalized to the peak output power. The transducer gain is normalized to the gain of a class-A PA.

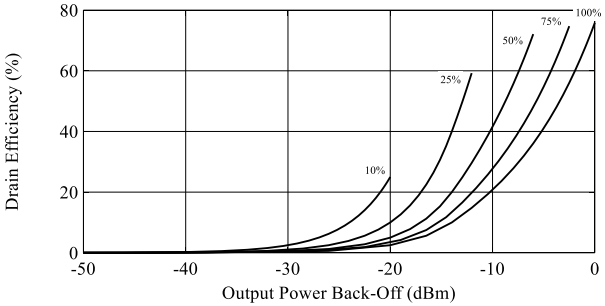


Fig. 1.2: Simulated drain efficiency vs. power back-off of a class-AB PA, when adjusting supply voltage (curve parameter denotes % of maximum supply voltage).

2 Theory of Class-G Supply Modulation

Class-G supply modulation is a discrete-level supply voltage modulation technique, in which the supply voltage of a PA is switched between discrete levels. If the PA is operated with a modulated RF signal, the supply voltage is switched according to the envelope of the modulated signal. Class-G supply modulation is a relatively young concept that was first introduced for low frequency audio applications in 1976 [8]. The adoption of the class-G supply modulation for RF applications was first proposed in [9] and the first RF PA systems with class-G modulation where published in 1995 [10]. It was shown that class-G modulation works well in the RF domain, and that a high efficiency improvement can be achieved. In the initial work on class-G the linearity degradation was not the main focus, since most systems were based on integrated silicon circuits. In general, there were not many publications available on the topic at the beginning of this thesis work in 2014, especially for PA architectures based on gallium nitride (GaN) semiconductors. This has been changed by the achievements presented in this thesis. Nowadays, class-G modulation is a competitive solution which shows performance that compares well with other state-of-the-art efficiency-enhancement techniques.

In the following the concept of class-G supply modulation is discussed in detail. First, the efficiency and transducer gain of a linear PA is analyzed under the conditions of variable power back-off and supply voltage levels, but with a fixed load (R_L). The behavior of the RF PA in relation to these parameters is crucial for the design of highly efficient supply modulated systems and, which is shown in this work, has proven to be a very complex issue. This first design step is usually done based on continuous wave (CW) load-pull measurements or simulations. It is important to know that, due to memory and thermal effects, the CW-based analysis does not exactly fit the behavior of the class-G PA system under dynamic operation, as it was shown in [11]. Nevertheless, the information obtained is useful to understand the effects of the various parameters of the system. Furthermore, the data can be used for simulations to investigate system performance and limitations while considering the effects of the bandwidth and amplitude distribution of the IQ modulated signal. This chapter is divided into three thematic parts. First the efficiency and linearity of a PA at power back-off is evaluated to investigate which amplifier class is best suited for class-G modulation. In the second part the dynamic requirements for the class-G supply modulator are investigated to find out how many supply voltage levels to use and which maximum switching frequency is required for a specific IQ modulation bandwidth and targeted efficiency enhancement. The

last part discusses the limitations in efficiency enhancement for the class-G modulation topology.

2.1 Supply modulation of linear and reduced conduction angle power amplifiers

The efficiency of linear and reduced conduction angle PAs, particularly class-A to class-C, depends on the instantaneous output power of the PA. It decreases with lower output power levels, as shown in Fig. 1.2. When a modulated signal with dynamic envelope amplitude is applied to a PA, the average efficiency is degraded since the average output power must be decreased to avoid overdriving the PA at the peak power levels. Therefore, the PAPR of the amplified signal is a very important property from a PA point of view. For a complex-valued signal vector $\underline{x}$, the PAPR (in dB) is defined by:

$$\mathrm{PAPR} = 10 \cdot \log_{10}\left(\max\left(\left|\underline{x}\right|^2\right)\right) - 10 \cdot \log_{10}\left(\mathrm{mean}\left(\left|\underline{x}\right|^2\right)\right) \qquad (1)$$

The PAPR determines the average power back-off that is required to drive the PA in a linear range, without clipping the maximum signal amplitudes. This is visualized by Fig. 2.1, which shows the time domain envelope- and RF power signals of a class-A PA. The gray shaded area represents the total dissipated energy. It can be concluded, that low envelope power levels significantly contribute to the total dissipated energy.

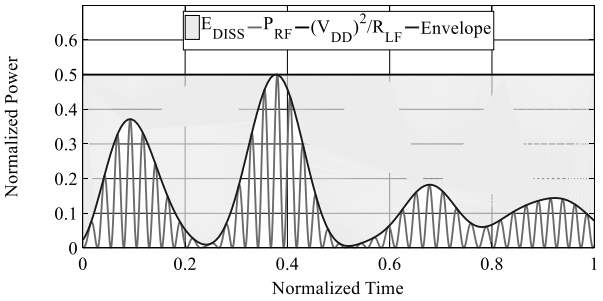


Fig. 2.1: Time domain signals of envelope- and RF power for a constant supply voltage. The dissipated energy is equivalent to the gray shaded area (simplified illustration).

In the following study, the possible performance enhancement of supply modulation and its impact on the PA characteristics are investigated. Therefore, the power back-off behavior of linear power amplifiers is analyzed for reduced supply voltages. Thereby it is considered

that R_L is constant (no simultaneous load modulation is applied). The variation of the supply voltage causes a mismatch regarding optimum PAE or P_{OUT}. To investigate this effect, the theory of the reduced conduction angle power amplifier classes [7] is expanded to investigate the power back-off behavior as function of the DC supply voltage levels. For this purpose, the PA is evaluated as a four-port device, two RF ports (p1, p2) and two low frequency (LF) ports (p3, p4), as shown in Fig. 2.2. The RF signal is fed into p1 and the amplified signal is obtained at p2. The supply modulator is connected at the port p3 and provides the DC to LF modulated supply voltage and current. In the first analysis, the LF port p4 is set to a constant bias level, resulting in a simplified three port representation of the PA which is also used in the literature [18]. Later in this chapter the port p4 is also modulated which allows dynamically controlling the quiescent bias point synchronously with the DC supply voltage which can be beneficial for some PA classes.

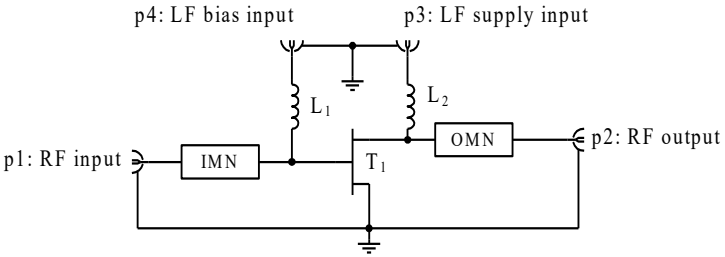


Fig. 2.2: Schematic of the supply modulated PA ports. L_1 and L_2 are RF-chokes, IMN and OMN the input- and output matching networks.

The following part is divided into four subsections: First the reduced conduction angle theory is introduced for supply modulated PAs, based on idealized conditions. Thereby the behavior of the different amplifier classes at power back-off with reduced supply voltage is investigated and the suitability for supply modulation is discussed. In the second part, the influence of discretized supply voltage levels, which represents the case of class-G supply modulation, is investigated. The third part addresses the knee I-V effects based on a quasi-static GaN-HEMT model and compares the result to the theoretically derived values. In the last part the linearity is considered, and the influence of supply modulation is discussed for continuous- and class-G supply modulation.

2.1.1 Power back-off efficiency with continuously reduced supply voltage

In continuous supply modulation the supply voltage of the PA (LF port p3) is adjusted with the envelope amplitude as shown in Fig. 2.3. The comparison to the constant supply

voltage case shown in Fig. 2.1 reveals that the area of dissipated energy is reduced significantly.

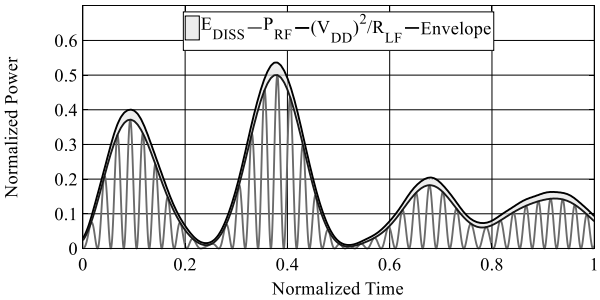


Fig. 2.3: Time domain signals of envelope- and RF power for a continuously modulated supply voltage (simplified illustration).

The analysis is based on an idealized model, where the saturated drain-source current is linearly dependent on the gate-source voltage. The load impedances are all set to be resistive. The drain-source current and -voltage are normalized to their maximum value (I_{DS_MAX}) and V_{DS_MAX}, respectively. In Fig. 2.4 (a) the load-line for a class-A PA is shown for operation with a resistive load and a normalized DC supply voltage (V_{DS_DC}) of 0.5. The conduction angle (α) of the drain-source current is 360°, which makes the drain-source voltage $v_{DS}(t)$ linearly dependent on the drain-source current $i_{DS}(t)$. In this case the PA operates linearly and the load line slope R_{LL} is constant (2) and identical to the load resistance R_L (3):

$$\frac{dR_{LL}}{dt} = \frac{d}{dt}\frac{v_{DS}(t)}{i_{DS}(t)} = 0 \quad , \alpha \geq 360 \tag{2}$$

$$R_L = R_{LL} \quad , \alpha \geq 360 \tag{3}$$

For lower conduction angles, the drain-source current is clipped at a level of zero to avoid negative current values. This causes the generation of harmonics. In the reduced conduction angle theory, the fundamental is terminated by a fixed resistance (R_{L1}) and all other harmonics are terminated by a short [7]. Therefore, the amplitude of the AC output voltage ($\hat{v}_{DS\_AC}$) depends only on the amplitude of the fundamental drain-source current ($\hat{\imath}_{DS\_AC1}$) and R_{L1} (4). This causes the load-line slope to differ from R_{L1} if other harmonics are present (5).

$$\hat{v}_{DS\_AC} = \hat{i}_{DS\_AC1} \cdot R_{L1} \tag{4}$$

$$R_L \neq R_{LL} \quad , \alpha < 360 \tag{5}$$

When supply modulation is applied, the load-line is shifted horizontally, since R_L is constant and the quiescent drain-source current (I_{DSQ}) is independent of V_{DS_DC}. The shift of the load-line and the quiescent bias points with supply voltage is shown in Fig. 2.4 (b) for the class-A case.

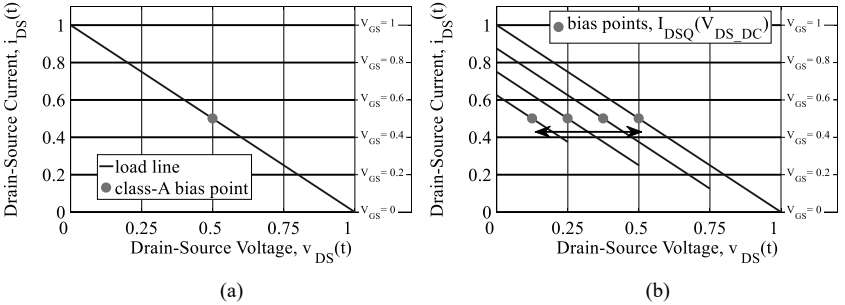


Fig. 2.4: Idealized transistor DC output characteristics with (a) class-A load-line and (b) load-line shift with DC supply voltage reduction.

For the class-A condition shown it is observed that the drain-source current is not excited over its full range and the current AC/DC ratio is reduced. This is caused by the fixed load impedance and the reduced supply voltage and is also valid for other PA classes. With the definition of $v_{DS}(t)$ in (6) the maximum value $\hat{i}_{DS\_AC1}$ can be calculated, based on two conditions. First (7) must be true to avoid negative values of $v_{DS}(t)$ and second (8) must be fulfilled to ensure that $v_{DS}(t)$ does not exceed V_{DS_MAX}. For maximum output power, V_{DS_DC} must be operated in the range from 0 to 0.5, therefore, (8) is not a limitation during operation with reduced V_{DS_DC}.

$$v_{DS}(t) = V_{DS\_DC} - \hat{i}_{DS\_AC1} \cdot \cos(\omega_1 t) \cdot R_{L1} \tag{6}$$

$$\hat{i}_{DS\_AC1}(V_{DS\_DC}) \leq \frac{V_{DS\_DC}}{R_{L1}} \quad , \frac{1}{2} \geq V_{DS\_DC} \tag{7}$$

$$\hat{i}_{DS\_AC1}(V_{DS\_DC}) \leq \frac{1-V_{DS\_DC}}{R_{L1}} \quad , \quad \frac{1}{2} \leq V_{DS\_DC} \tag{8}$$

The limitation of $\hat{i}_{DS\_AC1}$ causes several effects in the supply modulated PA: The maximum output power (P_{OUT_MAX}) becomes dependent on the supply voltage as defined in (9). It scales quadratically with the supply voltage, resulting in a V_{DS_DC} dependent reduction of the maximum output power (P_{OUT_BO}) with a decay of −20 dB/dec (10). Additionally, the efficiency of the PA classes with positive quiescent current ($I_{DSQ} > 0$ A; class-AB to class-A) reduces, since the DC supply current (I_{DS_DC}) does not scale linearly with $\hat{i}_{DS\_AC1}$ (derivation of I_{DS_DC} and $\hat{i}_{DS\_AC1}$ in appendix 9.1). This results in a V_{DS_DC} dependent drop of the DC power consumption at an output power back-off level (P_{DC_BO}) (11) of less than −20 dB/dec. The worst case is a class-A PA, where P_{DC_BO} decreases with only −10 dB/dec, since I_{DS_DC} is constant, independent of V_{DS_DC} ($I_{DS\_DC} = I_{DSQ}$). A possible solution for the class-A case is the modulation of the gate-source bias port (p4) to reduce I_{DSQ} simultaneously with V_{DS_DC}, which is discussed in Chapter 2.1.3. By combining (10) and (11) the drain efficiency at power back-off (η_{D_BO}) in dependency of the peak drain efficiency (η_{D_MAX}), i.e., η_D at maximum supply voltage and output power, is derived in (12). The DC to LF impedance at power back-off (Z_{LF_BO}), seen at port p3, is seen by the supply modulator and, therefore, an important parameter for the design of modulators. The impedance is defined by the fraction of V_{DS_DC} and the current I_{DS_DC} (13). Due to the dependency between V_{DS_DC} and P_{OUT_BO} in (10), Z_{LF_BO} is linearly dependent on the back-off drain efficiency η_{D_BO}.

$$P_{OUT\_MAX}(V_{DS\_DC}) = \frac{\hat{i}_{DS\_AC1}(V_{DS\_DC})^2 \cdot R_{L1}}{2} = \frac{V_{DS\_DC}^2}{2 \cdot Z_{L1}} \tag{9}$$

$$P_{OUT\_BO}(V_{DS\_DC}) = 10 \cdot \log_{10}\left(\frac{P_{OUT\_MAX}(V_{DS\_DC})}{P_{OUT\_MAX}(1)}\right) = 20 \cdot \log_{10}(V_{DS\_DC}) \text{ (dB)} \tag{10}$$

$$P_{DC\_BO}(V_{DS\_DC}) = 10 \cdot \log_{10}\left(\frac{I_{DS\_DC}(V_{DS\_DC})}{I_{DS\_DC}(1)}\right) + \log_{10}(V_{DS\_DC}) \text{ (dB)} \tag{11}$$