1 Introduction

Research in high-speed transistors is driven by applications in imaging and wide band communication. The long-term aim is to open up the “terahertz gap” – the almost unutilized range between optics and electronics from 0.1 to 3 THz of the electromagnetic spectrum. This range of millimeter und submillimeter wavelength provides wider bandwidth, improved spatial resolution, and concealed objects can be made detectable due to specific absorption and transmission properties [1]. Imaging systems are projected in medical, security and industrial inspection [2]. The atmospheric attenuation windows at 94, 140, 220 and 340 GHz allow for high-resolution radar assistance in fog, dust or smoke [3]. Further applications are in wireless high bit-rate and secure short-range communications [4].

Recent advances of InP heterojunction bipolar transistors (HBT) with several hundred gigahertz operating frequencies qualify them for key components in such systems e.g. for amplifier stages and local oscillators. Compared to SiGe bipolar transistors, they achieve higher bandwidth at less demanding scaling nodes and attain higher breakdown voltage at a given device bandwidth.

These advantages originate from the high electron mobility of the InGaAs base [5], [6], larger valence band separation of the emitter–base heterojunction and thus increased base doping up to the epitaxial limit of incorporation [7], as well as higher peak electron velocity and breakdown field of the InP collector [8], [9]. Silicon on the other hand scores with high quality native oxide, important for device passivation. Table 1.1 summarizes key material parameters of selected semiconductors.

TABLE 1.1

MATERIAL PROPERTIES OF SELECTED SEMICONDUCTORS AT $T = 300$ K.

	Si [10]	Ge [10]	GaAs [11]	InP [12]	$In_{0.53}Ga_{0.47}As$ [6]	GaN [13]
bandgap (eV)	1.12	0.66	1.42	1.35	0.75	3.4
hole mobility (cm^2/Vs)	450	1 800	400	140	300	30
electron mobility (cm^2/Vs)	1 450	3 900	8 500	4 600	12 000	1 000
electron peak velocity ($\times 10^7$ cm/s)	1	0.6	2	2.5	3	3.1
breakdown field (V/µm)	30	10	40	50	20	500

Nevertheless III-V technologies face constant pressure from silicon roadmaps [14]. The more than fifty years of collaborative efforts in developing Si processes and equipment not only result in lower cost and much higher scales of integration, but also is able to partly compensate for superior material properties available in compound semiconductors. To stay ahead, InP HBTs require continued development and adaptation in terms of device scaling together with surface passivation and yield as well as improved contact and thermal resistances. Up to now, SiGe HBTs of $0.12 \times 2.5\,\mu m^2$ emitter area have demonstrated highest current gain cutoff frequency $f_T = 300\,GHz$ and maximum oscillation frequency $f_{max} = 350\,GHz$ at collector current $I_C = 5.7\,mA$ and breakdown voltage $BV_{CEO} = 1.7\,V$ [15], [16], while $0.8 \times 5\,\mu m^2$ InP HBTs of this work feature $f_T = 420\,GHz$ and $f_{max} = 450\,GHz$ at $I_C = 27\,mA$ and $BV_{CEO} > 4.5\,V$. The InP HBTs of $0.8\,\mu m$ minimum feature size are far from their scaling limit, and operating frequencies beyond one THz appear to be feasible in Chapter 7 by scaling down the transistors.

In the lower range of high frequency operation, InP transistors compete with GaN high electron mobility transistors (HEMT) in terms of power performance [17]. Record GaN HEMTs of 60 nm gate length and $2 \times 50\,\mu m$ width show peak values of $f_T = 190\,GHz$ at drain−source voltage $V_{DS} = 4\,V$ and $f_{max} = 240\,GHz$ at $V_{DS} = 10\,V$, with maximal drain−source currents $I_{DS}{}^{max} = 160\,mA$ [18], [19]. Within this work, first triple finger InP HBTs of $3 \times 0.8 \times 9\,\mu m^2$ emitter area simultaneously demonstrate an $f_T = 320\,GHz$ and $f_{max} = 340\,GHz$ at $V_{CE} = 2.1\,V$ with maximum collector current $I_C{}^{max} > 270\,mA$ – even though epitaxy was not optimized for power performance. In the end, the key arguments of low cost and very high yield for SiGe HBTs as well as the superior power handling capability of GaN HEMTs fade when aggressively scaled to approach high frequency performance of InP transistors.

In recent years, InP-based HEMTs as well as HBTs demonstrated highest operating frequencies [20], [21], [22], [23]. Each device concept has its applications, where its specific set of technology metrics excels over the other. For instance, HBTs are preferred for millimeter-wave oscillators. They feature very reproducible DC parameters scalable by epitaxial design rather than lithographic layout, superior transconductance and linearity, lower phase noise, but higher overall noise figure. HEMTs on the other hand are suited e.g. for low-noise amplifiers.

In this work, InP double heterojunction bipolar transistors (DHBT) have been developed in transferred substrate technology (TS) to optimize high frequency performance. The 3" wafer-level process provides lithographic access to both, front- and backside of the transistors, aligned to each other. Thus, emitter and collector contact are scalable in proportion to each other, independent of the base width. The resulting linear device set-up eliminates dominant transistor parasitics and relaxes design trade-offs. The essential step for gaining frontal access to both sides of the epitaxial DHBT structure is the substrate transfer procedure. Along with the innovative TS DHBT set-up, the three-dimensional (3D) integration of passive elements and operational components on the transfer wafer supports functionality of the active devices and paves the way towards highly functional composite electronics, e.g. of wafer-level, 3D heterogeneous integrated circuits. The TS approach is concordant with the ITRS trend line, favoring double side processes in the future to push the limits beyond conventional device performance: "… the ultimate MOSFET is projected to be the multiple-gate device" [24]. Corresponding processes are currently explored for Si-based transistors [25], [26].

Chapter 2 introduces the DHBT concept and TS device topology. The relevant figures of merits are identified. Device design is discussed in detail to assess key limiters and optimize transistor performance by the TS approach. The technological aspects of this work are presented in Chapter 3 – from epitaxy design and mask set layout to device processing. Process modules specific to the TS technology are motivated and described in detail. The fabricated transistors are evaluated and benchmarked in Chapter 4 in terms of yield, DC, RF and power performance. Large and small-signal models are derived for parameter extraction and circuit design. Chapter 5 reports on monolithic microwave integrated circuits (MMIC) results – from the conception of passive elements to the realization of complete circuits in TS technology. Chapter 6 summarizes the work and Chapter 7 briefly discusses advanced process modules for continued increase in bandwidth, assessing future TS DHBT capabilities, based on scaling laws, device results and models of this work.