Dimitri Stoppel (Autor)

Interconnection development for InP-HBT terahertz circuits

https://cuvillier.de/de/shop/publications/8230

Chapter 1

Introduction

1.1 Motivation

The world we live in today is dominated by the information technology of the 21st century. The growing demand for more bandwidth in communication enabled the commercialization of monolithic microwave integrated circuits (MMICs). But also other fields now can be accessed with the help of MMICs, e.g. in biology and medicine with the non-invasive blood glucose measurement, protein states, molecular signatures, tissue identification and disease detection [1, 2]. These and many other application have a huge demand for high frequency electronics. To exploit the possibilities for the next generation of electronics in the terahertz frequency (> 300 Ghz), it is necessary to develop and commercialize terahertz microwave integrated circuits (TMICs).

Promising candidates for active devices for TMICs are based on silicon germanium (SiGe), gallium nitride (GaN) and indium phosphide (InP) [3–5]. Groups across the world are researching fast switching devices for the next generation of MMICs.

SiGe heterobipolar transistors (HBTs) are the high frequency (HF) heritage of the classical silicon complementary metal-oxide-semiconductor (CMOS) transistors. In this technology it is possible to integrate both, HBTs and high-electron-mobility transistors (HEMTs) monolithically on one substrate. Most recent results show highest maximum unity current gain cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) at 300 and 500 GHz, respectively. Limited by the bandgap of silicon, the devices are have a comparable low breakdown voltage of around 1.5 V. With this technology scheme it is possible to apply the high integration capability of silicon and combine it with high bandwidth devices, which is an interesting aspect of this approach [5].

Another technology scheme is reaching from the high power area of GaN devices. The latest achievements with GaN HEMTs showing f_t, f_{max} of 400 and 550 GHz. The obvious focus of

Table 1.1 Comparison of state-of-the art mm-wave technologies

f_t [GHz]	f_{max} [GHz]	Breakdown [V]	$L_E/W_E[\mu m^2]$	Technology	Institution	Ref.
337	400	3	0.25x4	InP/GaAsSb HBT	NTT	[7]
360	330	4.5	0.8x6	InP/InGaAs HBT	FBH	[8]
270	750	5	0.25x6	InP HBT	NGAS	[9]
610	1500	3	0.025x10	InP HEMT	NGAS	[10]
428	621	5	0.2x4.4	InP/GaAsSb HBT	ETH	[11]
404	901	4.3	0.18x2.7	InP/InGaAs HBT	UCSB/Teledyne	[12]
400	550	15	0.02	GaN HEMT	HRL	[3]
521	1150	3.5	0.13x2	InP	Teledyne	[4]
300	500	1.5	0.13x2.69	SiGe HBT	IHP	[5]
245	450	1.7	0.15x1	SiGe HBT	IMEC	[13]

GaN transistors are the high power applications, due to the high breakdown voltage and the high power added efficiency (PAE).

Nowadays the fastest oscillation speed achieved with a transistor has been fabricated with the highest electron mobility material, indium gallium arsenide (InGaAs). f_t and f_{max} values of 610 and 1500 GHz have been extracted from measurements of an InP HEMT. With such high bandwidth devices, power amplifier (PAs) with 10 stages were measured at 1.0 THz with a gain of 9 dB [6].

At the Ferdinand-Braun-Institute (FBH) in Berlin, an unique technology approach is followed. Instead of the classical triple mesa transistor scheme with lateral devices, a transferred-substrate (TS) process is utilized to fabricate vertical devices. A vertical approach has the advantage, that it avoids the occurrence of the extrinsic base collector capacitance. Such an approach is possible, since the half finished transistor is transferred to a host substrate to access the collector from the backside. A second and important benefit is the opportunity to either use a substrate with high thermal conductive substrate or e.g. a fully processed bipolar junction transistor with complementary metal–oxide–semiconductor (BiCMOS) wafer [14], as seen in Fig.1.1. Both, the immense scalability of the HBTs and the 3D-integration enable the fabrication of next generation TMICs with high complexity and frequency.

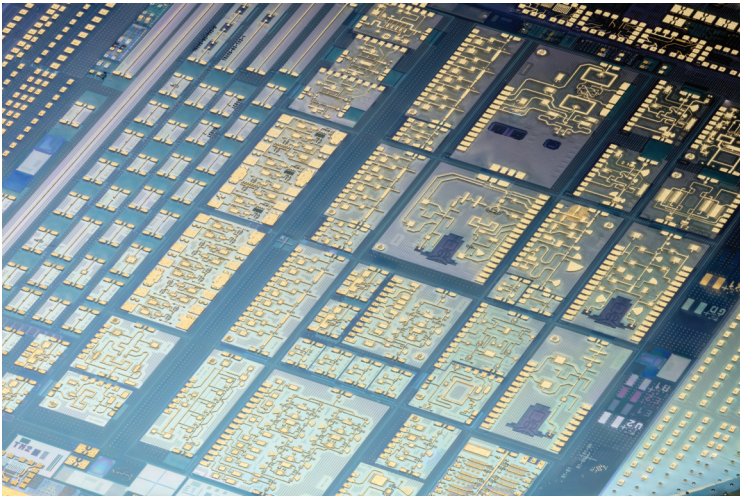

Figure 1.1 Macro photograph of a finished hetero integration wafer (BiCMOS and InP).

For TMICs and MMICs it is necessary to lower the process time to offer affordable circuits with a short design and fabrication loop time. Furthermore it is important to enhance the technology to enable a more complex topology more capabilities.

1.2 Scope of the dissertation

The scope of this dissertation is the improvement and further development of an TMIC process at the FBH. In chapter 1, the introduction for high frequency devices is established as it provides the motivation for this work. Chapter 2 provides a detailed description of the transferred-substrate process at the FBH. The subsequent three chapters show and explain the process developments that have been done to improve the process, constituting the main scientific achievements presented in this dissertation. In chapter 3, the process development for an improved plasma etch recipe is described, which decreases the process time significantly at maintained process quality. The development and implementation of thin film resistors (TFRs) fabricated with nickel-chrome (NiCr), is described in chapter 4. Aspects of process technology, thermal simulation, stress test, high frequency measurements and the usage in circuits are discussed. The third and last part of this thesis is covering the process development and integration of through-silicon vias (TSVs) in the TS process in chapter 5. The necessity thereof is demonstrated using high frequency simulations. Subsequently, the

detailed process development and the implementation into the process is covered. The sixth chapter provides a conclusion as well as an outlook into future work.

Chapter 2

InP HBT transferred-substrate process

2.1 Transferred-substrate process

The transferred-substrate (TS) process at the FBH is a unique method to create true vertical InP HBTs. Opposed to the classical triple mesa transistors, the TS process accesses the collector directly from the top due to the fact, that the device is flipped vertically.

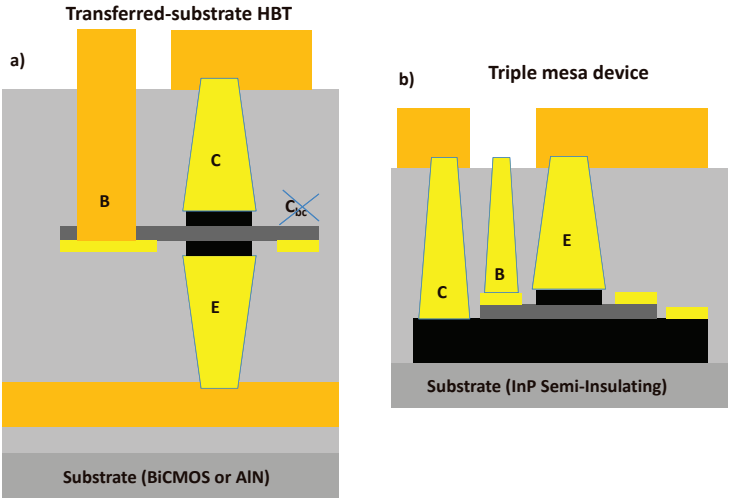

Figure 2.1 Comparison between the triple mesa and the transferred-substrate technology, a) transferred-substrate HBT, b) triple mesa HBT. Based on [14].

The parasitic collector base capacitance C_{bc}, which decreases the unity current-gain cutoff frequency f_t of a transistor, is eliminated in the TS process as seen in Fig.2.1. The extrinsic

C_{bc} is present in the triple mesa approach, while the TS process is released from that parasitic effect.

The common-emitter unity current-gain cutoff frequency f_t is,

$$\frac{1}{2\pi f_t} = \tau_c + \tau_b + C_{bc} \cdot (R_{ex} + R_c) + \frac{\eta kT}{qI_e}(C_{bc} + C_{je}) \tag{2.1}$$

where τ_c and τ_b are defined as collector and base transit times and C_{bc} and C_{je} standing for the depletion capacitances for the collector and emitter. R_{ex} and R_c are the collector and emitter resistances and the $(\eta kT/qI_e)^{-}1$ term is the transconductance of the transistor [15]. The maximum oscillation (unity power-gain) frequency f_{max} depends directly on f_t,

$$f_{max} = \sqrt{\frac{f_t}{8\pi(RC)_{eff}}} \tag{2.2}$$

where RC_{eff} is the base-collector time constant that includes the C_{bc} from Equ 2.1 and the R_{bb} which is the total sum of the base resistances [15]. By assuming that the base resistance is much larger than the emitter and collector resistances, their effect becomes negligible and only the base-collector path contributes to the $(RC)_{eff}$. With this assumption the f_{max} can be described as,

$$f_{max} = \sqrt{\frac{f_t}{8\pi(R_{bb}C_{bc})_{eff}}} \tag{2.3}$$

where R_{bb} and C_{bc} has the most impact on the f_{max} of the HBT. With the minimized C_{bc} in the TS process, the contribution to f_t and f_{max} is minimal. This paves the way for higher bandwidth InP HBT compared to the triple mesa transistor, at the same emitter width.

The minimized C_{bc} in the TS process is possible, due to the full wafer bonding procedure. In the middle of the TS process, the half finished HBT is transferred by adhesive wafer bonding to a host wafer. This wafer transfer facilitates the possibility to attach a non-processed host wafer like silicon (Si) or aluminum nitride (AlN) to the InP wafer. The more groundbreaking opportunity is to replace the host wafer with a fully processed BiCMOS wafer [8, 14]. With these technology schemes combined, it is possible to use the highly integrated silicon technology, so to say the brain with the muscles of the InP HBTs with the high breakdown voltage and the high frequency capability. With those technologies combined, it becomes possible to integrate not laterally but vertically (3D) e.g. voltage-controlled oscillator (VCO) with amplifier chains [14].

2.2 Process description

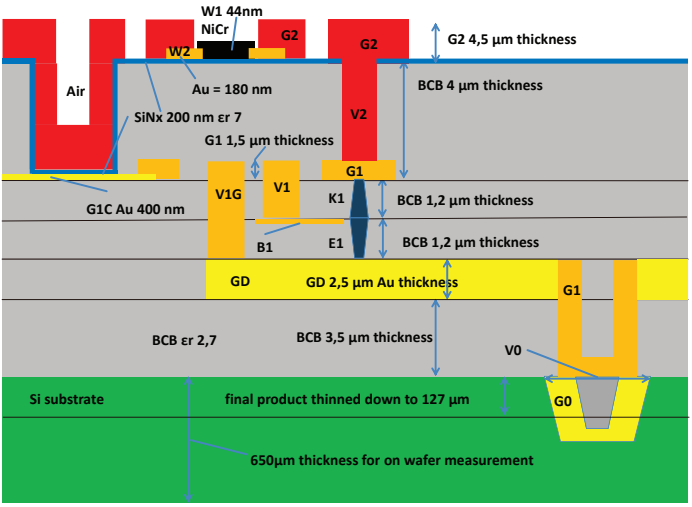

Figure 2.2 Cross section view of the TS process with a silicon host substrate with TSVs, which can be substituted by a BiCMOS wafer. Based on [16].

In the present status, the TS process contains three layers of electroplated gold metals (GD, G1 and G2) as shown in the Fig.2.2. These metals form the ground metal and connection to the emitter (GD), the first interconnects to emitter, base, collector, host substrate and capacitors (G1). The microstrip line, measurement and bond pads and the interconnects to the previous layers are connected with the last electroplated metal (G2). The process contains a metal-insulator-metal (MIM) capacitor with silicon nitride (SiNx) as dielectric material with a permittivity of $\varepsilon_r = 7$. A NiCr thin film resistor with a sheet resistance of 25 $\Omega/\square$ is integrated at the top layer. It is possible to integrate through-silicon vias into the host substrate to suppress parasitic substrate modes, that can occur after dicing the MMICs and mounting them into a system. The whole device and all its passive components and interconnects are embedded in benzocyclobutene (BCB). BCB has very good planarization capabilities, a high glass transition temperature of about 350 °C and with a ε_r of 2.65 it is a suitable material for high frequency applications [17].

The process begins with creating a mask layout. In the design phase the circuit designer utilizes either the extracted models of the active and passive components from a previous wafer run or an estimated model if e.g. a new epitaxy is tested. After combining all

components, the layout has to be exported. The finished mask layout is created according to the design rules and process bias based on the technology. An example for a final layout with more then 20 lithographic layers is shown in Fig.2.3. This layout contains all necessary components for a successful MMIC process, like process control monitoring (PCM) structures for metal contacts, sheet resistances and isolation measurements. The layout also includes all technology structures e.g. for step-height, alignment check and critical dimension (CD) measurements. To characterize the HF devices and passives, calibration structures are positioned in the layout. The most mask area is consumed by the end products (MMICs).

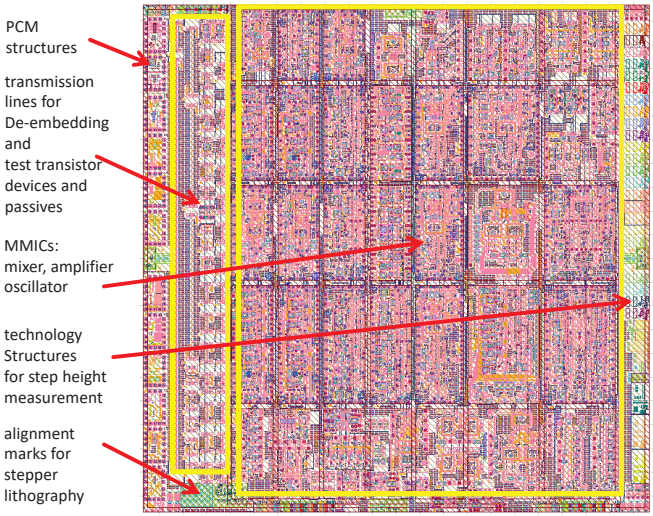

Figure 2.3 Layout example of an TS process with remarks on the content.

The transferred-substrate technology starts with the growth of the epitaxy on InP wafers. In the case of FBH, the epitaxy is ordered from a commercial supplier with following layers from bottom (substrate) to the top: two etch stops, sub-collector, collector, delta doping, grade, setback, base, emitter and emitter cap [18].

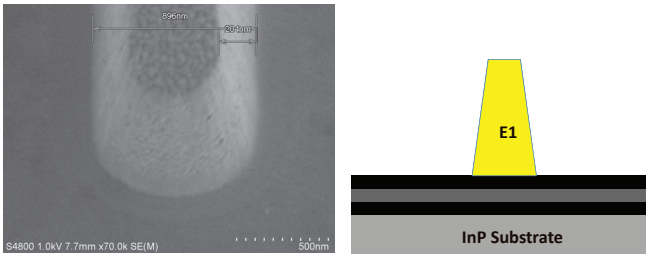

Figure 2.4 Illustration of the emitter process, a) SEM micrograph of a metalized emitter, b) cross-sectional sketch of the emitter.

The process starts similar to the conventional triple mesa process. As first lithography layer, the emitter contact metal is defined by the lift-off technique (E1). The emitter metal sets an ohmic contact to the highly doped emitter cap with extra metal to increase the distance between the forthcoming ground metal and the base as seen in Fig.2.4. The applied metal also serves as an etch mask to structure the emitter semiconductor. With that mask, the emitter cap (InGaAs) is wet etched by sulfuric acid and emitter (InP) by hydrochloric acid. Both acids are highly selective etchants to the target material. With the structured emitter semiconductor, the base contact surface is revealed and the isotropic etch mechanism creates a necessary undercut of circa 50 nm for the following step.

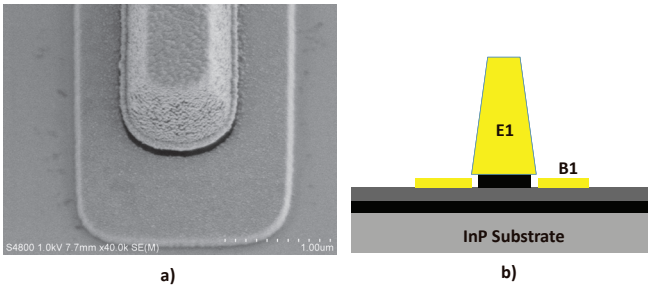

Figure 2.5 Illustration of the self-aligned base process, a) SEM micrograph of a metalized base, b) cross-sectional sketch of the base.

Subsequently, the base metalization (B1) is performed in a self-aligned process as seen in Fig.2.5, in which the base contact is established. This works because of the undercut of the emitter and the thinner base metal compared to the emitter semiconductor thickness. The pretreatment before the metalization and the metal sheet resistance have a significant impact on the f_{max}.

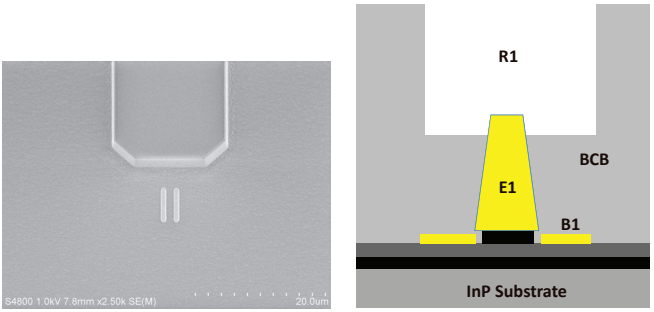

Figure 2.6 Illustration of the planarization and emitter reveal process, a) SEM micrograph of the dry etched BCB, b) cross-sectional sketch of the planarization.

After the base contact is established, the exposed semiconductor of the emitter and base is encapsulated with SiNx, to prevent the emitter-base diode from oxidizing. With the finished diode, the first planarization with BCB follows. To reveal the emitter top and provide a suitable trench for the upcoming ground metal, the BCB is dry etched (R1) as seen in Fig.2.6. The detailed description and development for a suitable dry etch recipe is described in chapter 3. In this step it is necessary to have a sufficient height of the emitter sticking out of the BCB for a good emitter-ground metal contact. Therefore, the etching must be maintained within a sufficient depth but at the same time shallow enough, to avoid a short circuit to the base.

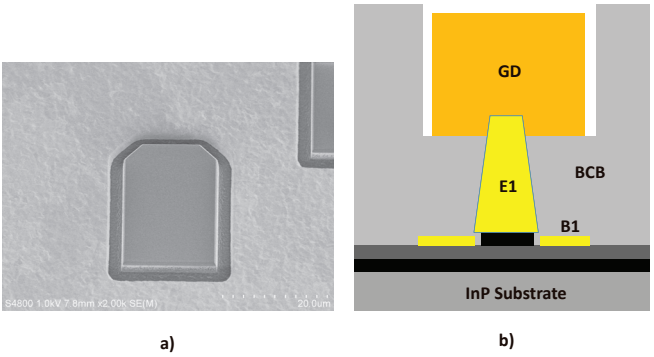

Figure 2.7 Illustration of the GD process, a) SEM micrograph of the electroplated ground metal, b) cross-sectional sketch of the grund metal.

With the emitter heads sticking out of the BCB and a dry etched trench, the ground metal (GD) can be applied by electroplating. The ground metal needs to be on the same vertical