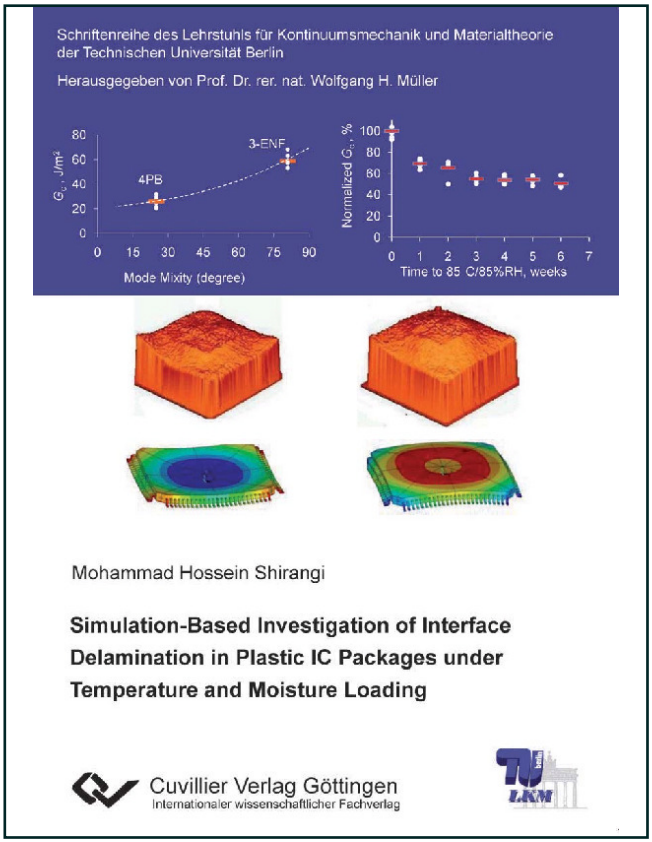
Mohammad Hossein Shirangi (Autor)

Simulation-based Investigation of Interface Delamination in Plastic IC Packages under Temperature and Moisture Loading



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Chapter 2 Reliability in Electronic Packaging

2.1 Introduction to Packaging Processes

The manufacturing phase of an integrated circuit can be divided into two steps. The first, wafer fabrication, is a sophisticated and intricate process of manufacturing the silicon chip. The second, assembly, is a highly precise and automated process of packaging the die. Those two phases are commonly known as “Front-End” and “Back-End”, respectively (quoted from STMicroelectronics).

Plastic Encapsulated Microcircuits (PEMs) are manufactured through a series of sequential processes, widely using metals and polymers in various forms such as in leadframes, encapsulants, adhesives, underfills, molding compounds and coatings (Seraphim *et al.*, 1989; Tummala, 2001). Fig. 2.1 shows typical processes undertaken to fabricate these plastic IC packages.

In the first step, large wafers containing up to several semiconductor chips are fabricated in a wafer fab. These finished wafers coming out of the wafer fab are electrically tested by contacting the exposed bond pads with a probe card. The purpose of this pretest is to early sort out circuits that will not likely result in functional products (van Roosmalen, 2006). The next step after the manufacturing of wafers is the packaging. Typically the wafers must be first prepared to gain the chip with required dimensions. In the following, the main steps from chip preparation to final steps of chip packaging will be reviewed (Tummala, 2001, van Driel 2007, van Roosmalen, 2006):

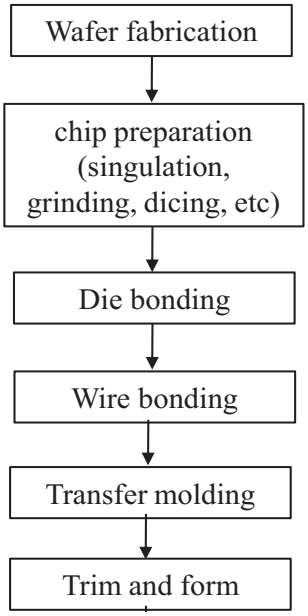

Figure 2.1 Manufacturing process of electronic IC packages.

1. *Chip preparation*: A typical thickness for many compact packages today is ~0.5 mm, almost the same as a standard wafer thickness, implying that most of the wafer backside will need to be removed to fit the eventual outline, this process is called *grinding*. Next, the ICs are cut out of the wafer and can be used for further 'single' processing. This is done at room temperature using a circular sawing or a laser cutting process (*sawing*).
2. *Die bonding*: The packaging process itself involves die attach and encapsulation, each cluster being a conglomerate of shapes and processes in itself. In the die bonding process, the single IC is attached on a carrier material, usually a metal called leadframe, by using some kind of polymeric die attach materials or in some cases by solder materials. Typical process temperature is 150-175°C for die attach and up to 300°C for solder die attach.
3. *Wire bonding:* To connect the die to its environment, the basic choice is between wire bonding and flip-chip technology. In a wire bonding process, the die is fixed into position with a metal-filled epoxy film or paste adhesive or, to allow operation at high die power dissipation, through soldering. A continuous wire, usually gold, is connected to the first bond pad by ultrasound-enhanced thermal compression, then stretched out and welded to the corresponding pin on the external connection structure. That structure will typically be a strip holding multiple patterns, meant to be encapsulated in the molding process, the so-called leadframe. After the weld is made, the wire is cut with a flame of electric arc and brought to the next bond pad, restarting the sequence. In power applications, the thin gold wires may be replaced by thick copper wiring or by aluminum straps. Wire bonding is still the major form of first level interconnection in the world today. At present, over 95% of the manufactured packages (in volume) are wire bonded and the majority of wire bonding is done with thermosonic gold ball bonding. A typical process temperature is 200-220°C.

4. *Chip coating*: For protection of the IC top surface a chip coat material can be used. The chip coat is a highly viscous liquid or paste that encapsulates the IC – mostly epoxies or silicones, with some inorganic filler. A typical process temperature is 150°C.
5. *Transfer molding process*: Transfer molding is the process most commonly used for die encapsulation. Epoxy resin liquefied by high temperature and pressure is forced through a mold chase over the die and leadframe and into the cavity on the frame where the die was placed earlier. The hardened epoxy eventually forms the body of the final package. In this process, the semiconductor IC, wires, and carrier are encapsulated by an epoxy-based material called Epoxy Molding Compound (EMC). The process temperature is about 175°C, followed by a 3 to 6 hours curing step at 175°C. The EMC materials as well as the transfer molding process will be introduced in Chapter 3 in more detail.
6. *Mark*, *Trim and Form*: Finally, the packages are marked and by a trim and form process redundant materials are removed.

Fig 2.2 shows some plastic packages, some of which will be used for reliability investigation in this work. In addition, the cross-section of a TQFP-epad package is illustrated in Fig. 2.3. In this epad package type, the leadframe is exposed to bottom surface of the package for increasing thermal capabilities.

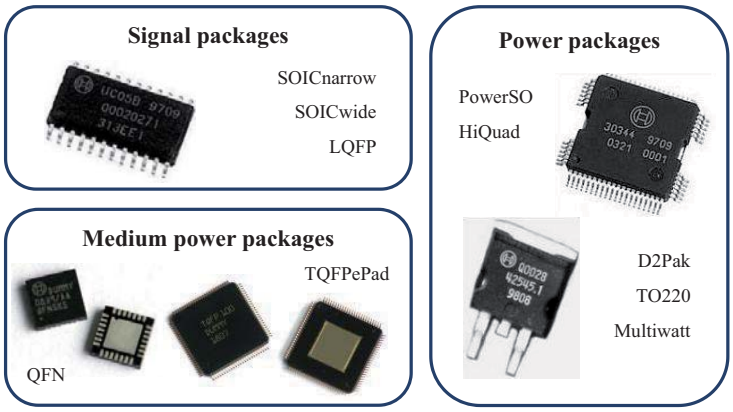

Figure 2.2 Some plastic packages used in automotive industry (courtesy of Robert Bosch GmbH).

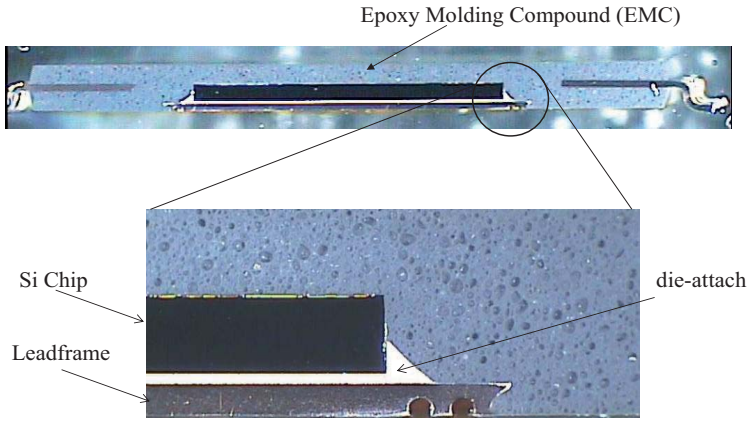

Figure 2.3 Cross-section of a TQFP-epad package.

After the IC packages are fabricated and qualified, they will be store and transported until they are used for their finial surface mount technology via a soldering process to mount these devices on the Printed Circuit Board (PCB). Reflow soldering is the most common method of attaching IC packages and other surface mount components to a circuit board. The goal of the reflow process is to melt the solder alloy particles within the solder paste without overheating and damaging the electrical components. Heating may be accomplished by passing the assembly through a reflow oven or under an infrared lamp or by soldering individual joints with a hot air pencil.

Today, environmental considerations force the so-called lead-free solder materials and the removal of lead materials from microelectronic systems. The materials used so far for the soldering are conventional PbSn eutectic soldering materials that induce automatic alignment of misplaced or non-flat die by surface tension. This phenomenon, together with the quite limited temperature budget imposed by advanced Si wafer technologies, limits the range of reliable alternatives. The alloy SnAgCu is a frequently used lead-free solder replacement for the solder reflow process (van Roosmalen, 2006). These lead-free solder materials need higher temperatures up to 260°C due to their higher melting point. These elevated reflow temperatures are more damaging for the reliability of the IC devices and cause several reliability problems.

2.2 Reliability Tests of Electronic Packages

In the early 1950s, the reliability problems drew attention due to the needs to understand the failure mechanism of unreliable components in US Air Force equipment and quickly, many problems were investigated on a wide front, such as measuring, predicting, and testing of the parts, equipments, even the system reliabilities (Zhang, 2007). However, the microelectronics industry had started booming in the late 1950s. The rapid progress of new designs, new materials, manner of fabrications, operation conditions, application criteria, etc. negated the existing data and models. The establishment of new reliability data on the new devices required expensive testing and was time-consuming. Even further, the improvement of analysis of new data could not catch up the development of new devices. Hence, reliability physics, or “physics of failure”, was created in the early 1960s. Researchers tried to establish the quantitative reliability requirements for devices, and related the fundamental physical and chemical behavior of materials to reliability parameters.

As the emphasis for decreasing costs and time to market in the semiconductor industry becomes even stronger, efficient and effective reliability qualification of products becomes more critical. Reliability qualification is often the last step before manufacturing release of a product and can thus directly impact the time to market. To uncover specific construction, material, and/or process related marginalities, semiconductor devices are qualified using specially designed tests in order to ensure that they have sufficient life so that failures do not occur during the normal usage period. These tests are called reliability tests and their specific purpose is to determine the

failure distributions, evaluate new designs, components, processes and materials, discover problems with safety, collecting reliability data, and to perform reliability control (van Driel, 2007). Reliability tests are classified under various names according to the test format, purpose, method of applying stress, and other factors. In reliability tests, environmental conditions (temperature, moisture) are extrapolated such as to accelerate the circumstances under which the product could fail. Historically, a number of standard tests have been defined by worldwide consortia such the Joint Electron Device Engineering Council (JEDEC), the institute for Interconnection and Packaging electronic Circuits (IPC) and the International Electro-technical Commission (IEC). Table 2.1 describes some of these testing methods (Siliconfareast, 2009, van Driel, 2007).

Table 2.1 Common reliability testing methods of semiconductor packages.

Reliability Test	Reference Specs	Conditions
Solder Heat Resistance Test (SHRT)	JEDEC JESD22-A113	- 24 hours Bake at 125C - Temperature/Humidity Soak based on MSL - 3X IR Reflow at the prescribed peak temperature (about 235C for non-Pb-free parts; 260C for Pb-free)
Temperature Cycle Testing (TCT)	JEDEC JESD22-A104	- Mil Std 883 Method 1010: - Must be conducted for a minimum of 10 cycles
Thermal Shock (TS)	JEDEC JESD22	- Must be conducted for a minimum of 15 cycles
Autoclave or Pressure Cooker Test (PCT)	JEDEC JESD22-A102	- Preconditioned - Soak at 121C/100% RH for 168 hours - Pressure = 2 atm - Unbiased
Highly Accelerated Stress Test (HAST)	JEDEC JESD22-A110	- Preconditioned - Soak at 130C/85% RH for 96 to 100 hours - Biased
Temp Humidity Bias (THB) Test	JEDEC JESD22-A101	- Preconditioned - Soak at 85C/85% RH for 1000 hours - Biased

In the following, some of these reliability tests together with the failure mechanisms expected from the test will be discussed.

Solder Heat Resistance Test (SHRT): As its name implies, SHRT is a reliability test for assessing the ability of a device to withstand the thermal stresses of the soldering process. It is also sometimes referred to as 'preconditioning' if it precedes another reliability test. Preconditioning is usually done for surface-mount devices prior to PCT, THB, and HAST, all of which accelerate corrosion if the package cracks after preconditioning. Preconditioning may also be done prior to temperature cycling or thermal shock, both of which aggravate incipient mechanical failures induced by the precondition. In effect, preconditioning simulates the board soldering process while the tests following it simulate the stresses that the device will experience after mounting.

In order to perform moisture preconditioning on plastic IC packages, different conditioning levels are available, each posing a different degree of damage on the plastic parts. Moisture Sensitivity Levels (MSL) are introduced by JEDEC standards and for each IC package the MSL level with which the package was successfully qualified should be reported. MSL levels are 1 to 6, with 1 being the most severe and 6 being the less severe one. For example, in an MSL1 assessment, the IC package should withstand experimental conditions of 85%RH (Relative Humidity) at 85°C for a period of 168 hours. However, in an MSL6 assessment, the IC package should withstand experimental conditions of 60%RH/30°C for a period of 6 hours.

Temperature Cycle Testing (TCT): TCT determines the ability of parts to resist extremely low and extremely high temperatures, as well as their ability to withstand cyclic exposures to these temperature extremes. A mechanical failure resulting from cyclical thermo-mechanical loading is known as a fatigue failure. During this test, IC packages are subjected to a typical temperature change from, *e.g.,* -50°C to 150°C for a number of cycles. Typical numbers of cycles are 200 to 1000 or more, and depend on the application. For instance, the demand for IC packages aimed for an automotive application is higher than those aimed for customer application.

Thermal Shock (TS): TS is performed to determine the resistance of the part to sudden changes in temperature. The parts undergo a specified number of cycles, which start at ambient temperature. The parts are then exposed to an extremely low (or high) temperature and, within a short period of time, exposed to an extremely high (or low) temperature, before going back to ambient temperature.

Autoclave Test, or **Pressure Cooker Test (PCT):** This test is a reliability test performed to assess the ability of a product to withstand severe temperature and humidity conditions. It is used primarily to accelerate corrosion in the metal parts of the product, including the metallization areas on the surface of the die. It also subjects the samples to the high vapor pressure generated inside the autoclave chamber. Autoclave testing consists of soaking the samples for 168 hours at 121°C, 100% RH, and 2 atm. Intermediate read points at 48H and 96H may also be employed.

Temperature, Humidity, Bias (THB): THB is a reliability test designed to accelerate metal corrosion, particularly that of the metallizations on the die surface of the device. Aside from temperature and humidity which are enough to promote corrosion of metals in the presence of contaminants, bias is applied to the device to provide the potential differences needed to trigger the corrosion process, as well as to drive mobile contaminants to areas of concentration on the die. THB testing employs the following stress conditions: 1000 hours at 85°C, 85% RH, with bias applied to the device. The main drawback of THB is its long duration, necessitating weeks before useable data are obtained.

Highly Accelerated Temperature/Humidity Stress Test (HAST): This test was developed as a shorter alternative to THB Testing. If THB testing takes 1000 hours to complete, HAST results are available within 96-100 hours. Like THB testing, HAST accelerates corrosion, particularly that of the die metal lines and thin film resistors. HAST requires preconditioning and is conducted with electrical bias at 130°C and 85% RH for 96-100 hours.