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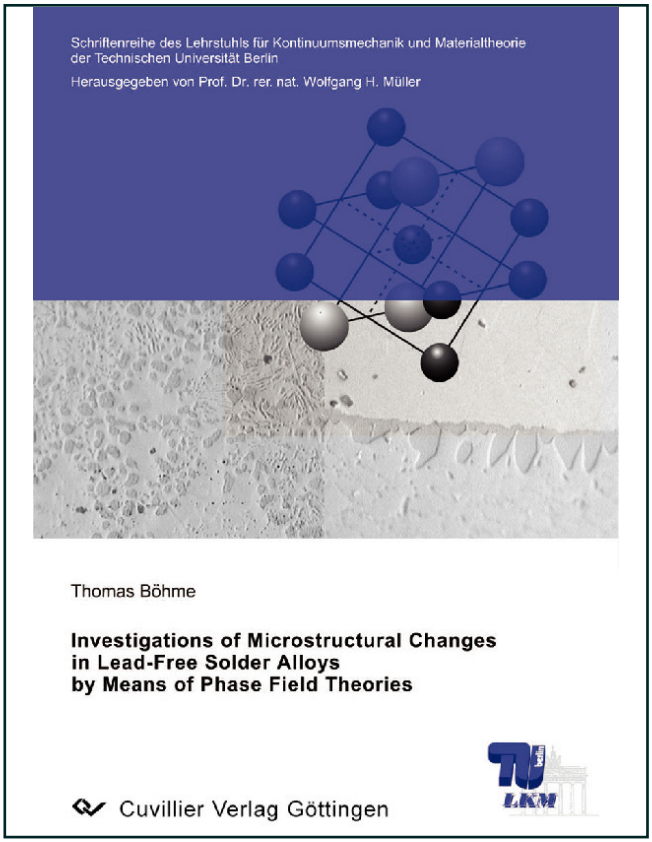
Investigations of Microstructural Changes in Lead-Free Solder Alloys by Means of Phase Field Theories



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Das Fehlen von Wissenschaft, das heißt Unkenntnis von Ursachen, macht dazu geneigt, oder besser, zwingt dazu, sich auf den Rat und die Autorität anderer zu verlassen.

Thomas Hobbes, (1588 - 1679)

Chapter 1

Introduction

1.1 Tendencies in Microelectronic Packaging

1.1.1 Technological Trends

As a consequence of the "technological revolution" in the last 20 years there is an ongoing miniaturization in the area of microelectronics driven by an increasing requirement for mobility (*e.g.*, mobile phones or notebooks) and more complex functionalities (*e.g.*, multimedia or fly-by-wire systems). Therefore the minimal feature size[1] within semiconductors continuously decreases whereas the number of transistors rapidly grows (*cf.*, Fig. 1.1). This process results in the use of smaller and smaller amounts of matter, and, consequently, the demands on strength and lifetime of the used materials considerably rise while the structural size is continuously reduced.

1.1.2 Environmental Concerns

In addition to the technological trends *environmental initiatives* become increasingly important, in particular in the high-technology countries. The purpose of these activities is the reduction of electronic waste and/or the hazardous substances within (*e.g.*, Cd, Hg, Pb). So, for instance *the annual amount of the German electronic waste is more than four times of the volume of the 140 m high* Cheops *pyramid in Egypt* (estimation of the German environmental organization BUND, [118]) or *130 million cell phones were estimated to be retired in 2005 in the US. This value corresponds to 81.250 pounds of lead resulting from the lead solder used in the printed wiring boards, which enter the waste stream.* (estimation of the environmental organization Inform, [48]).

[1] The minimal feature size defines 1/2 of the distance between cells in a dynamic RAM (DRAM).

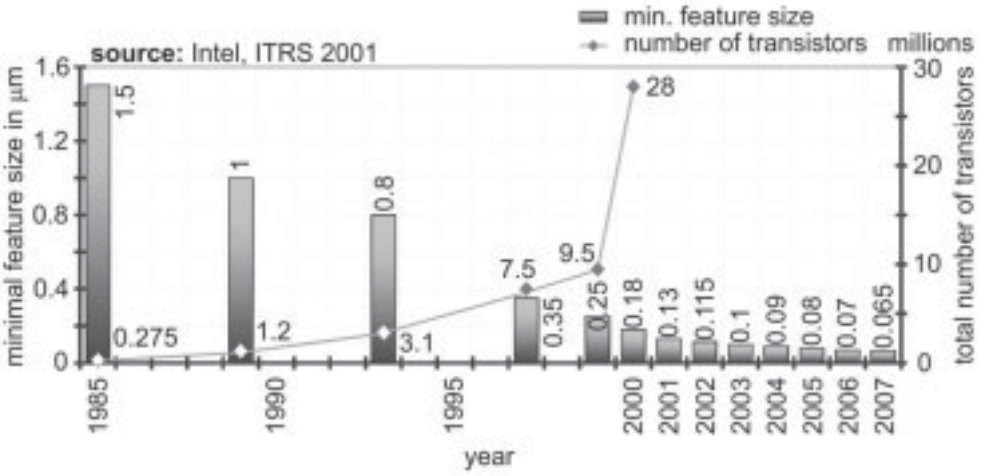

Figure 1.1: The development of the minimal feature size (partially expected) and the number of transistors in microelectronics, source: Intel, [62] and ITRS, [63].

These citations underscore the problems following from the technological progress and, thus, environmental initiatives are strongly necessary. In what follows the ecological efforts are briefly explained for the three regions of *Europe*, *Asia*, and the *USA*. However, although the regulations differ, the remaining time for broad-scale use of traditional Sn-Pb-based solders is certainly limited and, consequently, adequate lead-free materials must be investigated and evaluated, in particular from a theoretical and experimental materials science point of view.

a. Europe, in particular Germany

In the EU two initiatives are worth mentioning: the directives WEEE (directive on Waste Electrical and Electronic Equipment, [33]) and the RoHS (Restriction of the use of certain Hazardous Substances in electrical and electronic equipment, [32]), which require the industry to take care of the disposal of electronic devices and which regulate/forbid the use of certain substances, such as Pb, Hg, or Cd in electronics. These directives must be transposed into national law by the member states. Germany, for example, passed the so-called "ElektroG" law, [53], which, among other things, restricts the use of Pb as of July, 1st, 2006. However, the technological progress could not follow the original RoHS restrictions in the pre-defined period, so that exemptions[2] were subsequently included, [56].

[2]For example, Pb and Cd in optical and filter glasses, Pb in high melting temperature type solders (*i.e.* Sn-Pb solders with more than 85% Pb) and in solders, which internally complete a viable electrical connection to certain integrated circuit packages (Flip Chips) are further permitted (exemption until 2010).

b. Asia, in particular Japan and China

Undoubtedly, Japan represents the "trendsetter" in the area of so-called "green electronics". Already since 1990 the Japanese companies voluntarily committed in so-called *Environmental Protection Charters* to avoid waste and to save natural recourses. Based on the JEIDA[3] roadmap, [50], which appeared in 1999 these agreements were successively extended by specific aims, in particular with respect to the lead-free legalization process in the microelectronic sector. In April 2001 (*i.e.*, two years before the adequate EU directive WEEE were passed) the *Home Electric Appliance Recycling Law* were put into full force, which regulates the response of the manufacturer for the disposal of old electronics, [107].

The fast environmental progress in Japan is also based on the fact, that the leading electronic companies, such as Fujitsu, Toshiba, Sony or Panasonic use the environmental awareness for marketing strategies and compete for an ecological image. For instance, Sony already introduced in March 2001 the first lead-free camcorder on the market, [50]. Moreover, up to the middle of 2002 about 50% of the Pb solders were eliminated by the most Japanese electronic companies compared with the level of 1997, [95].

In China the Ministry of Information Industry has introduced an RoHS-like law called *Management Methods for Pollution Prevention and Control in the Production of Electronic Information Products*, [95], which represents Chinese policy on reduction of hazardous substances used in electronic information products. It includes manufacturing, imports, *and* packing, but explicitly exclude exporting products. In a first step, products containing certain toxic constituent parts must be labeled since March 2007, [49]. First concrete restriction, and without exceptions as in the RoHS, are planned for 2008.

c. USA

The U.S. Environmental Protection Agency has introduced a *Toxic Release Inventory* rule, which lowers the reporting thresholds for the emission of lead and lead compounds to 100 pounds (approx. 45 kg) for facilities and companies, [95], by April 2001. Furthermore one finds in different states rules regulating the use of lead for example in paint and batteries. However, although various states plan lead-free and/or recycling regulations for electronic appliances, there is no communicated federal position.

In 2003 California passed the so-called *Electronic Waste Recycling Act*, which includes the recycling and the design of optical electronic equipment, [95]. Furthermore the law restrict, similar to the EU RoHS directive, the use of certain hazardous substances

[3] Japan Electronics Industry Development Association.

(*e.g.* Pb, Hg, Cd) by January 2007, [49].

Beside these "governmental efforts" various globally acting companies increasingly head toward lead-free products. For example, Intel recently announced the change to lead-free processors, [99].

1.2 Solder Materials

1.2.1 Solders in Microelectronic Packaging

The last paragraph already indicates the key role of solder materials in microelectronics. Consequently the question arise: Where and for which reasons solders are used in microelectronic packaging. Figure 1.2 illustrates various packaging variants typically used. Obviously, solder materials assume two important tasks: **(a)** they guarantee

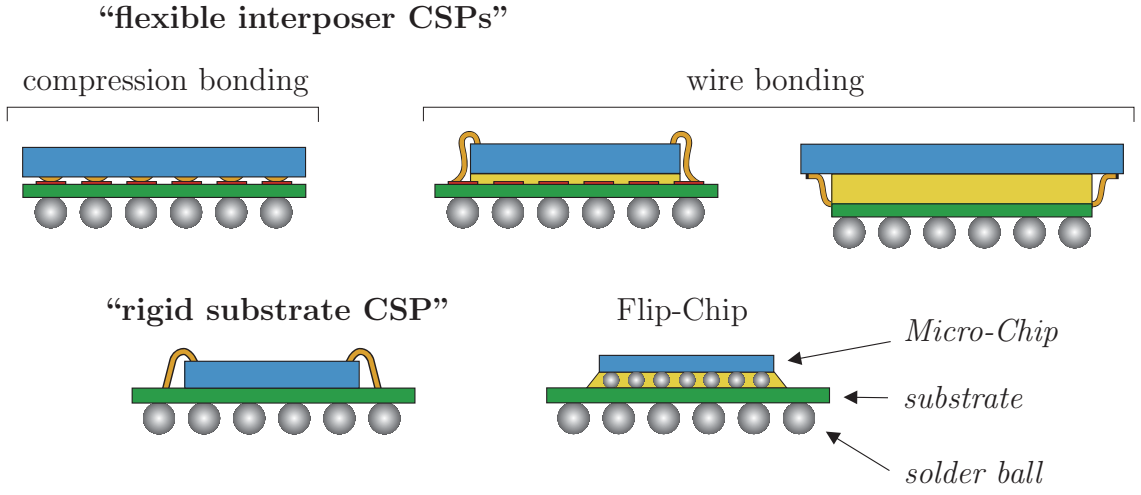

Figure 1.2: Different types of Chip Scale Packaging (CSPs).

the electrical connection between the chip-unit and the electronic circuits within the substrate and **(b)** they provide the mechanical connection of the different electronic components on the printed circuit board. Consequently there is a specific demand on strength and lifetime of the used materials.

Furthermore the assembling by means of *Surface Mount Technology*[4] (SMT) and *reflow soldering*[5] requires moderate melting temperatures for the solder materials,

[4]In this manufacturing procedure the electronic components are directly – *i.e.*, without the use of pins – soldered on the circuit board.

[5]Here the substrate/board is firstly completely assembled, and the joining connection is realized by a subsequent heat treatment of the whole electronic device, *i.e.*, chip unit, substrate and (solid) solder.

so that the supersensitive chip units do not fail during the joining process. Indeed, the above manufacturing procedures allow an extremely compact packaging (*e.g.*, the application of chips on both sides of the substrate), but, in contradiction to the conventional Pin-Through-Hole (PTH) assembling, SMT solder joints increasingly tend to rupture, [105]. Here the conventional eutectic Sn-Pb solder ($c_{\mathrm{Sn}} = 0.63$) represents a good compromise. On the one hand both components as well as the mixtures have sufficiently low melting temperatures, namely, [119, 1]:

$$T_{\mathrm{Sn}}^{\mathrm{melt}} = 232\,^{\circ}\mathrm{C} \quad , \quad T_{\mathrm{Pb}}^{\mathrm{melt}} = 327\,^{\circ}\mathrm{C} \quad , \quad T_{\mathrm{Sn-Pb}}^{\mathrm{eut}} = 183\,^{\circ}\mathrm{C}\,.$$

On the other hand the containing Pb enables the components at the joint interface, *e.g.*, Sn and Cu, to immediately form InterMetallic Compounds (IMCs) in the molten state (see also Section 1.3). Additionally, Pb reduces the surface tension of Sn, which, in turn, increases the wetting properties of Sn, [1]. Hence lead plays an important role for the resistance of the joining connection and, under the background of the lead-free legalization process, the question about an adequate alternative arises.

1.2.2 Lead-free Materials

In the last years various lead-free alloys became important for the use in microelectronics. Table 1.1 shows different solders, which are under consideration. Here the first five items represent so-called *soft solders*, whereas the last item, Ag-Cu, identifies a typical *brazing alloy* (*i.e.*, $T^{\mathrm{melt}} > 450\,^{\circ}\mathrm{C}$). Obviously, there is no material, which is uniquely favored by the companies due to diverse application fields, country-specific material costs or different material properties. For instance Sn-Cu cannot be used for reflow soldering since the relatively high melting temperature (*cf.*, Table 1.1) does not allow sufficiently long soldering time. Here experts recommend to use Sn-Ag, whereas Sn-Cu is considered for *wave soldering* applications, [1].

Solder	Composition (mass concentration)	T^{melt} in °C
Sn-Ag-Cu	$c_{\mathrm{Ag}} = 0.038$, $c_{\mathrm{Cu}} = 0.007$ (eutectic)	217
Sn-Bi	$c_{\mathrm{Bi}} = 0.580$ (eutectic)	138
Sn-Cu	$c_{\mathrm{Cu}} = 0.007$ (eutectic)	227
Sn-Ag	$c_{\mathrm{Ag}} = 0.035$ (eutectic)	221
Sn-Zn	$c_{\mathrm{Zn}} = 0.090$	199
Ag-Cu	$c_{\mathrm{Cu}} = 0.290$ (eutectic)	778

Table 1.1: Various lead-free solder materials under discussion, source: [83],[112]

In contrast to soft solders, brazing materials, such as the binary solder Ag-Cu, are usually employed for highly-stressed or high temperature connections, *e.g.*, for gas pipe joints. In particular, in microelectronics brazing materials are used for high-performance applications, in which – due to lower thermal expansion – ceramics-based packages are preferred over plastics. Here the silicon chip must be fixed to

a metallized ceramic substrate, whereas the occurring ceramic-metal connection is realized by means of brazing solders, [69, 97].

However, soft solders as well as brazing materials show similar material phenomena, in particular micro-structural changes.

1.3 Microstructures in Solders

1.3.1 Phenomenology

From a microscopic point-of-view solder balls as illustrated in Figure 1.2 are basically subjected to *four* different micro-structural changes, *cf.*, Fig. 1.3:

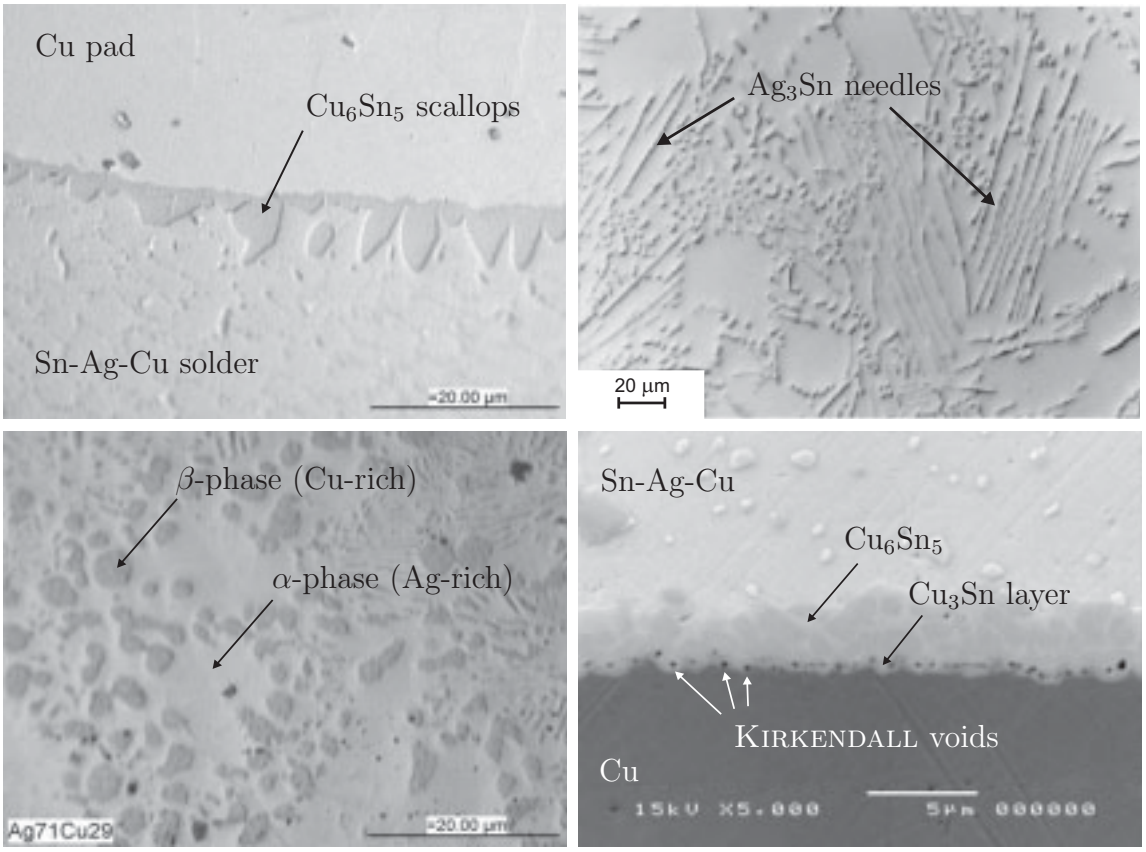

Figure 1.3: Various mircrostructural effects observed in solder materials. 1st row (left): IMC scallops (Cu_6Sn_5) at the interface solder/substrate. 1st row (right): IMC needles (Ag_3Sn) in the solder bulk, source: [92]. 2nd row (left): Phase separation by spinodal decomposition in eutectic Ag-Cu after 40h heat treatment. 2nd row (right): Kirkendall void formation in the thin Cu_3Sn layer at the interface solder/substrate, source: [120].

(a) *Formation and growth of scallop-shaped InterMetallic Compounds*[6] *(IMCs) at the interface solder/substrate*: Here the IMCs are formed and grow in the molten state due to an *interfacial reaction*. In the case of a Cu substrate and an Sn-containing solder (*e.g.*, Sn-Ag-Cu) this reaction takes place between Cu and Sn and necessitates a mass transport from the substrate to the solder, [70]. Primarily by means of repeating reflow soldering the "scallops" further expand and may have a positive influence on the strength and lifetime of the solder joints, because they guarantee a "dovetail connection". In contrast, there are stress peaks in the vicinity of the IMCs leading to crack initiation. Consequently, the positive effects are limited by a critical size of the scallops.

(b) *IMC formation in the interior of the solder*: One of the most popular examples for this phenomenon are Ag_3Sn precipitates observed in lead-free SAC solders (Sn-Ag-Cu). These IMCs typically occur in form of needles or plates and are formed due to a chemical reaction in the molten state during soldering. However, once developed, they do not essentially grow within the solid state. Nevertheless, the IMCs are - in contradiction to the solder - extremely stiff and brittle, which yields stress peaks and mismatching during, *e.g.*, thermal cycling of the electronic device.

(c) *Phase separation and coarsening through spinodal decomposition and* Ostwald *ripening in the solder bulk*: In contrast to IMC-formation phase separation and coarsening are diffusion processes *exclusively* driven by aspects of thermodynamical stability and interfacial energy minimization, *cf.*, Section 1.3.2 and [23]. The resulting "composite" of different phases can be interpreted as a "particle reinforced material" in which the stiffer phase acts as the reinforcement. Unfortunately mechanical failure, such as cracks, favorably grow along the phase boundary (*cf.*, Figure 1.4) which result, among other reasons, from thermal mismatching. Thus the benefit of phase dispersion is limited by a critical phase size.

(d) Kirkendall *voiding at the interface solder/substrate*: Generally speaking, the Kirkendall effect is induced due to a difference in the diffusion coefficients of to neighboring regions, [25]. In particular the occurring IMCs show considerably different diffusion coefficients with respect to Cu. Therefore, the diffusion of Cu from the pad via the interface Cu/Cu_3Sn into Cu_3Sn is much slower than the diffusion of Cu from Cu_3Sn into the Cu_6Sn_5 scallops, which also cannot be corrected by the invers diffusion of Sn through the Cu_6Sn_5/Cu_3 interface, [120]. As a consequence vacancies on the lattice sites remain within the Cu_3Sn layer, which coalesce to macroscopic voids by means of vacancy diffusion. Additionally, stress peaks in the vicinity of the voids result in further void growth and micro crack formation, which may proceed failure.

[6] The IMCs are often called in literature "Intermetallic Phases" or "ordered phases." This notation is quite misleading, since it leads to the confusion with phases known from thermodynamics, which are not formed from chemical reactions.