
Contents

List of Figures, Tables, Symbols	vi
Summary	xi
1 Introduction	1
1.1 Motivation	1
1.1.1 Multipurpose Technology Products	1
1.1.2 On-chip wiring demands	2
1.1.3 Three-dimensional integration	3
1.1.4 Biologically inspired neural processing	4
1.2 Interconnect needs for 3D-integration	5
1.2.1 Peripheral Interconnects	5
1.2.2 Area interconnects	6
1.2.3 Through-chip vias	7
1.2.4 Conclusion	9
1.3 A new 3D-chip-integration concept	11
1.3.1 Process chain	11
1.3.2 Critical steps	13
1.4 Subject of this thesis	15
1.4.1 Scope	15
1.4.2 Procedure	17
1.4.3 Outline	18
2 Thinning and wafer handling	19
2.1 Introduction	19
2.1.1 Concepts for waferbonding	19
2.1.2 Concepts for wafer thinning	20
2.2 Wafer bonding	21
2.2.1 Permanent bond to handling substrate	22
2.2.2 Evaluation of temporary bonding techniques	24
2.2.3 Temporary bonding with surface topology	26
2.2.4 Results	28
2.3 Wafer thinning	29
2.3.1 Mechanical wafer thinning: Lapping	29
2.3.2 Chemical mechanical polishing: CMP	31
2.3.3 Chemical thinning	33
2.3.4 Results	34
2.4 Conclusion	36

CONTENTS

3 Patterned electroplating and via filling	37
3.1 Introduction	37
3.1.1 Challenges	38
3.1.2 Methods of electroplating	39
3.1.3 Plating characteristics on plain substrates	40
3.2 Through-mask plating	41
3.2.1 Plating setup	41
3.2.2 Patterning	41
3.2.3 Seed layer removal	43
3.2.4 Results	44
3.3 Via filling process evaluation	45
3.3.1 Factors influencing feature filling	45
3.3.2 Via preparation	47
3.3.3 Via filling	49
3.3.4 Results	49
3.4 Conclusion	52
4 Bonding and chip-stacking	55
4.1 Introduction	55
4.1.1 Available metallic bonding techniques	56
4.1.2 Solid liquid interdiffusion	59
4.1.3 Choice of bonding method	61
4.2 The SOLID process	61
4.2.1 Cu—Sn intermetallic system	62
4.2.2 Dynamics of solder layers	64
4.3 SOLID bonding process evaluation	66
4.3.1 Bonding with unstructured metal layers	66
4.3.2 SOLID bonding evaluation with thinned chips	68
4.3.3 Bonding with patterned area metallization	69
4.3.4 Results	70
4.4 Chip-stacking with through-chip vias	73
4.4.1 Results	74
4.5 Conclusion	75
5 Scaling of microjoints	77
5.1 Introduction	77
5.1.1 Optimization potential in SOLID bonding	77
5.1.2 Prerequisites for scaling of microjoints	80
5.1.3 Kinetic control with metallic separation layers	83
5.2 Phase growth kinetics with metal barriers	85
5.2.1 Material selection criteria	86
5.2.2 Solid state phase growth	86
5.2.3 Results	87

CONTENTS

5.3	Wetting of barrier layers	91
5.4	Conclusion	92
6	Outlook	93
A	Experiments and samples	95
A.1	List of samples and processed substrates	95
A.2	Mask Layouts	96
B	Processes	99
B.1	Process chain for wafer elements	99
B.2	Chip-stacking sequence for flip-chip-bonder	100
B.3	Lithography	101
B.4	Ion-beam sputtering	101
B.5	Lapping sequence	104
C	Equipment	105
C.1	Electroplating setup	105
C.2	Waferbonding presses	105
C.3	Thinning equipment	106
C.4	Flip-chip bonder	107
Bibliography		109
Acknowledgement		119
Curriculum vitae		121