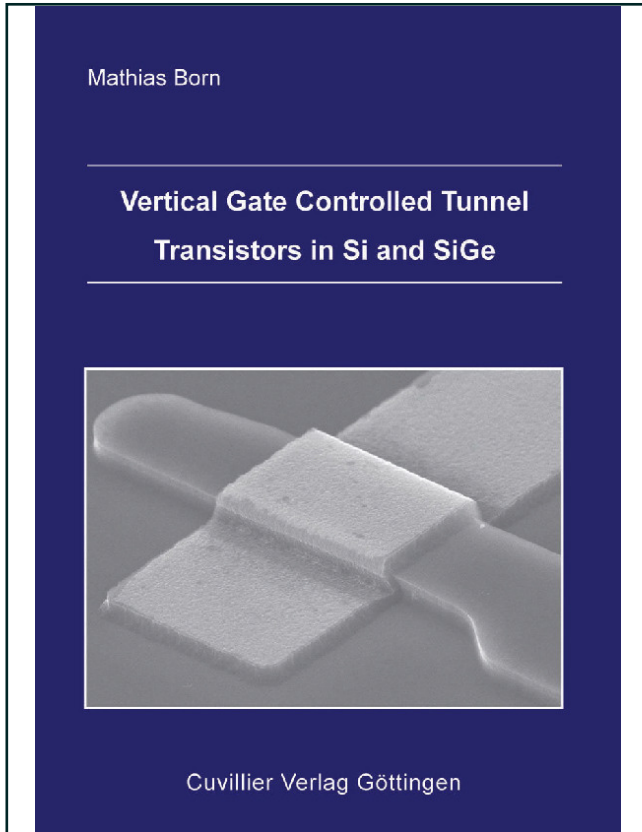




Mathias Born (Autor)

# Vertical Gate Controlled Tunnel Transistors in Si and SiGe



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