



Contents

Abstract	i
Kurzfassung	iii
List of Publications	v
Contents	vii
List of Figures	xi
List of Tables	xv
1 Introduction	1
1.1 Race Conditions	3
1.2 Locking	6
1.3 A Part of the Solution: Atomic Blocks	9
1.4 Goals and Contributions of this Thesis	12
1.5 Outline	15
2 State of the Art and Related Work	17
2.1 Automatic Parallelization	17
2.2 Programming Models	19
2.3 Error Detection Tools	20
2.4 Non-Blocking Algorithms	21
2.5 Efficient Locking Implementations	23
2.6 Summary	24



3	Identification of Atomic Blocks in Parallel Code	25
3.1	Related Work	27
3.2	Identification of Atomic Blocks	33
3.2.1	Assumptions of our Algorithm and the Resulting Limitations	34
3.2.2	Concurrency Analysis	36
3.2.3	Basic Algorithm	37
3.2.4	Sample Execution	39
3.3	Optimizations	41
3.3.1	Removal of Non-Critical Dependences	41
3.3.2	Removal of Dependences over Read-Only Variables	44
3.3.3	Removal of Dependences Between Builtin Data Structures	45
3.3.4	Detection of Concurrent Instructions that Execute in a Single Thread	46
3.4	Summary	47
4	Foundations of Transactional Memory and Lock Inference	49
4.1	Transactional Memory	49
4.1.1	General Concept	50
4.1.2	Software Transactional Memory	51
4.1.3	Overview of SwissTM	53
4.1.4	Advantages and Disadvantages of STM	59
4.2	Lock Inference	60
4.2.1	Lock Inference by Gudka et al.	61
4.2.2	Limitations of Lock Inference by Gudka et al.	64
4.3	Summary	65
5	Combining Lock Inference with Lock-Based Software Transactional Memory	67
5.1	Related Work	68
5.2	Combining Lock Inference with STM	76
5.2.1	Compiler Analysis and Code Transformation	77
5.2.2	Integration in SwissTM	79
5.3	Optimizations	82
5.3.1	Runtime Loop Inspection	82
5.3.2	Specialized Container Data Structures	84
5.4	Summary	88



6	Tuning of Software Transactional Memory Locking Granularity at Runtime	89
6.1	Related Work	90
6.2	Overview of Tuning the Number of Locks at Runtime	94
6.3	Resizing Heuristics	96
6.4	Memory Layout of the Lock Table	97
6.5	Maintaining the Size of the Lock Table	101
6.6	The Resizing Operation	102
6.7	Summary	111
7	Evaluation	113
7.1	STAMP Benchmarks	113
7.2	Hardware and Software Setup	117
7.3	Baseline Measurements	118
7.4	Identification of Atomic Blocks	119
7.5	STM and Lock Inference Optimizations	127
7.6	Summary	141
8	Conclusions and Future Work	143
	Bibliography	149